SONY

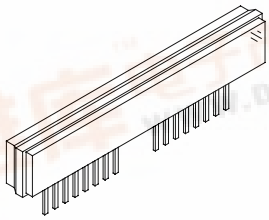
ILX103A

3000-pixel CCD Linear Image Sensor (B/W)

Description

The ILX103A is a rectangular reduction type CCD linear image sensor designed for bar code POS hand scanner and optical measuring equipment use. A built-in timing generator and clock-drivers ensure single 5V power supply for easy use.

16 pin SIP (Ceramic)



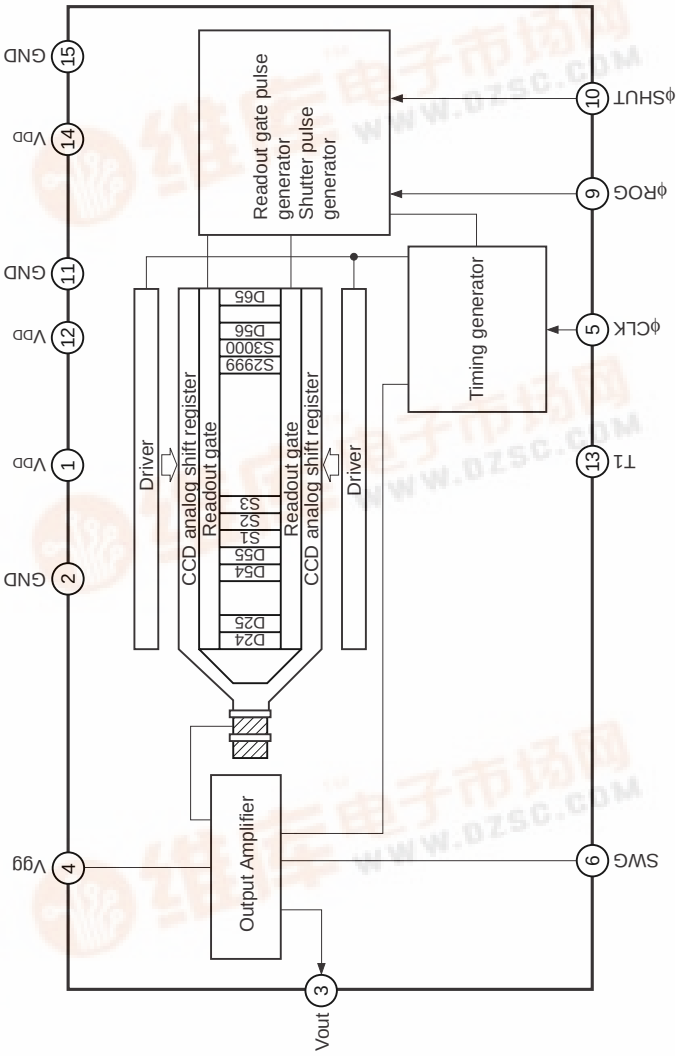
Features

- Number of effective pixels: 3000 pixels
- Pixel size: 7µm × 200µm (7µm pitch)
- S/H output
- Built-in timing generator and clock-drivers
- Output amplifier gain switching function (2-level: switching gain ratio 1:4)
- SIP small package
- Clock frequency: 500kHz (Typ.), 100kHz (Min.), 1MHz (Max.)

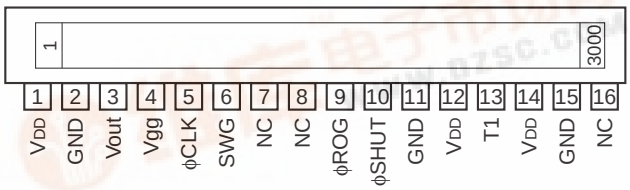
Absolute Maximum Ratings

• Supply voltage	V_{DD}	6	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Internal Structure



Pin Configuration (Top View)



E98X48A91-PS

Pin Description

Pin No.	Symbol	Description
1	V_{DD}	Power supply
2	GND	GND
3	Vout	Signal output
4	Vgg	Output circuit gate bias
5	ϕCLK	Clock pulse input
6	SWG	Control (Output circuit amplification factor ×4/×1)
7	NC	NC
8	NC	NC
9	ϕROG	Readout gate pulse input
10	ϕSHUT	Electrical shutter pulse input
11	GND	GND
12	V_{DD}	Power supply
13	T1	TEST (Connect to GND with 1000pF capacitor)
14	V_{DD}	Power supply
15	GND	GND
16	NC	NC

Mode Description

Output circuit gain	Pin 6 SWG
High	V_{DD}
Low	GND

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	4.5	5.0	5.5	V

Input Pin Capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕCLK pin	$C_{\phi CLK}$	—	10	—	pF
Input capacity of ϕROG pin	$C_{\phi ROG}$	—	10	—	pF
Input capacity of ϕSHUT pin	$C_{\phi SHUT}$	—	10	—	pF

Electro-optical Characteristics (Analog Characteristic) (Note 1)

Ta = 25°C, V_{DD} = 5V, Clock frequency: 500kHz, Light source = 3200K,
IR cut filter: CM-500S (t = 1.0mm), Output circuit gain low mode

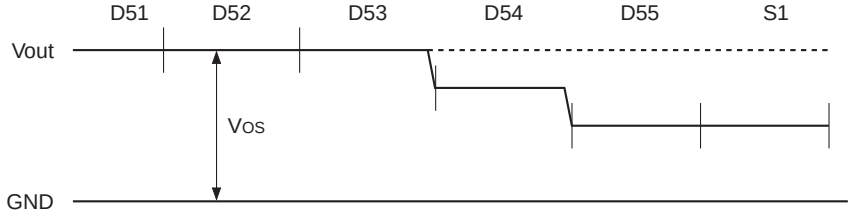
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	52.5	75	97.5	V/(lx · s)	Note 2
Sensitivity 2	R2	—	925	—	V/(lx · s)	Note 3
Sensitivity nonuniformity	PRNU	—	5.0	10.0	%	Note 4
Saturation output voltage	V_{SAT}	0.6	0.8	—	V	—
Dark voltage average	V_{DRK}	—	2.5	6.0	mV	Note 5
Dark signal nonuniformity	DSNU	—	5.0	12.0	mV	Note 6
Image lag	IL	—	5.0	—	%	Note 7
Dynamic range	DR	—	320	—	—	Note 8
Saturation exposure	SE	—	0.01	—	lx · s	Note 9
5V current consumption	I_{VDD}	—	7.0	17.0	mA	—
Total transfer efficiency	TTE	92.0	97.0	—	%	—
Output impedance	Z_O	—	250	—	Ω	—
Offset level	V_{OS}	—	2.5	—	V	Note 10

Note)

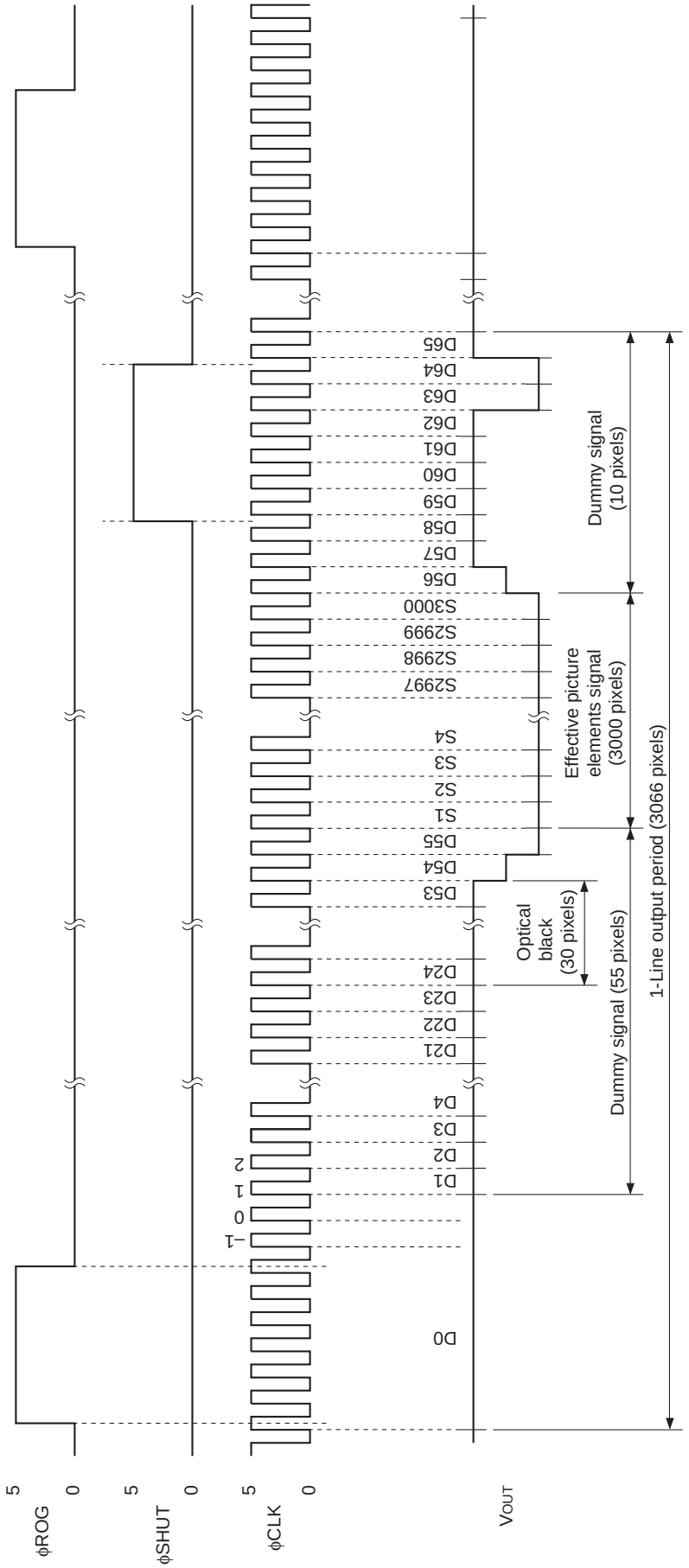
1. In accordance with the given electro-optical characteristics, the even black level is defined as the average value of D24, D25 to D53.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. Light source: LED λ = 660nm
4. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

   The maximum output of the effective pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
5. Integration time is 10ms.
6. The difference between the maximum and average values and the difference between the minimum and average values of the dark output voltage is calculated. The larger value is defined as dark signal nonuniformity. Integration time is 10ms.
7. Typical value is used for clock pulse and readout pulse. V_{OUT} = 500mV.
8. DR = V_{SAT}/V_{DRK}
   When optical integration time is shorter, the dynamic range sets wider because dark output voltage is in proportion to optical integration time.
9. SE = V_{SAT}/R1
10. Vos is defined as indicated below.



Clock Timing Diagram

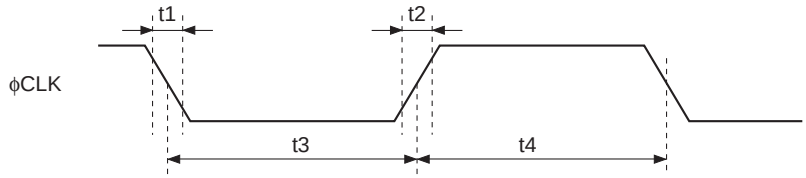


Input Clock Voltage Condition

Item	Min.	Typ.	Max.	Unit
V_{IH}	3.0	V_{DD}	5.5	V
V_{IL}	0.0	—	0.1	V

* This is applied to the all external pulses. (φCLK, φROG, φSHUT)

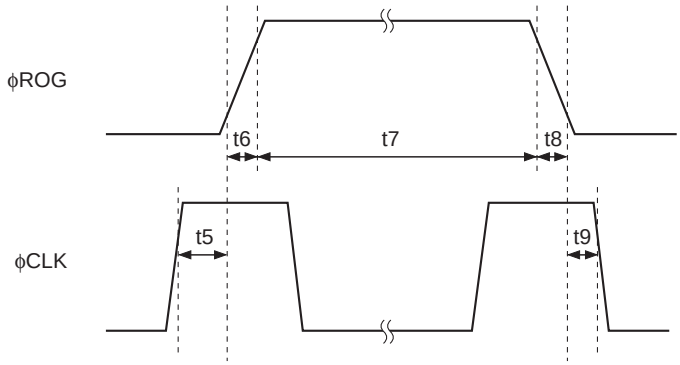
φCLK Timing (For all modes)



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse rise/fall time	t1, t2	0	10	100	ns
φCLK pulse Duty*1	—	40	50	60	%

*1 $100 \times t4/(t3 + t4)$

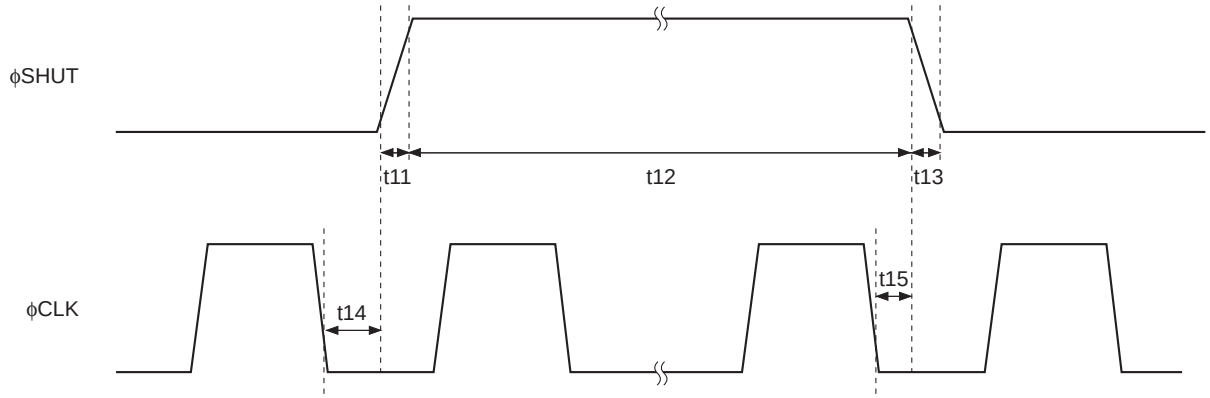
φROG, φCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φCLK pulse timing 1	t5	1/8τ	1/4τ	3/8τ	ns
φROG, φCLK pulse timing 2	t9	1/8τ	1/4τ	3/8τ	ns
φROG pulse rise/fall time	t6, t8	0	10	100	ns
φROG pulse period	t7	6τ	10τ	20τ	ns

Note) τ is the period of φCLK.

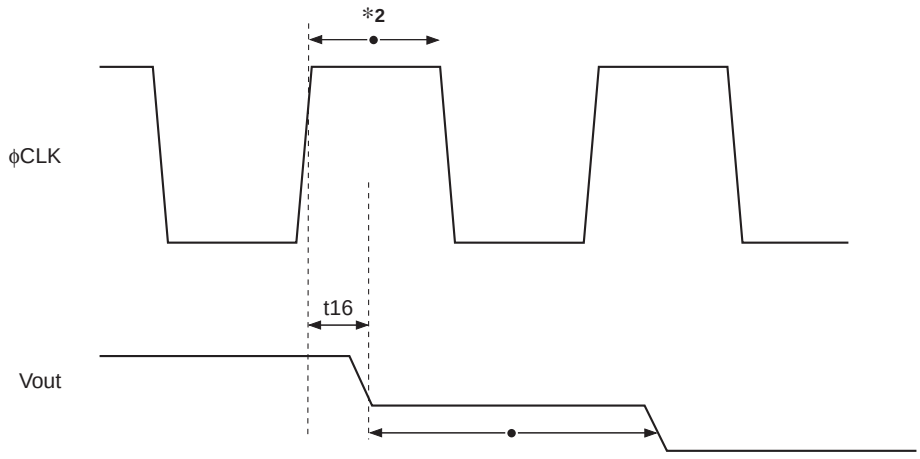
ϕSHUT, ϕCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
ϕSHUT pulse rise/fall time	t11, t13	0	10	100	ns
ϕSHUT pulse period	t12	4000	5000	—	ns
ϕSHUT, ϕCLK pulse timing 1	t14	150	200	250	ns
ϕSHUT, ϕCLK pulse timing 2	t15	150	200	250	ns

Note) The high periods of ϕROG and ϕSHUT are separated for 10τ or more.

ϕCLK Output Signal Timing *1

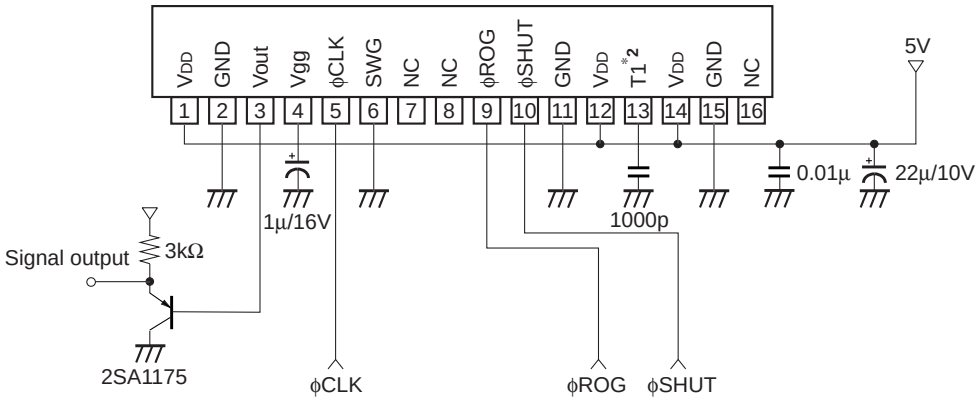


Item	Symbol	Min.	Typ.	Max.	Unit
ϕCLK-Vout output delay time1	t16	—	230	—	ns

*1 fck = 500kHz, ϕCLK Duty = 50%, ϕCLK rise/fall time = 10ns

*2 • is data period.

Application Circuit (Output gain low mode)*1



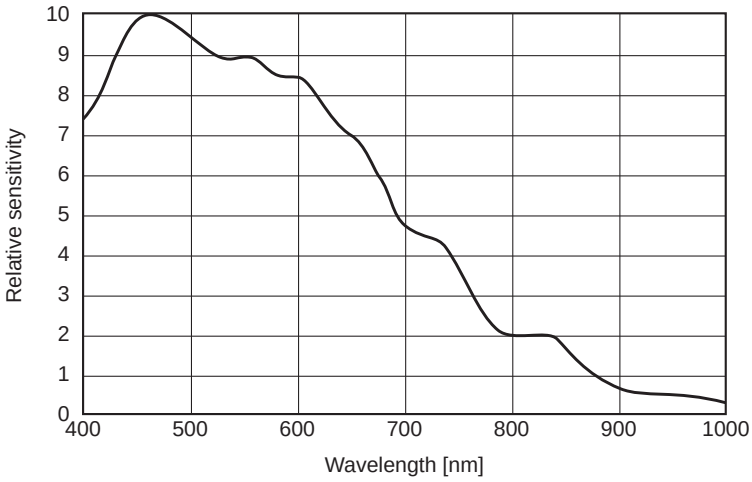
*1 This circuit diagram is the case when output circuit gain is low.

*2 Connect T1 (Pin 13) to GND with 1000pF capacitor.

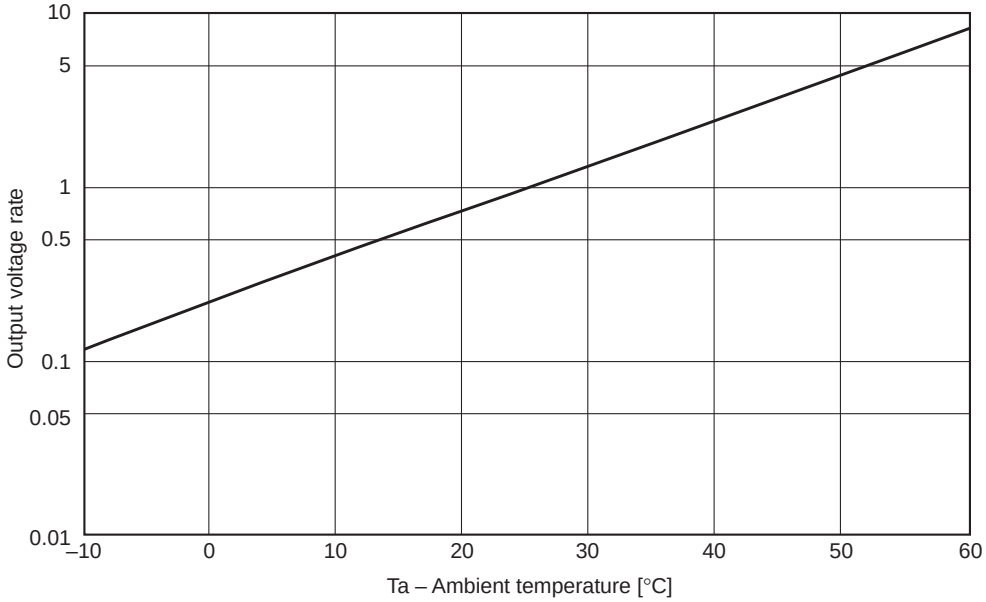
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 5V, Ta = 25°C)

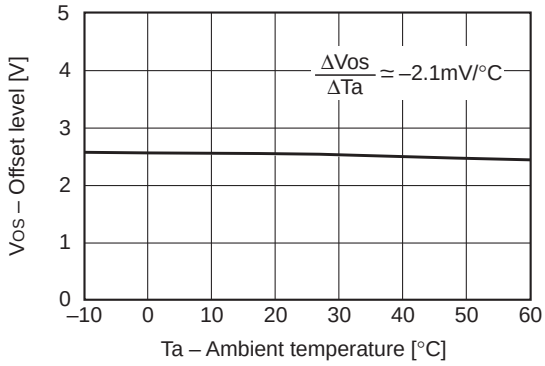
Spectral sensitivity characteristics (Standard characteristics)



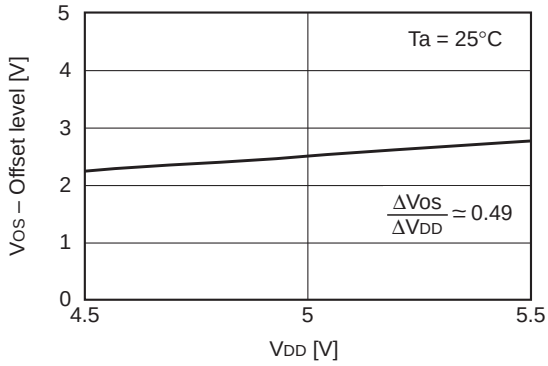
Output voltage vs. Temperature characteristics (Standard characteristics)



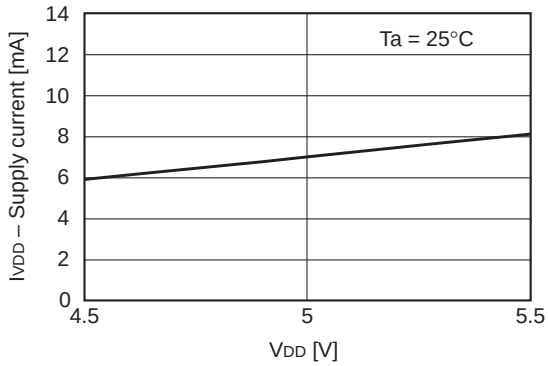
Offset level vs. Temperature characteristics (Standard characteristics)



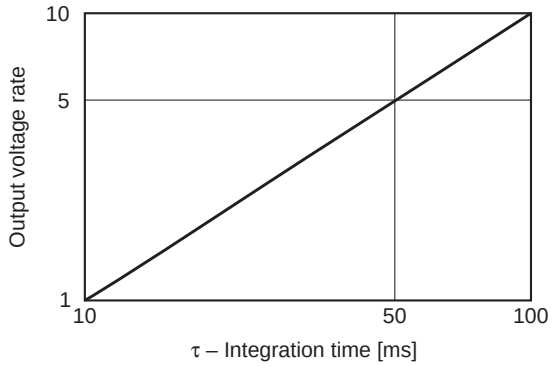
Offset level vs. V_{DD} characteristics (Standard characteristics)



Supply current vs. V_{DD} characteristics (Standard characteristics)



Output voltage vs. Integration time (Standard characteristics)



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-SIP Packages

The following points should be observed when handling and installing cer-SIP packages.

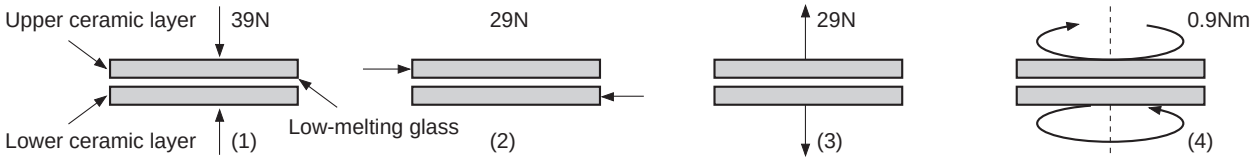
a) Remain within the following limits when applying static load to the ceramic portion of the package:

(1) Compressive strength: 39N/surface (Do not apply load more than 0.5mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with a soldering iron.

(3) Rapid cooling or heating.

(4) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

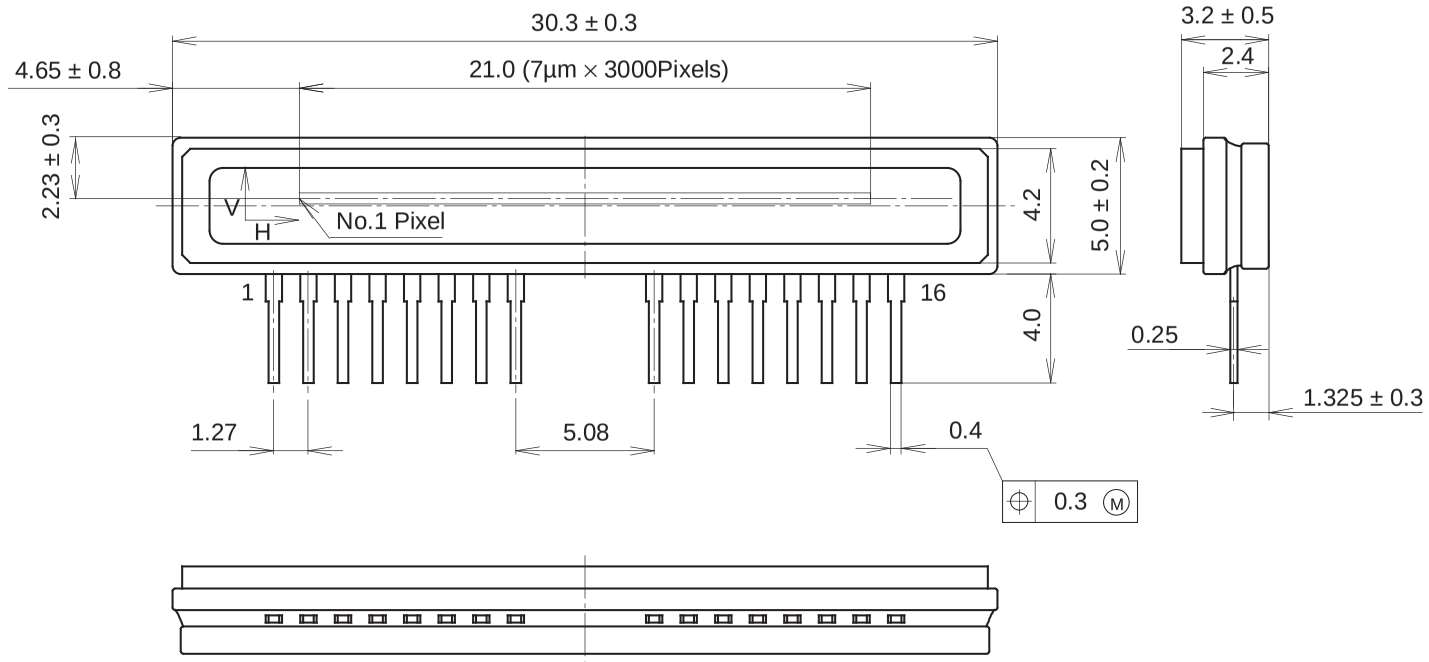
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

7) Normal output signal is not obtained immediately after device switch on.

Package Outline Unit: mm

16pin SIP



1. The height from the bottom to the sensor surface is 1.6 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-SIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.3g
DRAWING NUMBER	LS-D4(E)