SONY

ILX115LA

5000-pixel × 3 line CCD Linear Sensor (Color)

Description

The ILX115LA is a reduction type CCD linear sensor developed for color DPPC. This sensor reads A3-size documents at a density of 400 DPI (Dot Per Inch).

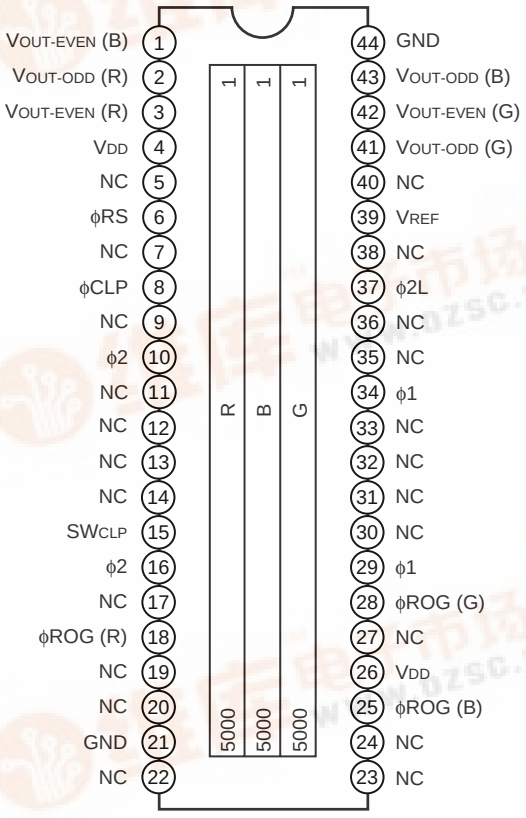
Features

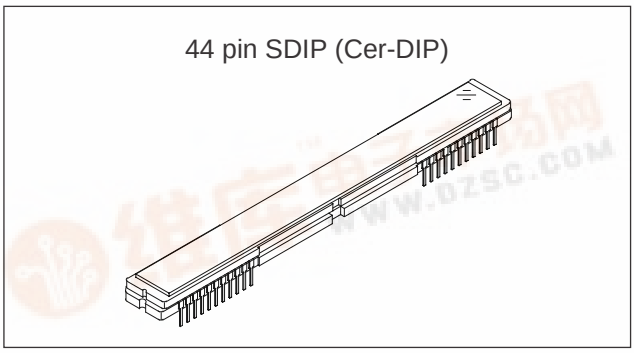
- Number of effective pixels: 15000 pixels (5000 pixels × 3)
- Pixel size: 14µm × 14µm (14µm pitch)
- Distance between line: 84µm (6 lines)
- Maximum data rate: 30MHz/color (20MHz/color during clamp circuit usage)
- Single 9V power supply
- Input Clock Pulse: CMOS 5V drive
- Number of output: 6 (2/color)
- Package: 44pin SDIP (400mil)

Absolute Maximum Ratings

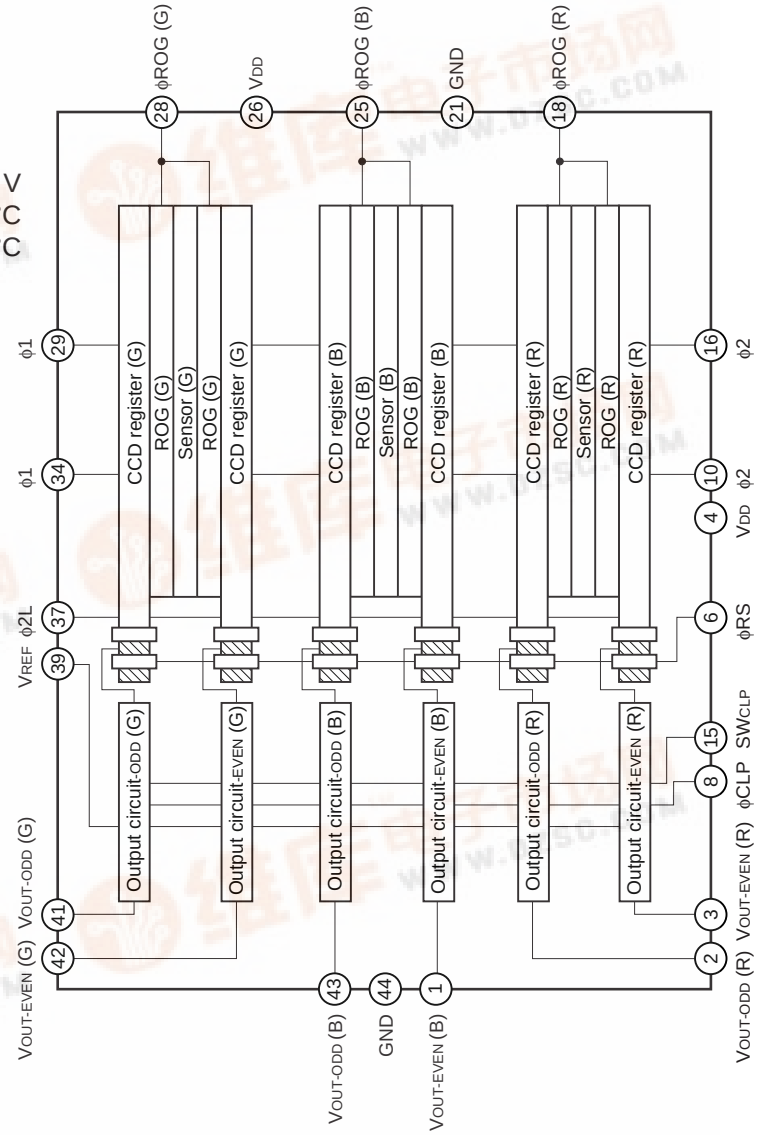
• Supply voltage	V_{DD}	11	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)





Block Diagram



E99705-PS

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V_{OUT-EVEN}$ (B)	Signal output (B)	23	NC	NC
2	$V_{OUT-ODD}$ (R)	Signal output (R)	24	NC	NC
3	$V_{OUT-EVEN}$ (R)	Signal output (R)	25	ϕROG (B)	Clock pulse input
4	V_{DD}	9V power supply	26	V_{DD}	9V power supply
5	NC	NC	27	NC	NC
6	ϕRS	Clock pulse input	28	ϕROG (G)	Clock pulse input
7	NC	NC	29	ϕ1	Clock pulse input
8	ϕCLP	Clock pulse input	30	NC	NC
9	NC	NC	31	NC	NC
10	ϕ2	Clock pulse input	32	NC	NC
11	NC	NC	33	NC	NC
12	NC	NC	34	ϕ1	Clock pulse input
13	NC	NC	35	NC	NC
14	NC	NC	36	NC	NC
15	SW_{CLP}	Clamp switch	37	ϕ2L	Clock pulse input
16	ϕ2	Clock pulse input	38	NC	NC
17	NC	NC	39	V_{REF}	Power supply (Clamp)
18	ϕROG (R)	Clock pulse input	40	NC	NC
19	NC	NC	41	$V_{OUT-ODD}$ (G)	Signal output (G)
20	NC	NC	42	$V_{OUT-EVEN}$ (G)	Signal output (G)
21	GND	GND	43	$V_{OUT-ODD}$ (B)	Signal output (B)
22	NC	NC	44	GND	GND

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	8.55	9	9.45	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕ1, ϕ2	$C_{\phi 1}$, $C_{\phi 2}$	—	1800	—	pF
Input capacity of ϕ2L	$C_{\phi 2L}$	—	60	—	pF
Input capacity of ϕRS	$C_{\phi RS}$	—	60	—	pF
Input capacity of ϕROG	$C_{\phi ROG}$	—	60	—	pF
Input capacity of ϕCLP	$C_{\phi CLP}$	—	60	—	pF

Note) Input capacity of ϕ1, ϕ2 is a value gathering respective related pins.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φ2L, φRS	fφ1, fφ2, fφ2L, fφRS	—	1	15	MHz
φCLP	fφCLP	—	1	10	MHz

Input Clock Pulse Voltage

Item		Min.	Typ.	Max.	Unit
φ1, φ2, φ2L, φRS, φROG, φCLP pulse voltage	High level	4.75	5.0	5.25	V
	Low level	–0.3	0	0.1	V

Mode Description

	Pin condition	
	8pin φCLP	15pin SWCLP
Clamp circuit not used	VDD	GND
Clamp circuit used	φCLP	VDD

Electrooptical Characteristics (Note 1)

Ta = 25°C, V_{DD} = 9V, $f\phi_{RS}$ = 1MHz, Input clock = 5Vp-p, Clamp circuit used,
Light source = 3200K, IR cut filter: CM-500S (t = 1.0mm)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	5.10	6.80	8.50	V/(lx · s)	Note 2
	Green	R_G	5.17	6.89	8.61		
	Blue	R_B	5.48	7.30	9.13		
Sensitivity nonuniformity		PRNU	—	5	15	%	Note 3
Saturation output voltage		V_{SAT}	1.5	1.8	—	V	
Saturation exposure	Red	SE_R	0.18	0.26	—	lx · s	Note 4
	Green	SE_G	0.18	0.26	—		
	Blue	SE_B	0.16	0.25	—		
Dark voltage average		V_{DRK}	—	1.5	3	mV	Note 5
Dark signal nonuniformity		DSNU	—	1.5	5	mV	
Image lag		IL	—	0.02	—	%	Note 6
Supply current		I_{VDD}	—	45	60	mA	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	185	—	Ω	—
Offset level		V_{OS}	—	4.4	—	V	Note 7

Notes

1) In accordance with the given electrooptical characteristics, the even black level is defined as the average value of D24, D26 to D72. The odd black level is defined as average value of D23, D25 to D71.
2) For the sensitivity test light is applied with a uniform intensity of illumination.
3) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

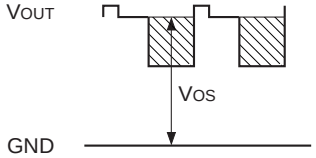
   V_{OUT} = 500mV

   $$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

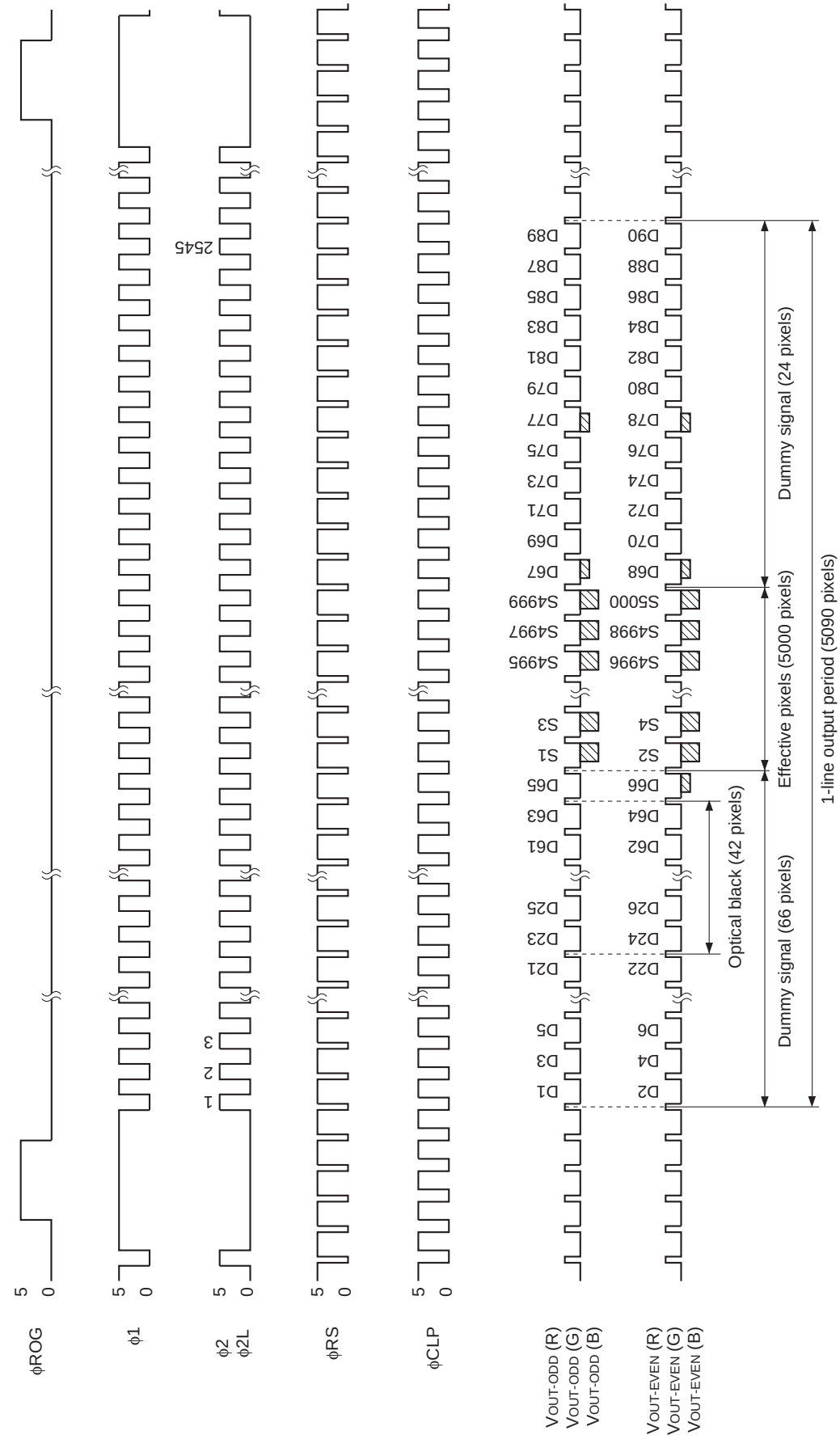
   Where the 5000 pixels are divided into blocks of 100, even and odd pixels, respectively the maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
4) Saturation exposure is defined as follows.

   $$SE = V_{SAT}/R\ [lx \cdot s]$$

5) Optical signal accumulated time τint stands at 10ms.
6) V_{OUT} (B)= 500mV (typ.)
7) Vos is defined as indicated below.
   V_{OUT} indicates $V_{OUT-ODD}$ (R), $V_{OUT-EVEN}$ (R), $V_{OUT-ODD}$ (G), $V_{OUT-EVEN}$ (G), $V_{OUT-ODD}$ (B), $V_{OUT-EVEN}$ (B).

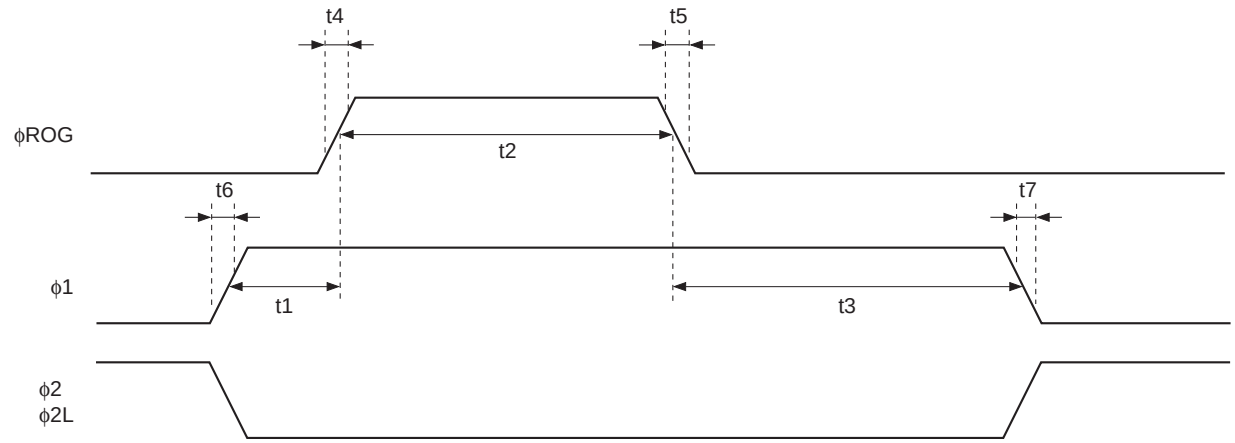


Clock Timing Chart 1[*1]

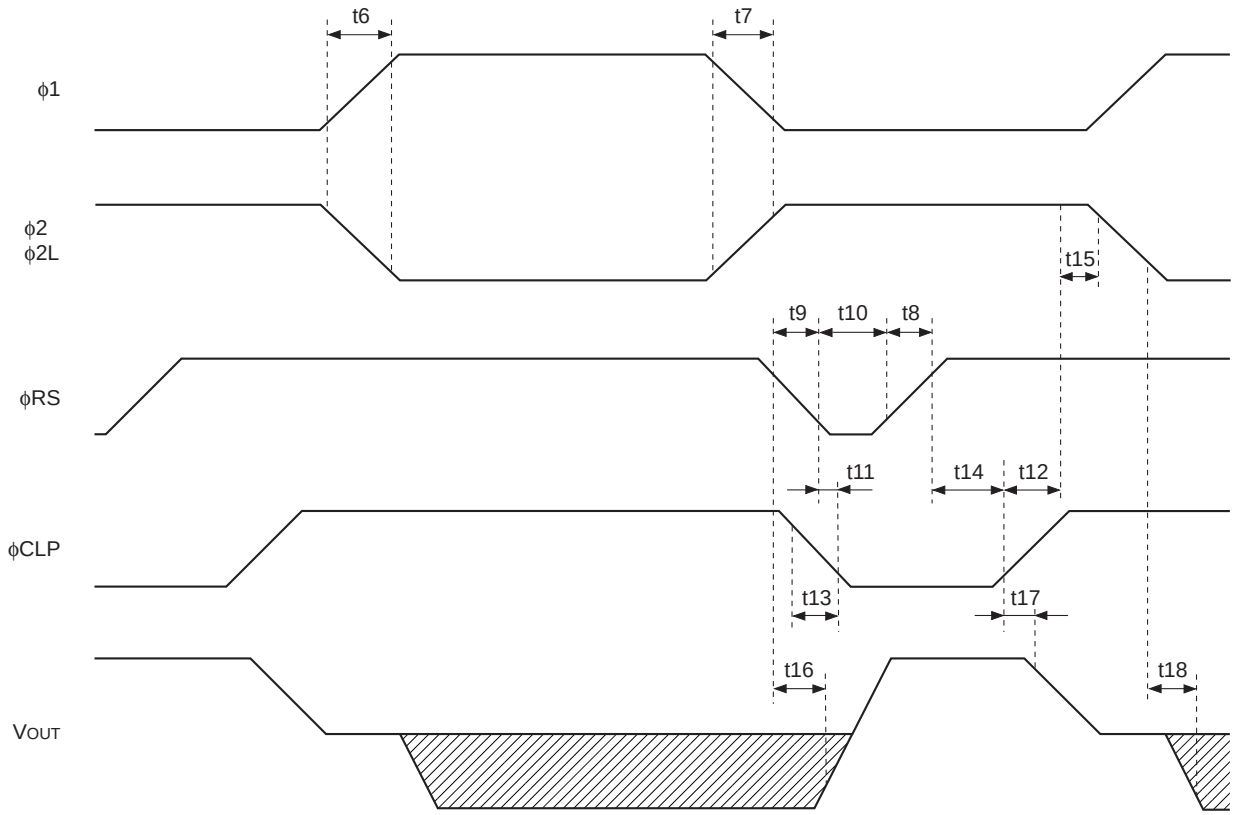


[*1] The transfer pulses (φ1, φ2, φ3) must have more than 2545 cycles.

Clock Timing Chart 2

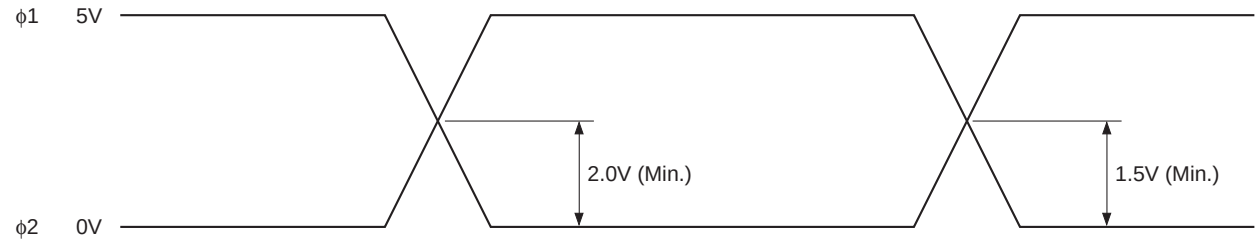


Clock Timing Chart 3

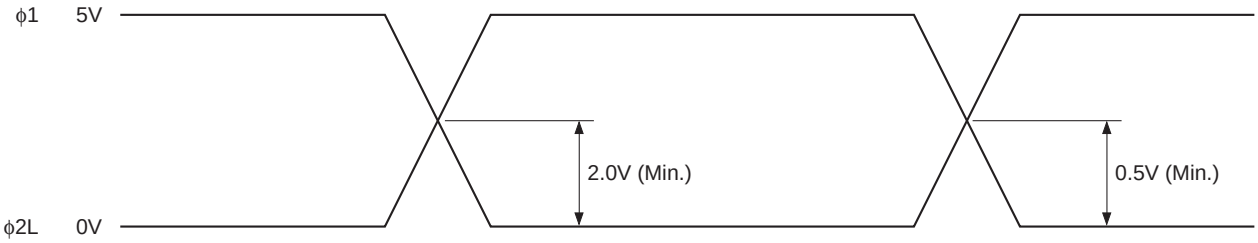


Clock Timing Chart 4

Cross point φ1 and φ2



Cross point φ1 and φ2L

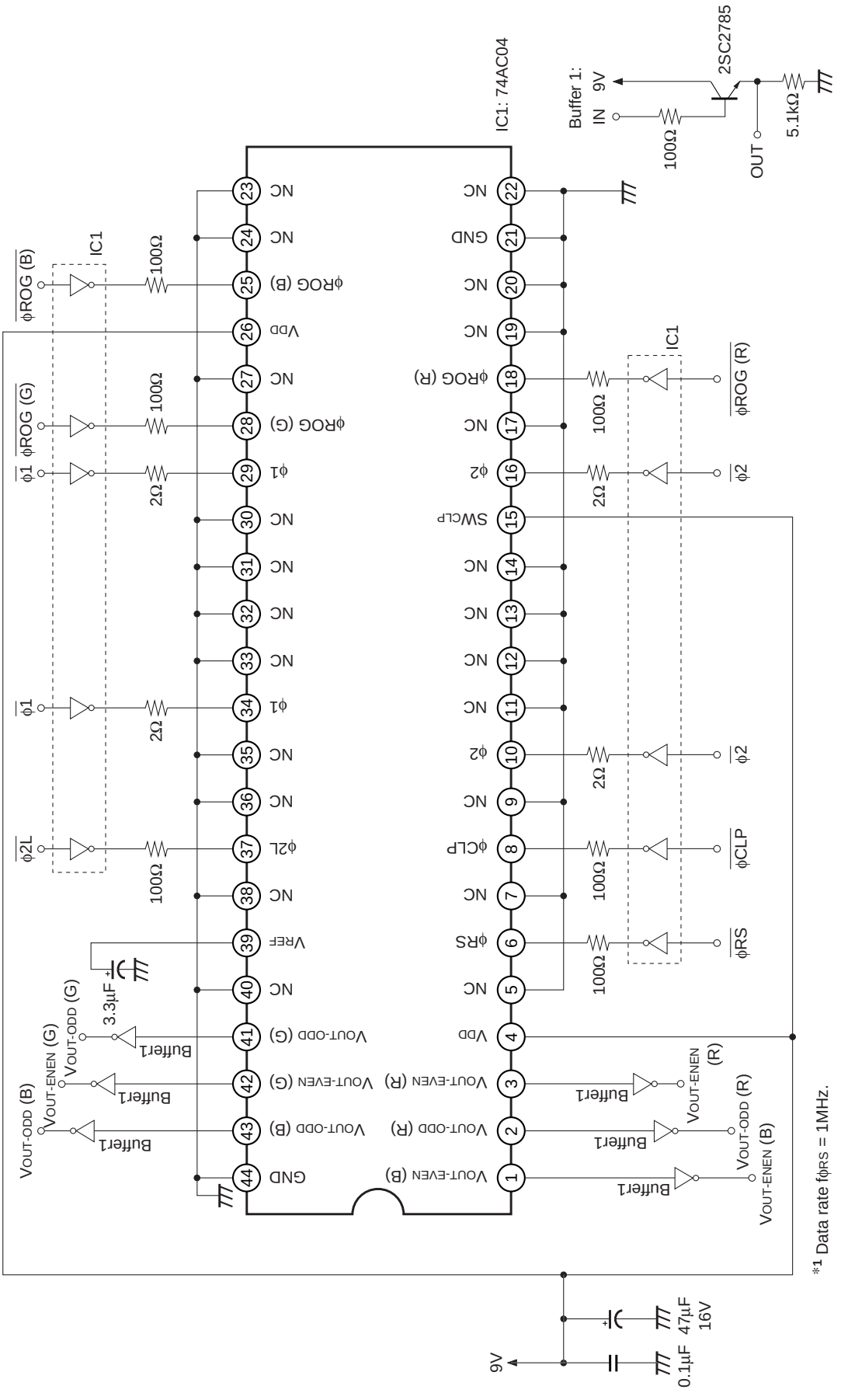


Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φ1 pulse timing	t1	50	100	—	ns
φROG pulse high level period	t2	600	1000	—	ns
φROG, φ1 pulse timing	t3	400	1000	—	ns
φROG pulse rise time	t4	0	10	100	ns
φROG pulse fall time	t5	0	10	100	ns
φ1 pulse fall time /φ2 pulse rise time	t6	0	5	10	ns
φ1 pulse rise time /φ2 pulse fall time	t7	0	5	10	ns
φRS pulse rise time	t8	0	5	10	ns
φRS pulse fall time	t9	0	5	10	ns
φRS pulse low level period	t10	8	200*1	—	ns
φRS, φCLP pulse timing 1	t11	0	50*1	—	ns
φCLP pulse rise time	t12	0	5	10	ns
φCLP pulse fall time	t13	0	5	10	ns
φRS, φCLP pulse timing 2	t14	16	200*1	—	ns
φCLP φ2L pulse timing	t15	0	70*1	—	ns
Signal output delay time for φRS	t16	—	12	—	ns
Signal output delay time for φCLP	t17	—	4	—	ns
Signal output delay time for φ2L	t18	—	12	—	ns

*1 These timing is the recommended condition under $f_{\phi RS} = f_{\phi CLP}$ = 1MHz.

Application Circuit*1

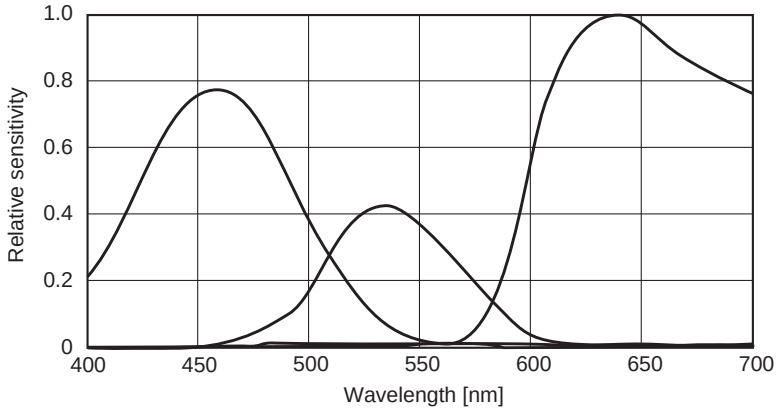


*1 Data rate fφRS = 1MHz.

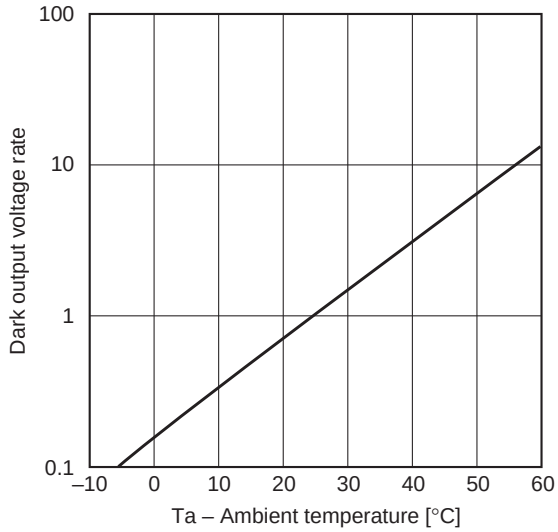
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 9V, Ta = 25°C)

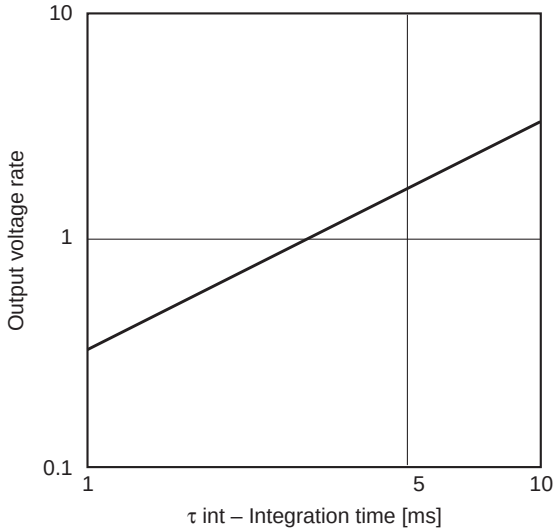
Spectral sensitivity characteristics (Standard characteristics)



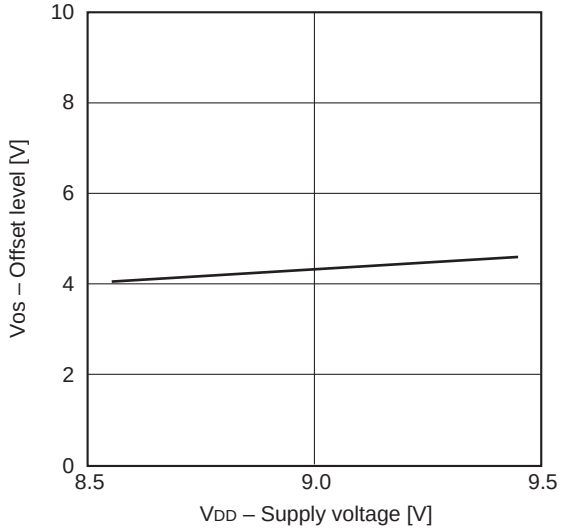
Dark output voltage rate vs. Ambient temperature (Standard characteristics)



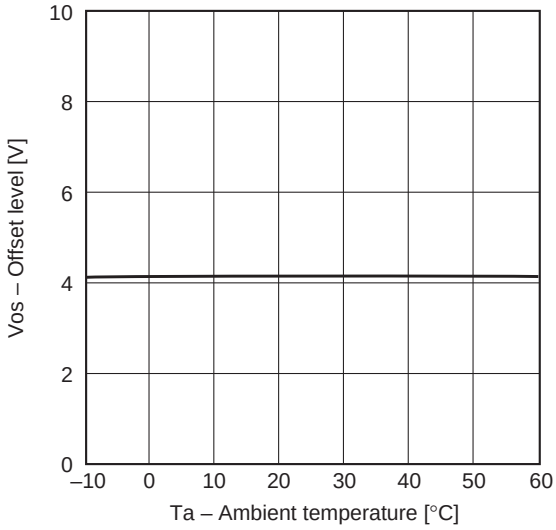
Output voltage rate vs. Integration time (Standard characteristics)



Offset level vs. Supply voltage (Standard characteristics)



Offset level vs. Ambient temperature (Standard characteristics)



Notes of Handling

1) Static charge prevention

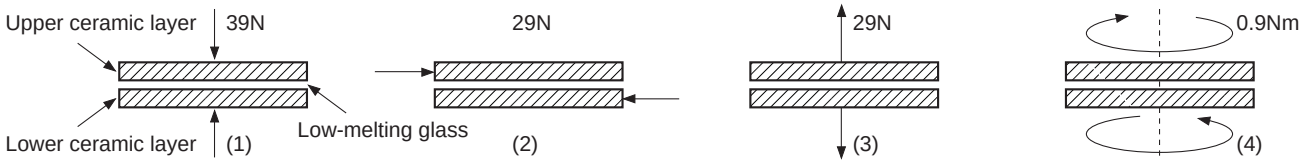
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

a) Remain within the following limits when applying a static load to the ceramic portion of the package:
   (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
   (2) Shearing strength: 29N/surface
   (3) Tensile strength: 29N/surface
   (4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,
   (1) Applying repetitive bending stress to the external leads.
   (2) Applying heat to the external leads for an extended period of time with a soldering iron.
   (3) Rapid cooling or heating.
   (4) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
   (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

   Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

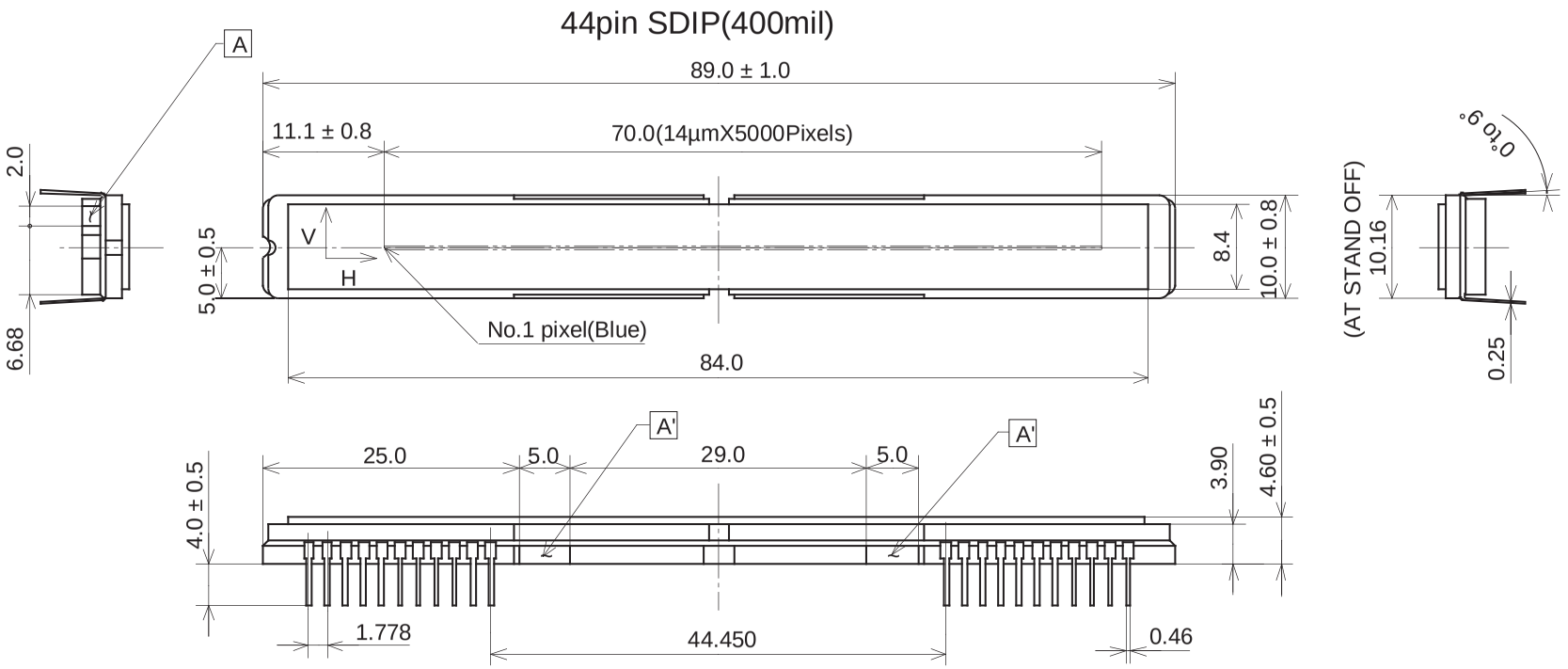
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm



1. The point **"A"** of the package is the horizontal reference.
   The two points **"A'"** of the package are the vertical reference.
2. The height from the bottom to the sensor surface is 2.4 ± 0.3m.
3. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.
4. The notch of the package must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	11.5g
DRAWING NUMBER	LS-B15-01(E)