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SONY

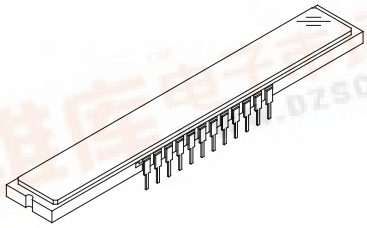
# ILX508A

## 7926-pixel CCD Linear Image Sensor (B/W)

### Description

The ILX508A is a reduction type CCD linear sensor developed for high resolution copiers. This sensor reads A3-size documents at a density of 600 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use. In addition reset pulse can switch between internal generation and external input.

24 pin DIP (Ceramic)



### Features

- Number of effective pixels: 7926 pixels
- Pixel size: 7µm × 7µm (7µm pitch)
- Built-in timing generator and clock-drivers
- Ultra high sensitivity
- Ultra low lag/low dark voltage
- Output method
- Maximum operating frequency: 12.5MHz

### Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD1}$ | 11 | V |
| | $V_{DD2}$ | 6 | V |
| • Operation temperature | | –10 to +60 | °C |
| • Storage temperature | | –30 to +80 | °C |

**Pin Configuration** (Top View)

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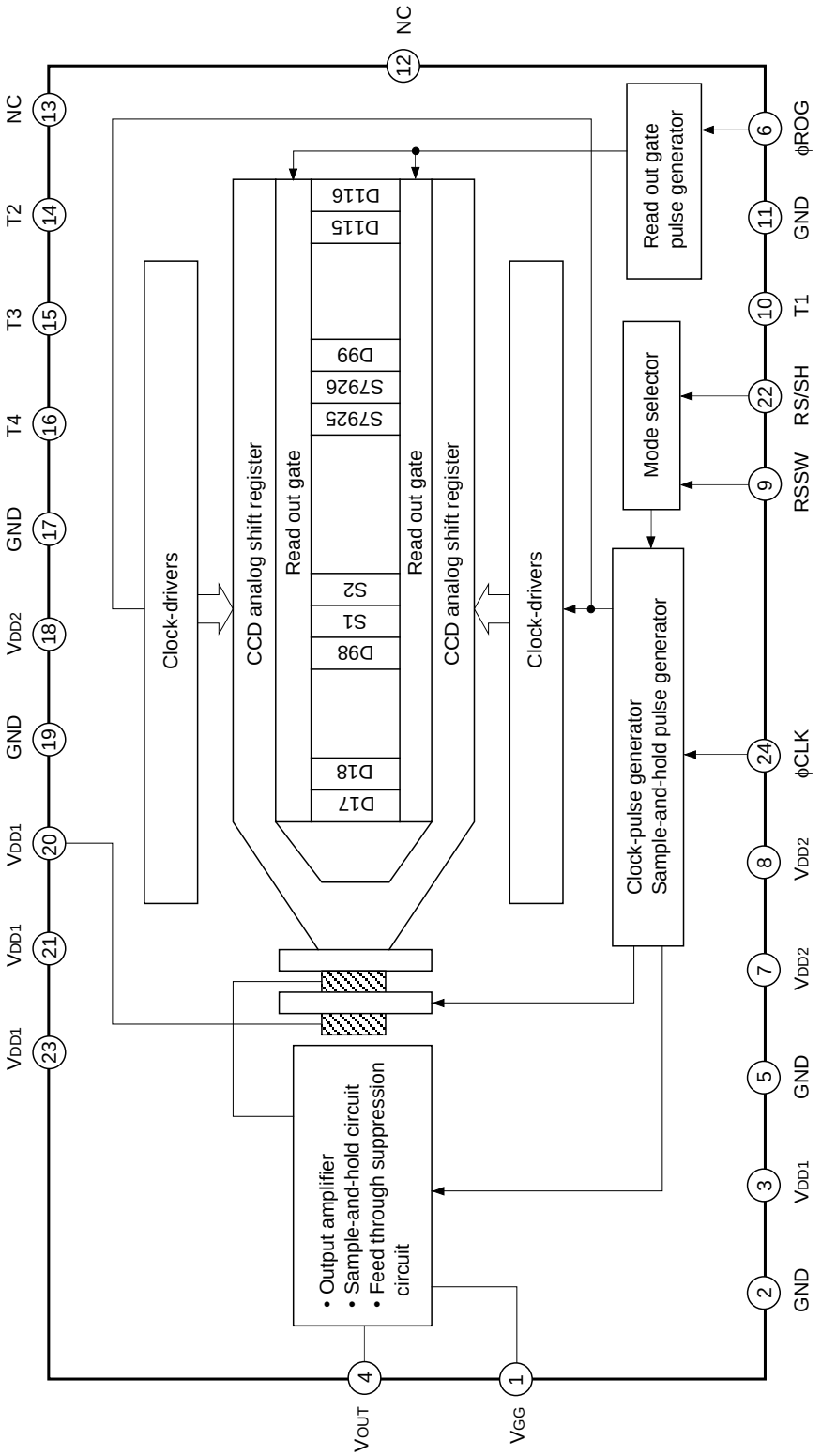
## Block Diagram



**Pin Description**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | $V_{GG}$ | Output circuit gate bias |
| 2 | GND | GND |
| 3 | $V_{DD1}$ | 9V power supply |
| 4 | $V_{OUT}$ | Signal output |
| 5 | GND | GND |
| 6 | $\phi$ROG | Clock pulse |
| 7 | $V_{DD2}$ | 5V power supply |
| 8 | $V_{DD2}$ | 5V power supply |
| 9 | RSSW* | RS pulse external, internal selection (External RS $\rightarrow$ $V_{DD1}$, Internal RS $\rightarrow$ GND) |
| 10 | T1 | Test pin (5V) |
| 11 | GND | GND |
| 12 | NC | NC |
| 13 | NC | NC |
| 14 | T2 | Test pin (GND) |
| 15 | T3 | Test pin (5V) |
| 16 | T4 | Test pin (GND) |
| 17 | GND | GND |
| 18 | $V_{DD2}$ | 5V power supply |
| 19 | GND | GND |
| 20 | $V_{DD1}$ | 9V power supply |
| 21 | $V_{DD1}$ | 9V power supply |
| 22 | RS/SH* | Clock pulse or S/H switch |
| 23 | $V_{DD1}$ | 9V power supply |
| 24 | $\phi$CLK | Clock pulse |

* Output mode is changeable as follows.

| 9pin \ 22pin | GND | $V_{DD1}$ | $\phi$RS |
|---|---|---|---|
| GND | Internal RS without S/H | Internal RS with S/H | — |
| $V_{DD1}$ | — | — | External RS without S/H |

**Recommended Voltage**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD1}$ | 8.5 | 9.0 | 9.5 | V |
| $V_{DD2}$ | 4.75 | 5.0 | 5.25 | V |

**Note)** Rules for raising and lowering power supply voltage.
To raise power supply voltage, first raise $V_{DD1}$ (9V) and then $V_{DD2}$ (5V).
To lower voltage, first lower $V_{DD2}$ (5V) and then $V_{DD1}$ (9V).

**Clock Characteristics**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input capacity of φCLK | CφCLK | — | 10 | — | pF |
| Input capacity of φROG | CφROG | — | 10 | — | pF |
| Input capacity of RS/SH | C RS/SH | — | 10 | — | pF |
| φCLK frequency | fφCLK | — | 1 | 12.5 | MHz |
| φRS frequency | fφRS | — | 1 | 12.5 | MHz |

**Electrooptical Characteristics**[*1]

(Ta = 25°C, $V_{DD1}$ = 9V, $V_{DD2}$ = 5V, Light source = 3200K, $\phi$CLK = 1MHz, Internal $\phi$RS mode without S/H, IR cut filter, CM-500S (t = 1.0mm))

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Sensitivity1 | R1 | 7.5 | 10.8 | 13.9 | V/(lx · s) | *2 |
| Sensitivity2 | R2 | — | 24.6 | — | V/(lx · s) | *3 |
| Sensitivity nonuniformity | PRNU | — | 5 | 12.5 | % | *4 |
| Saturation output voltage | $V_{SAT}$ | 1.0 | 1.5 | — | V | *5 |
| Saturation exposure | SE | 0.072 | 0.139 | — | lx · s | *6 |
| Even and odd black level DC difference | $\Delta V$ | — | 1.0 | 10.0 | mV | *7 |
| Dark voltage average | $V_{DRK}$ | — | 0.3 | 2 | mV | *8 |
| Dark signal nonuniformity | DSNU | — | 0.6 | 5 | mV | *9 |
| Image lag | IL | — | 0.02 | — | % | *10 |
| 9V supply current | $I_{VDD1}$ | — | 16 | 32 | mA | — |
| 5V supply current | $I_{VDD2}$ | — | 5 | 16 | mA | — |
| Total transfer efficiency | TTE | 90 | 97 | — | % | — |
| Output impedance | $Z_O$ | — | 600 | — | Ω | — |
| Offset level | $V_{OS}$ | — | 3.0 | — | V | *11 |
| Dynamic range | DR | 500 | 5000 | — | — | *12 |

*1 In accorcance with the given electrooptical characteristics, the even black level is defined as the mean value of D8, D10, D12, D14, and D16.

*2 For the sensitivity test light is applied with a uniform intensity of illumination.

*3 W lamp (2854K).

*4 PRNU is defined as indicated below. Ray incidence conditions are the same as for *2.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

Where the 7926 pixels are divided into blocks of 102, even and odd pixels, respectively (Even and odd last blocks are 87.) The maximum output of each block is set to $V_{MAX}$, the minimum output to $V_{MIN}$ and the average output to $V_{AVE}$.

*5 Use below the minimum value of the saturation output voltage.

*6 Saturation exposure is defined as follows.

$$SE = \frac{V_{SAT}}{R1}$$

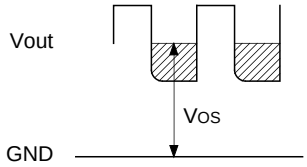
*7 Indicates the DC difference in value between odd black level and even black level.

*8 optical signal accumulated time $\tau$ int stands at 10ms.

*9 The difference between the maximum and mean values of the dark output voltage is calculated for even and odd respectively. The larger value is defined as the dark signal nonuniformity.
Optical signal accumulated time $\tau$ int stands at 10ms.

*10 $V_{OUT}$ = 500mV (Typ.)

*11 $V_{OS}$ is defined as indicated below.

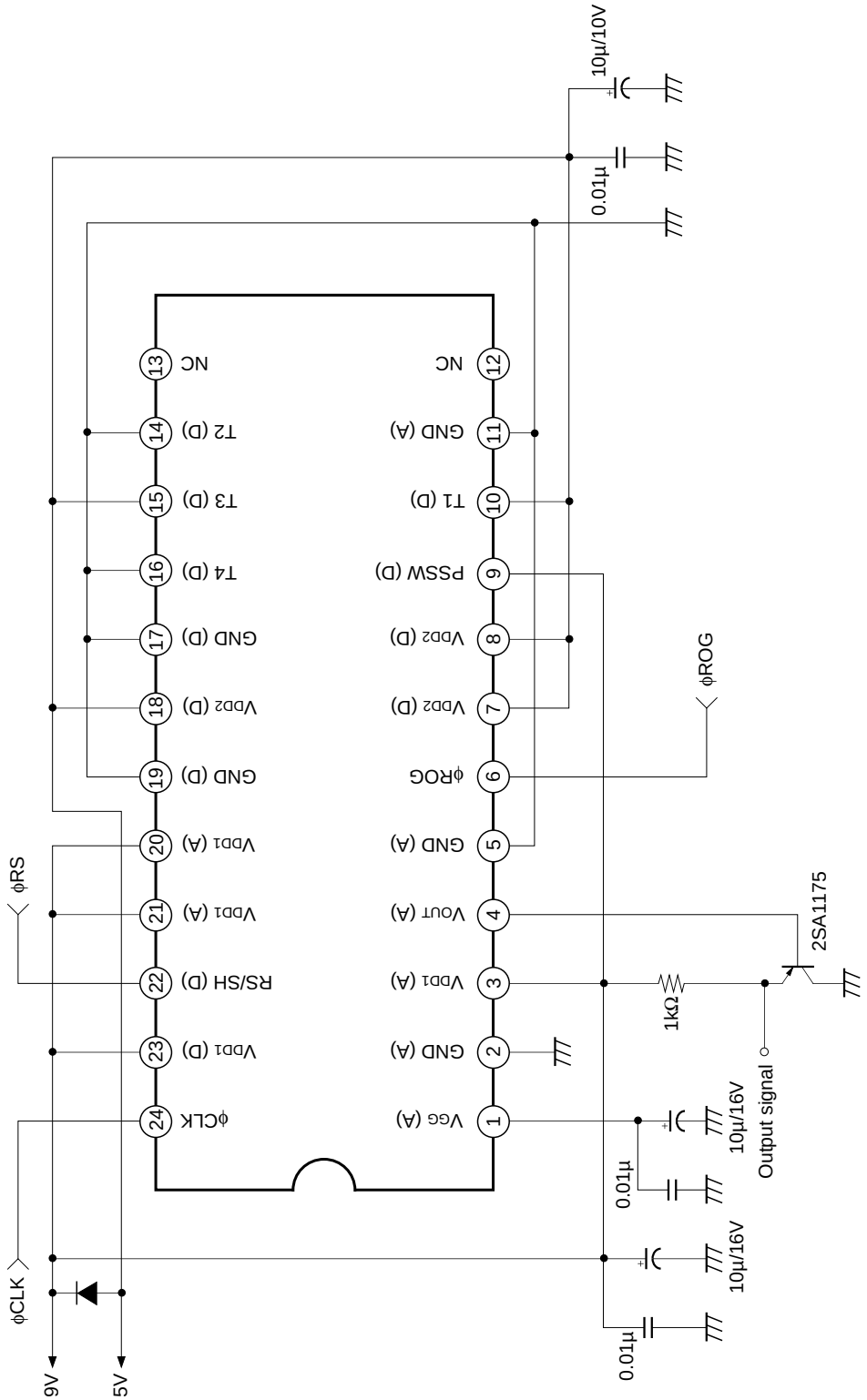



*12 Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.

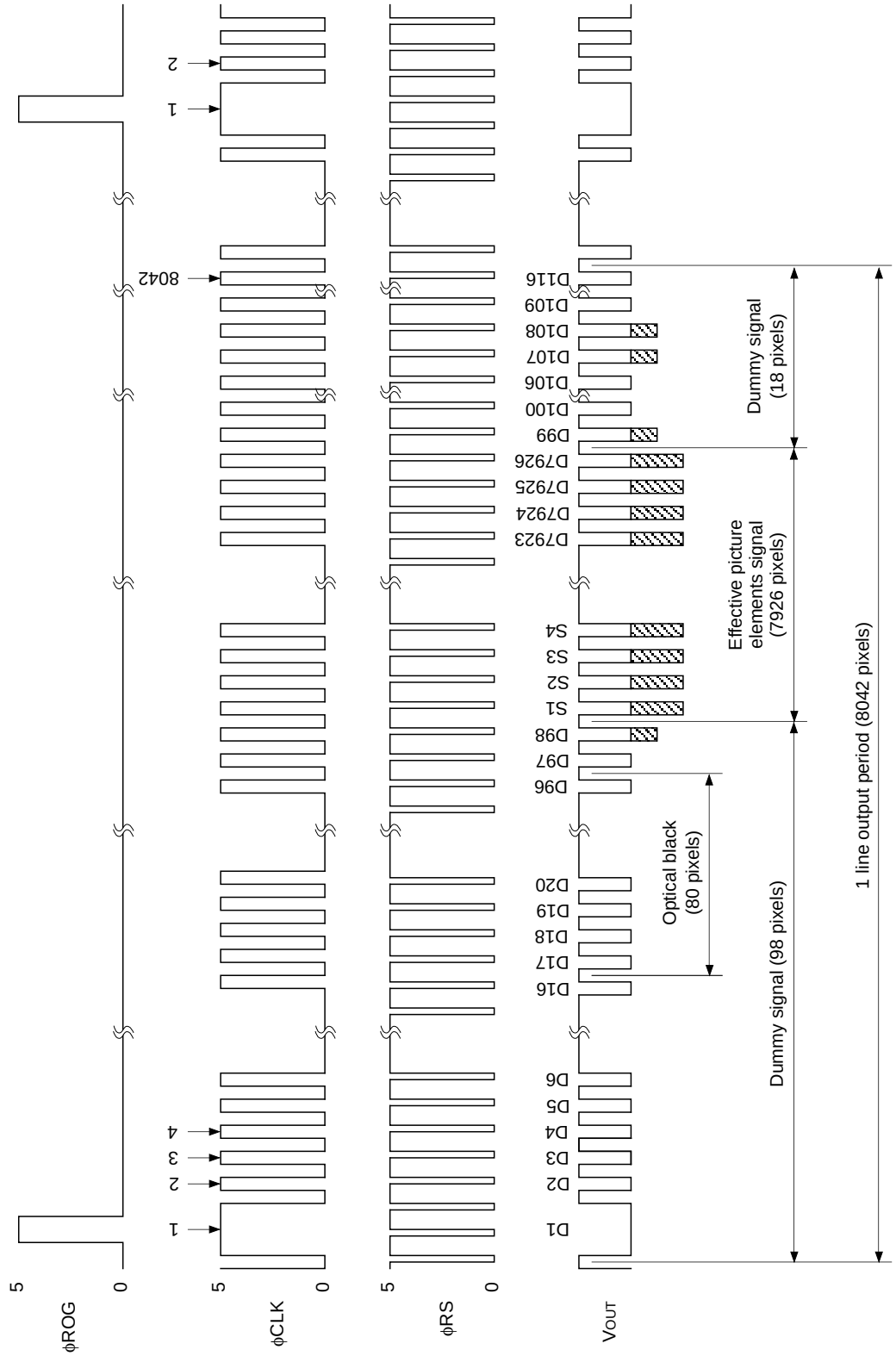
**Application Circuit** (External φRS)




* When noise influence into output signal is large, connect pins indicated by (A) to the analog power supply and pins indicated by (D) to the digital power supply, and also use a decoupling capacitor of large capacitance.

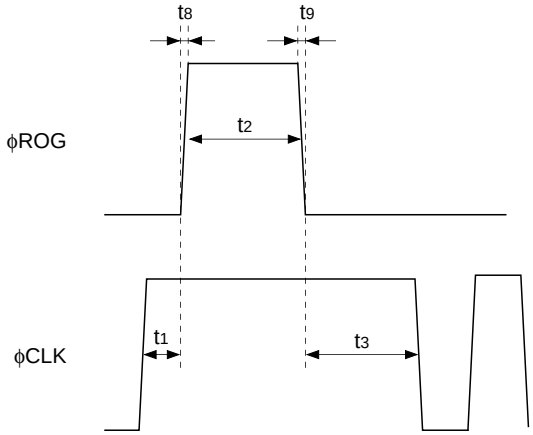
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Clock Timing Diagram** (External ϕRS)

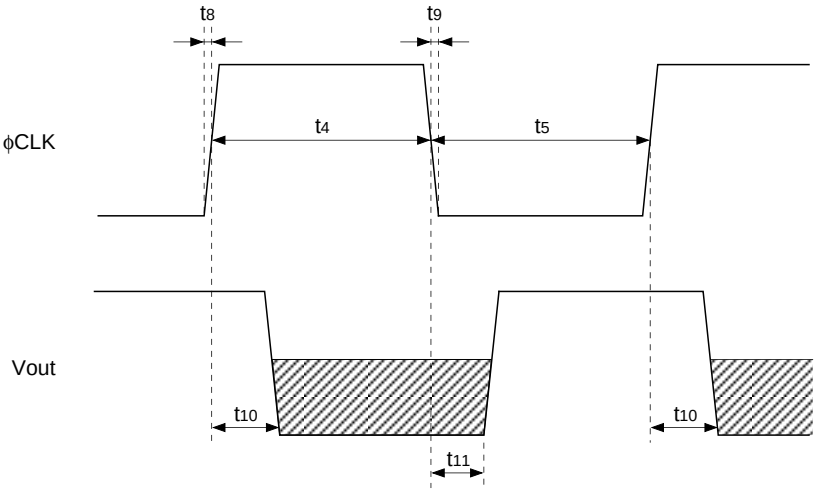


## Clock pulse Waveform Conditions

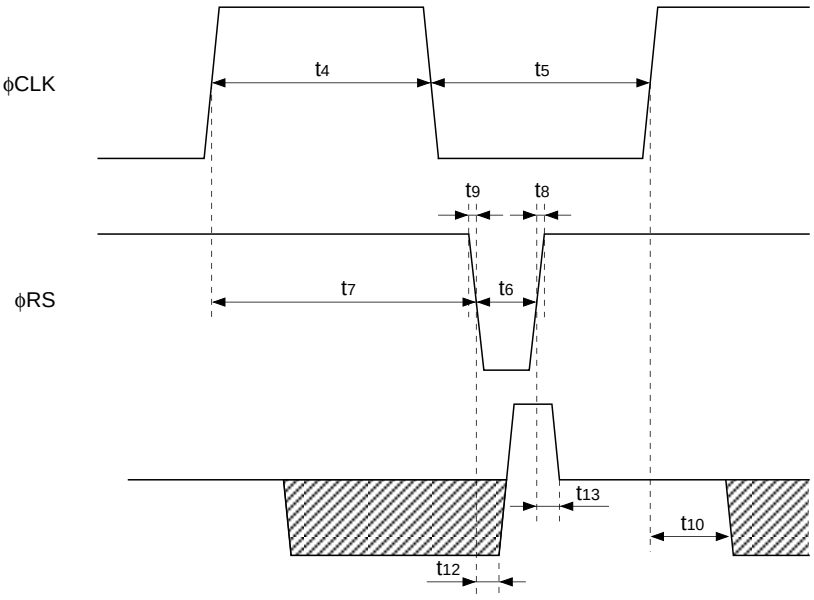
### φCLK, φROG pulse related




### Internal φRS mode




### External φRS mode

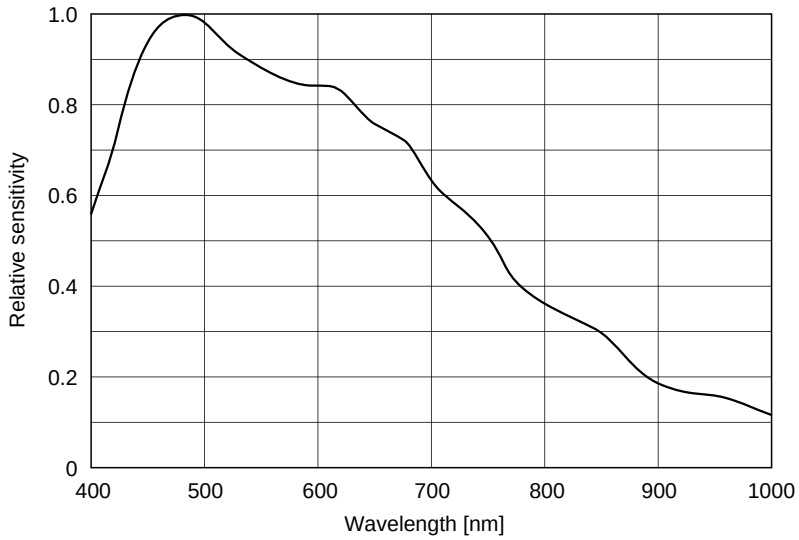


| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| φROG, φCLK pulse timing | | $t_1$ | 200 | 300 | — | ns |
| φROG, φCLK pulse timing | | $t_3$ | 1200 | 1500 | — | ns |
| φROG pulse high level period | | $t_2$ | 1200 | 1500 | — | ns |
| φCLK pulse high level period | | $t_4$ | 40 | 500*1 | — | ns |
| φCLK pulse low level period | | $t_5$ | 40 | 500*1 | — | ns |
| φRS pulse low level period | | $t_6$ | 25 | 100*1 | — | ns |
| φCLK, φRS pulse timing | | $t_7$ | 60 | 550*1 | $10 + t_4 + t_5$ | ns |
| Input clock pulse rise/fall time | | $t_8$, $t_9$ | — | 5 | 10 | ns |
| Input clock pulse voltage | High level | VφCLK, VφROG | 4.5 | 5.0 | 5.5 | V |
| | Low level | VφRS | 0 | — | 0.5 | V |
| Signal output delay time | Internal φRS | $t_{10}$ | — | 95 | — | ns |
| | | $t_{11}$ | — | 70 | — | ns |
| | External φRS | $t_{12}$ | — | 45 | — | ns |
| | | $t_{13}$ | — | 60 | — | ns |

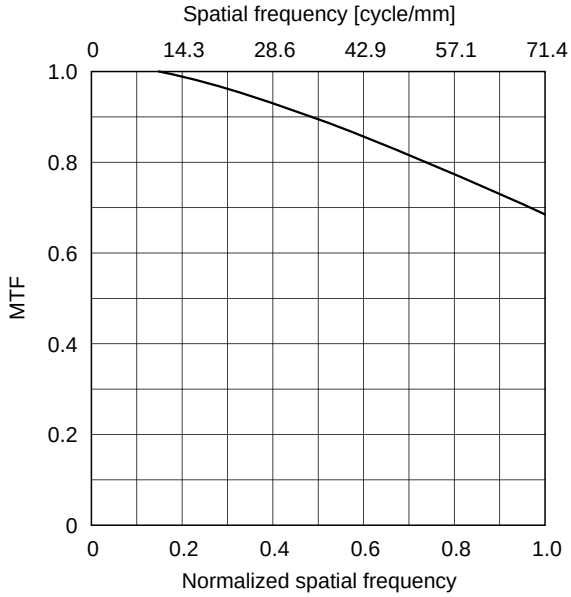
*1 The frequency of φCLK is 1MHz.

**Example of Representative Characteristics** ($V_{DD1}$ = 9V, $V_{DD2}$ = 5V, Ta = 25°C)

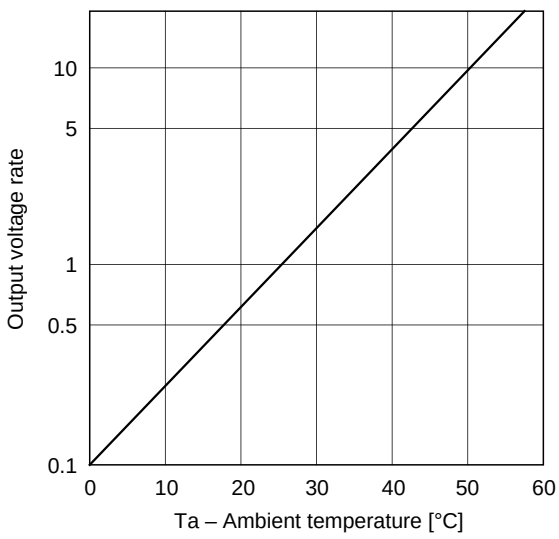
**Spectral sensitivity characteristics (Standard characteristics)**



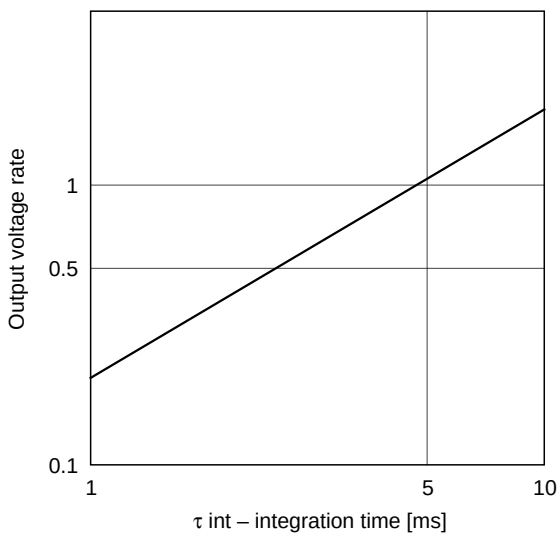

**MTF of main scanning direction (Standard characteristics)**



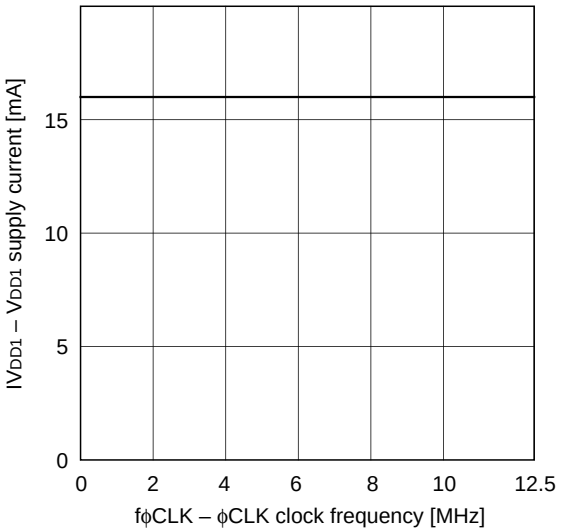

**Dark signal output temperature characteristics (Typical characteristics)**



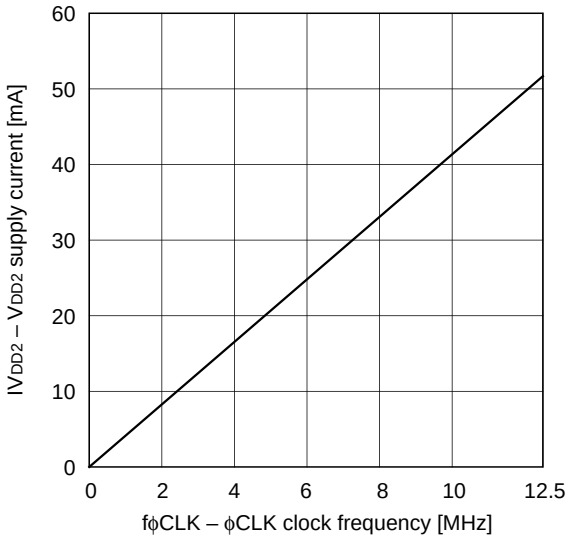

**Integration time output voltage characteristics (Typical characteristics)**



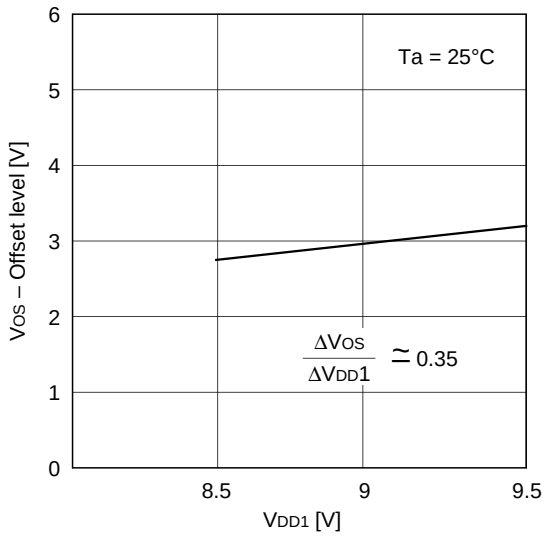
**Operational frequency characteristics of the $V_{DD1}$ supply current (Typical characteristics)**



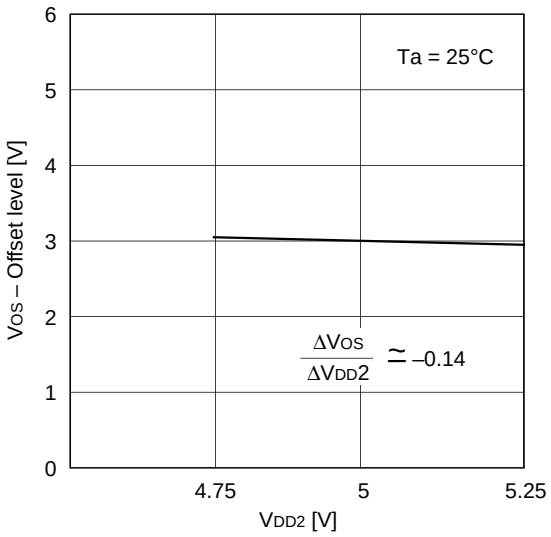

**Operational frequency characteristics of the $V_{DD2}$ supply current (Typical characteristics)**



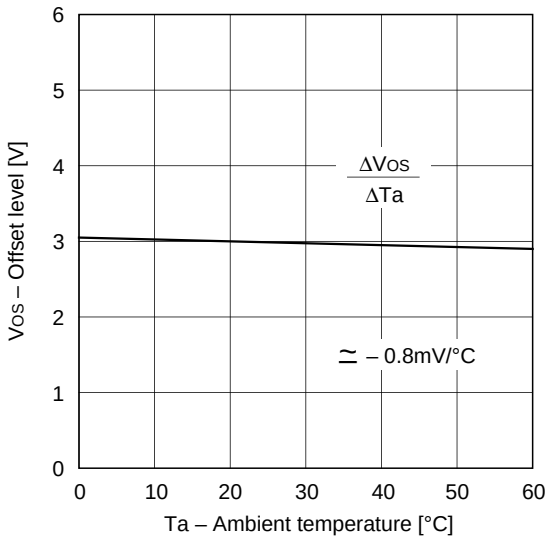

**Offset level vs. $V_{DD1}$ characteristics (Typical characteristics)**




**Offset level vs. $V_{DD2}$ characteristics (Typical characteristics)**




**Offset level vs. Temperature characteristics (Typical characteristics)**



**Notes on Handling**

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Regulation for raising and lowering the power supply voltage.
   When raising the supply voltage, first raise $V_{DD1}$ (9V) and then $V_{DD2}$ (5V).
   Similarly, lower $V_{DD2}$ (5V) first and then $V_{DD1}$ (9V).

3) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficienty.
   c) To dismount an imaging device do not use a solder suction equipment.
      When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

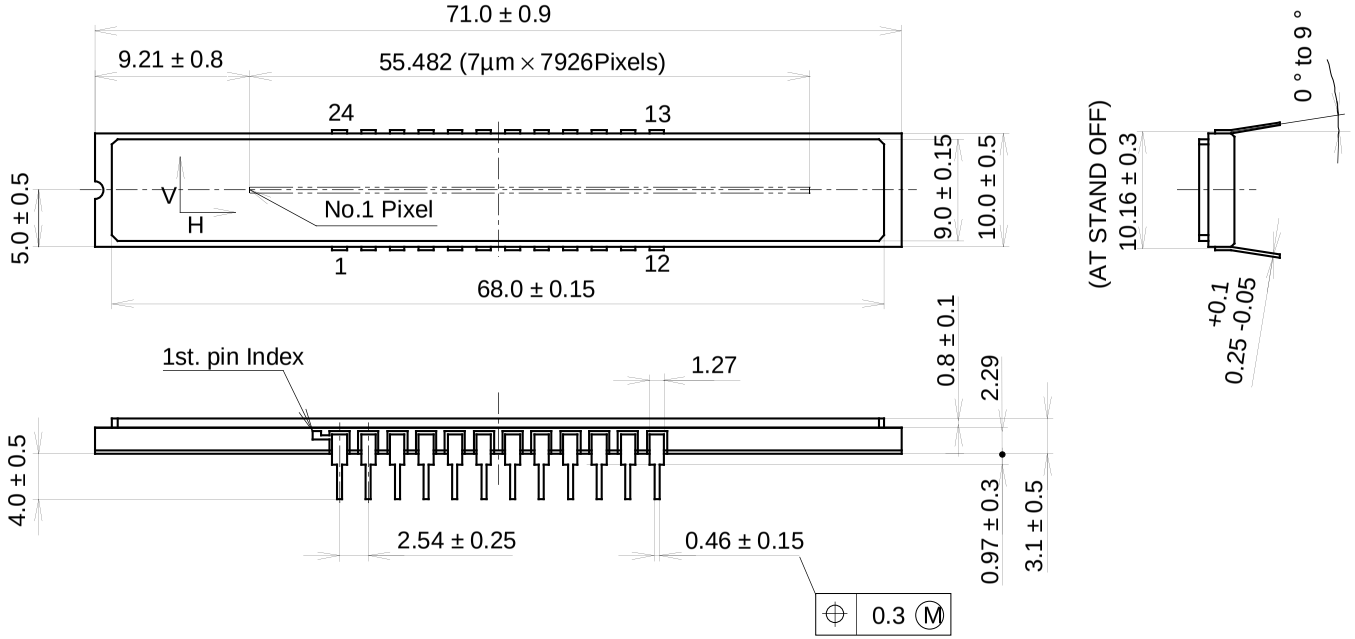
4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained.
      Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humity will affect the characteristics.
   Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

**Package Outline** Unit: mm

## 24Pin DIP (400mil)




1. The height from the bottom to the sensor surface is 1.42 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

## PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | Ceramic |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | 42ALLOY |
| PACKAGE WEIGHT | 5.8g |