SONY

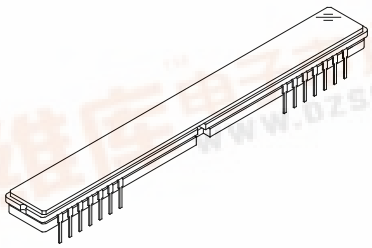
ILX532A

7500-pixel CCD Linear Sensor (B/W)

Description

The ILX532A is a reduction type CCD linear sensor developed for high resolution copiers. This sensor reads A3-size documents at a density of 600DPI, at high speed.

28 pin DIP (Cer-DIP)



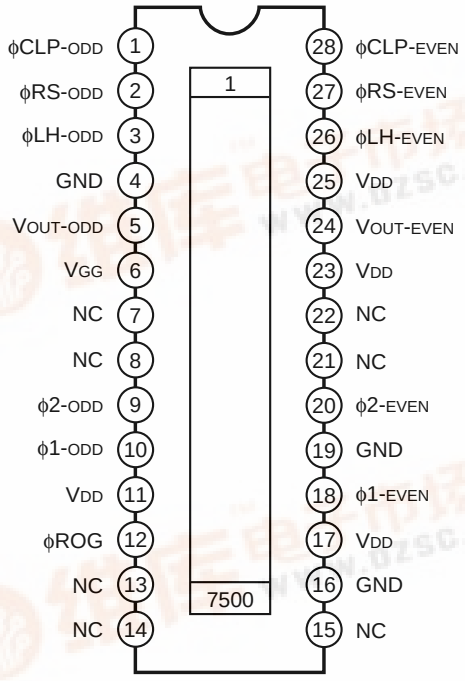
Features

- Number of effective pixels: 7500 pixels
- Pixel size: 7µm × 7µm (7µm pitch)
- Clamp circuit are on-chip
- Signal output phase of two-output simultaneous-output (alternate-output is available)
- Ultra high sensitivity/Ultra low lag
- Max Data Rate: 40MHz
- Single 12V power supply
- Input Clock Pulse: CMOS 5V drive
- Package: 28 pin Cer-DIP (400mil)

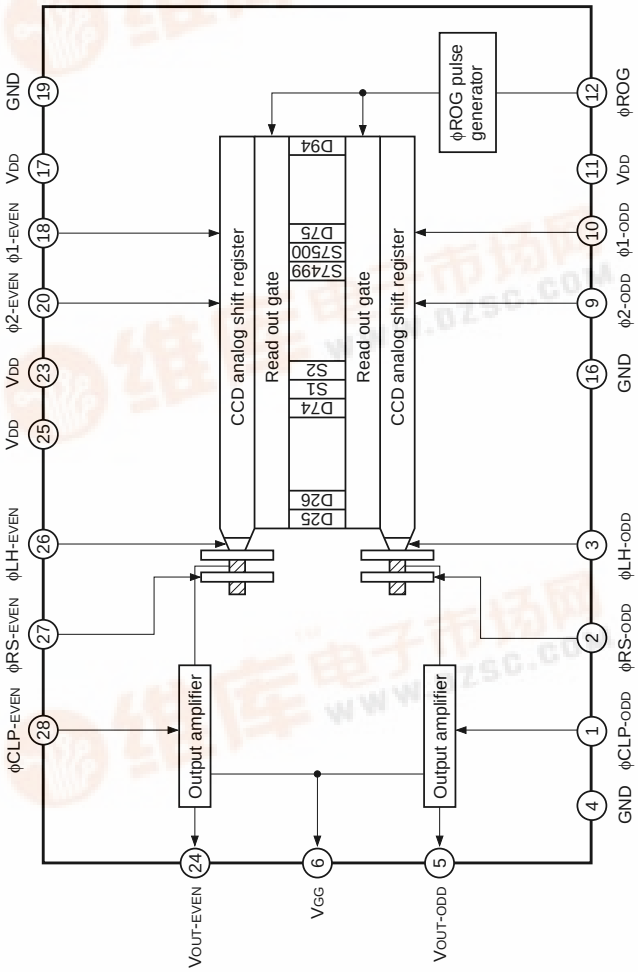
Absolute Maximum Ratings

• Supply voltage	V_{DD}	15	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



E98344-PS

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	φCLP-ODD	Clock pulse input (odd pixel)	15	NC	NC
2	φRS-ODD	Clock pulse input (odd pixel)	16	GND	GND
3	φLH-ODD	Clock pulse input (odd pixel)	17	V_{DD}	12V power supply
4	GND	GND	18	φ1-EVEN	Clock pulse input (even pixel)
5	$V_{OUT-ODD}$	Signal out (odd pixel)	19	GND	GND
6	VGG	Output circuit gate bias	20	φ2-EVEN	Clock pulse input (even pixel)
7	NC	NC	21	NC	NC
8	NC	NC	22	NC	NC
9	φ2-ODD	Clock pulse input (odd pixel)	23	V_{DD}	12V power supply
10	φ1-ODD	Clock pulse input (odd pixel)	24	$V_{OUT-EVEN}$	Signal out (even pixel)
11	V_{DD}	12V power supply	25	V_{DD}	12V power supply
12	φROG	Readout gate clock pulse input	26	φLH-EVEN	Clock pulse input (even pixel)
13	NC	NC	27	φRS-EVEN	Clock pulse input (even pixel)
14	NC	NC	28	φCLP-EVEN	Clock pulse input (even pixel)

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φ1*1, φ2*1	Cφ1, Cφ2	—	500	—	pF
Input capacity of φLH*1	$C_{\phi LH}$	—	10	—	pF
Input capacity of φRS*1	$C_{\phi RS}$	—	10	—	pF
Input capacity of φCLP*1	$C_{\phi CLP}$	—	10	—	pF
Input capacity of φROG	$C_{\phi ROG}$	—	10	—	pF

*1 It indicates that φ1-ODD, φ1-EVEN as φ1, φ2-ODD, φ2-EVEN as φ2, φLH-ODD, φLH-EVEN as φLH, φRS-ODD, φRS-EVEN as φRS, φCLP-ODD, φCLP-EVEN as φCLP.

Clock Frequency

	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φLH, φRS, φCLP	$f_{\phi1}$, $f_{\phi2}$, $f_{\phi LH}$, $f_{\phi RS}$, $f_{\phi CLP}$	—	1	20	MHz
Data rate	$f_{\phi R}$	—	2	40	MHz

Input Clock Pulse Voltage Condition

		Min.	Typ.	Max.	Unit
φ1, φ2, φLH, φRS, φCLP, φROG pulse voltage	Low level	—	0	0.1	V
	High level	4.75	5.0	5.25	V

Electrooptical Characteristics (Note 1)

(Ta = 25°C, V_{DD} = 12V, $f_{\phi R}$ = 2MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	8.2	11	13.8	V/(lx · s)	Note 2
Sensitivity 2	R2	—	25.1	—	V/(lx · s)	Note 3
Sensitivity nonuniformity	PRNU	—	4	10	%	Note 4
Saturation output voltage	V_{SAT}	1.8	2.5	—	V	Note 5
Saturation exposure	SE	0.13	0.23	—	lx · s	Note 6
Register imbalance	RI	—	1	7	%	Note 7
Dark voltage average	V_{DRK}	—	0.3	2.0	mV	Note 8
Dark signal nonuniformity	DSNU	—	0.6	5.0	mV	Note 9
Image lag	IL	—	0.02	—	%	Note 10
Supply current	I_{VDD}	—	30	60	mA	—
Total transfer efficiency	TTE	92	98	—	%	—
Output impedance	Zo	—	150	—	Ω	—
Offset level	V_{OS}	—	6.5	—	V	Note 11

Notes)

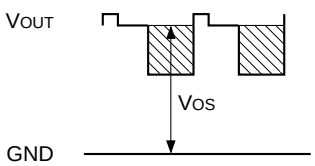
1. In accordance with the given electrooptical characteristics, the even black level is defined as the average value of D6, D8, to D24. The odd black level is defined as the average value of D5, D7, to D23.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. W lamp (2854K)
4. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.
   V_{OUT} = 500mV (Typ.)

   $$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

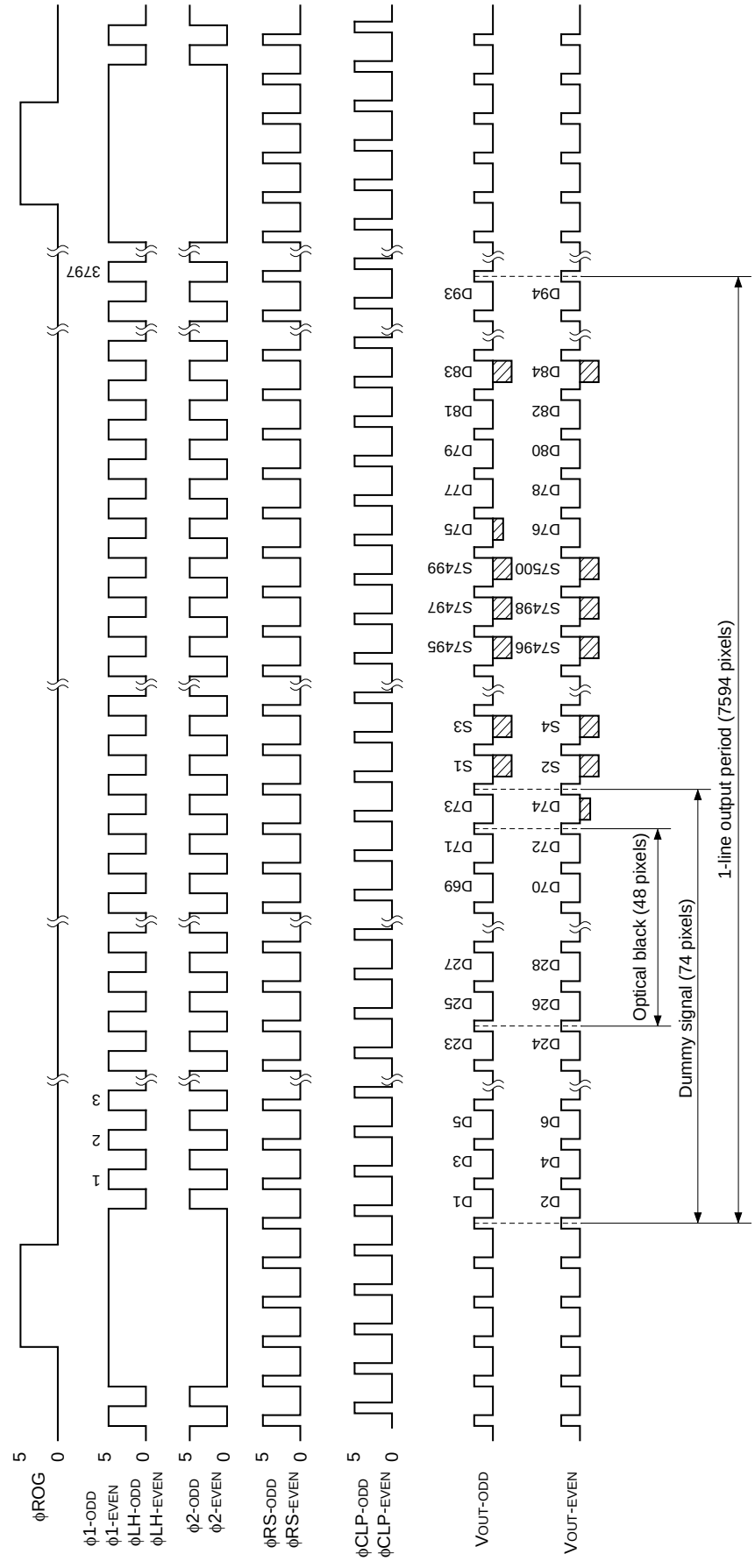
   The maximum output of each odd and even pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
5. Use below the minimum value of the saturation output voltage.
6. Saturation exposure is defined as follows. $SE = \frac{V_{SAT}}{R1}$
7. RI is defined as indicated bellow. V_{OUT} = 500mV (Typ.)

   $$RI = \frac{|\ V_{ODD\text{-}AVE} - V_{EVEN\text{-}AVE}\ |}{\left(\frac{V_{ODD\text{-}AVE} + V_{EVEN\text{-}AVE}}{2}\right)} \times 100\ [\%]$$

   Where average of odd pixels output is set to $V_{ODD\text{-}AVE}$, even pixels to $V_{EVEN\text{-}AVE}$.
8. Optical signal accumulated time τ int stands at 10ms.
9. The difference between the maximum and average values of the dark output voltage is calculated for even and odd respectively. The larger value is defined as the dark signal nonuniformity.
   Optical signal accumulated time τ int stands at 10ms.
10. V_{OUT} = 500mV (Typ.)
11. V_{OS} is defined as indicated below.

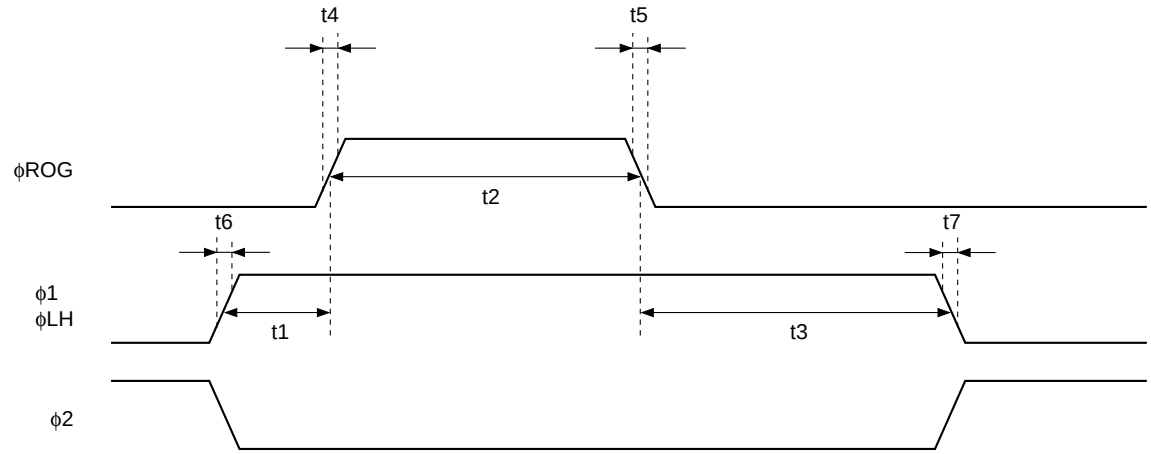


Clock Timing Chart 1 (simultaneous output)

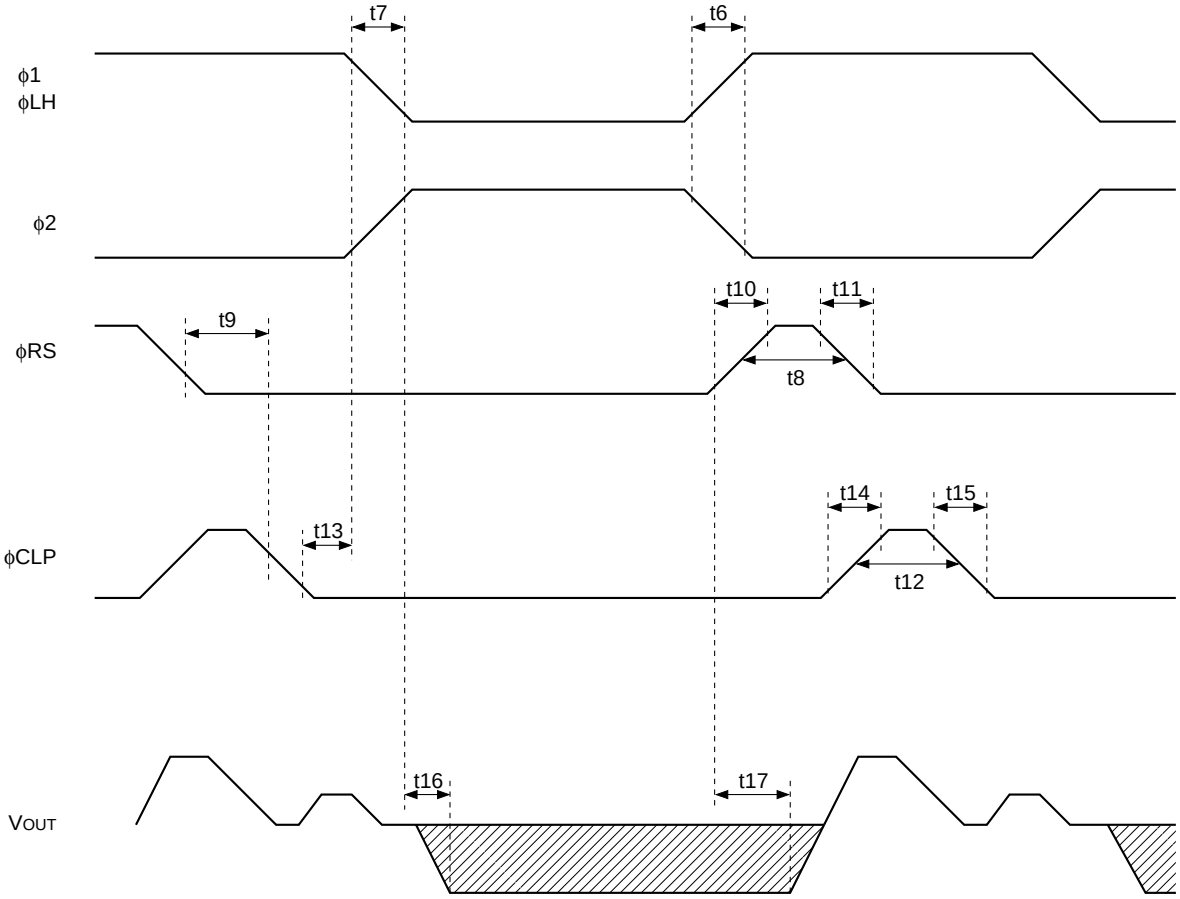


Note) The transfer pulses (φ1, φ2, φLH) must have more than 3797 cycles.

Clock Timing Chart 2



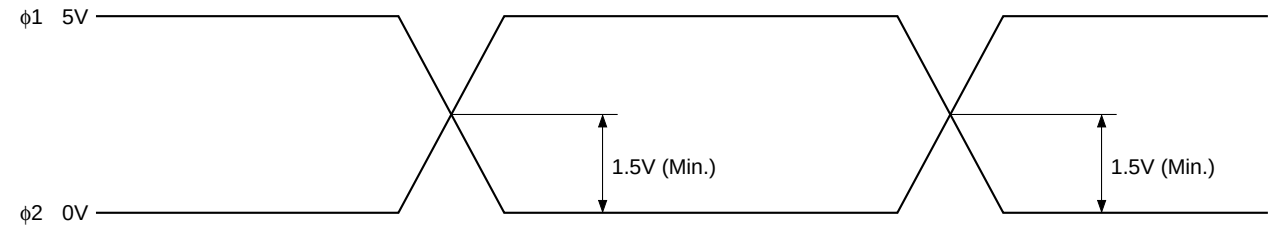
Clock Timing Chart 3



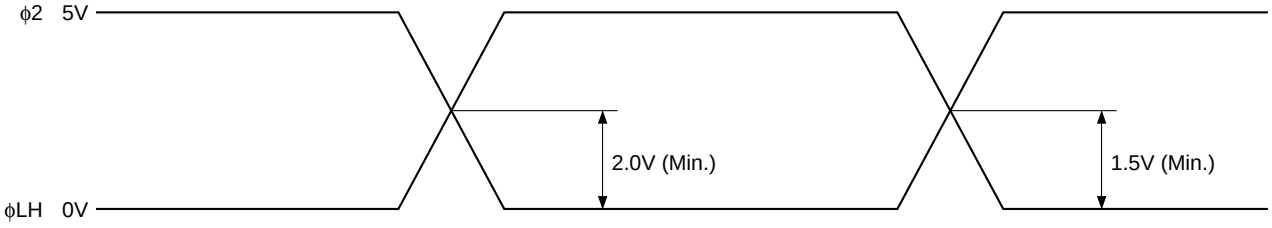
Clock timing of φ1, φ2, φLH, φRS, φCLP and VOUT at odd or even are the same as timing chart 3 in the case of alternate output.

Clock Timing Chart 4

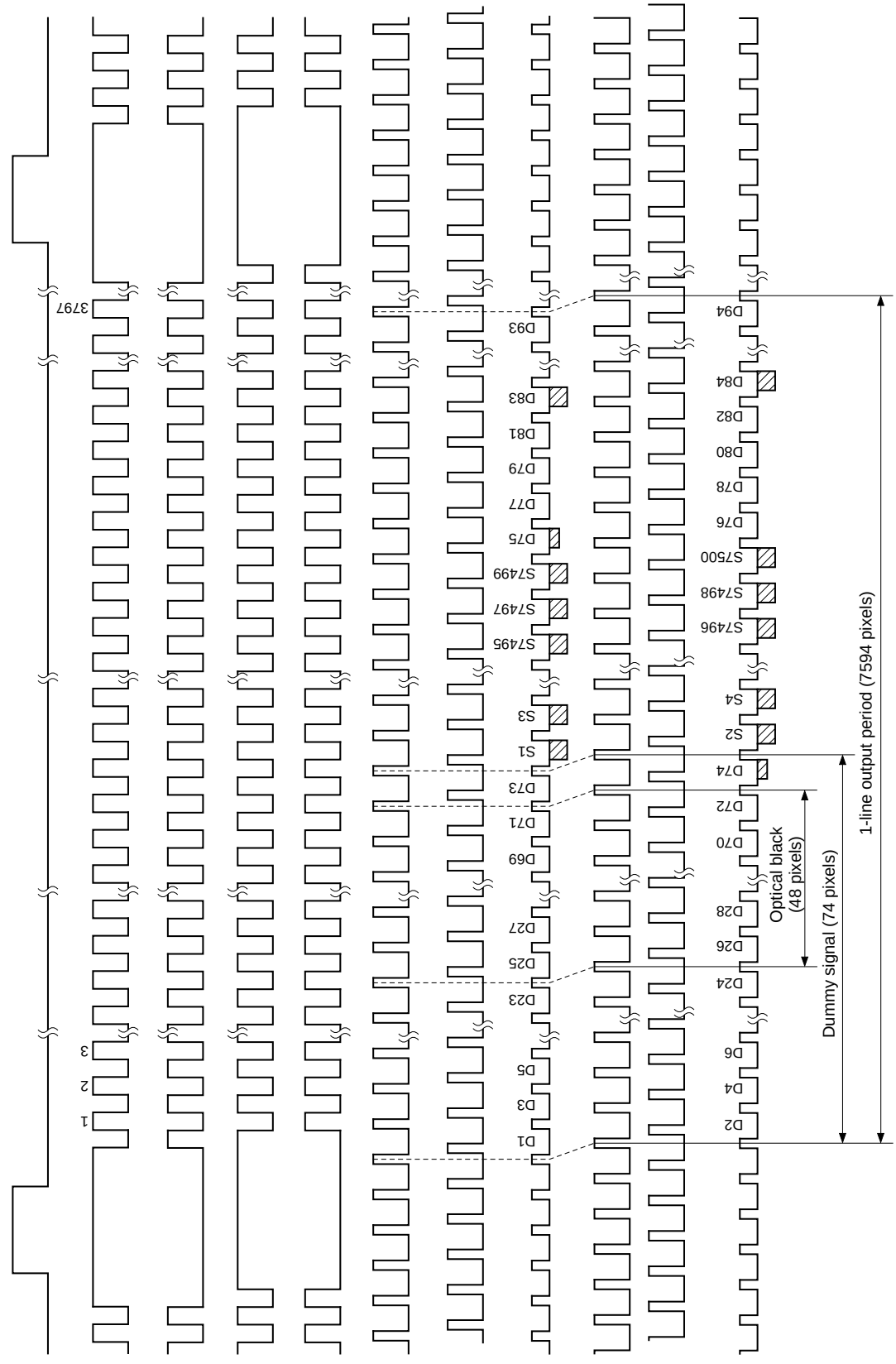
Cross point ϕ1 and ϕ2



Cross point ϕLH and ϕ2



Clock Timing Chart 5 (alternate output*1)



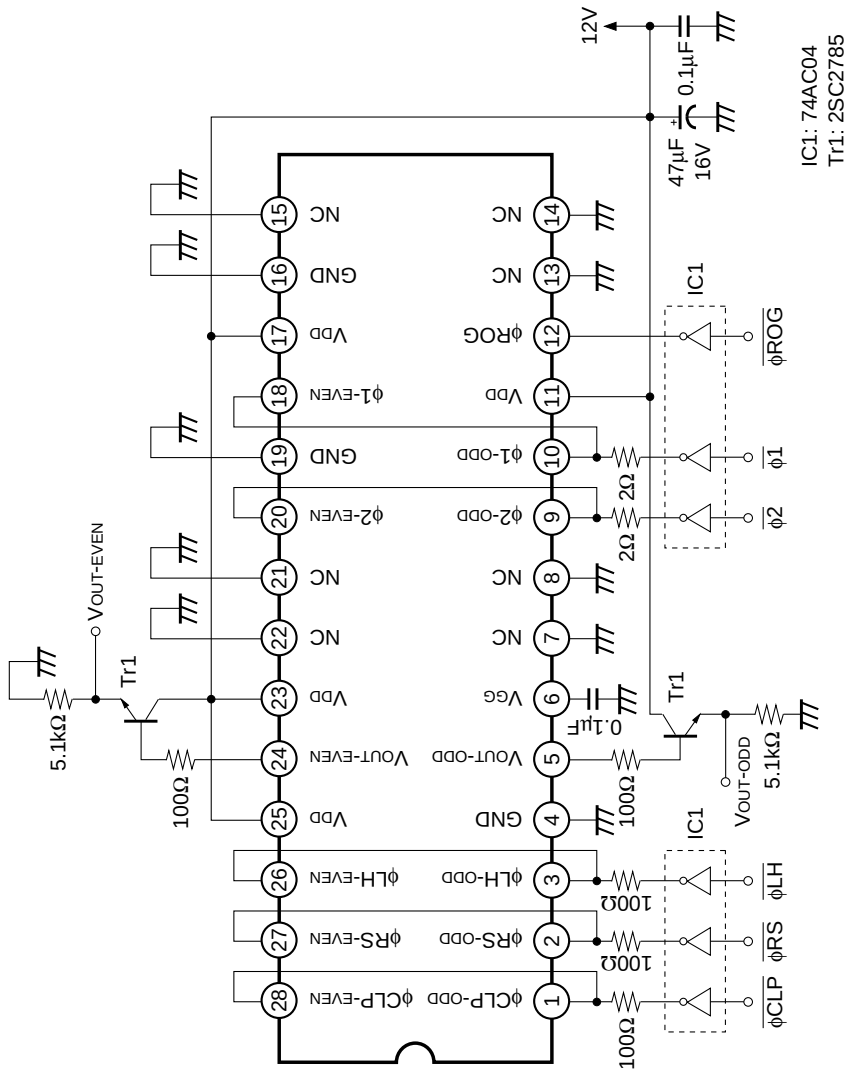
Note) The transfer pulses (φ1, φ2, φLH) must have more than 3797 cycles.
*1 Alternate output is available by making φ1-EVEN, φ2-EVEN, φLH-EVEN, φRS-EVEN, φCLP-EVEN delayed to φ1-ODD, φ2-ODD, φLH-ODD, φRS-ODD, φCLP-ODD for half a cycle.

Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
ϕROG, ϕ1 pulse timing	t1	50	100	—	ns
ϕROG pulse high level period	t2	1000	1500	—	ns
ϕROG, ϕ1 pulse timing	t3	1000	1500	—	ns
ϕROG pulse rise time	t4	0	5	10	ns
ϕROG pulse fall time	t5	0	5	10	ns
ϕ1 pulse rise time/ϕ2 pulse fall time	t6	0	20	60	ns
ϕ1 pulse fall time/ϕ2 pulse rise time	t7	0	20	60	ns
ϕRS pulse high level period	t8	10	200*1	—	ns
ϕRS, ϕCLP pulse timing	t9	10	200*1	—	ns
ϕRS pulse rise time	t10	0	10	30	ns
ϕRS pulse fall time	t11	0	10	30	ns
ϕCLP pulse high level period	t12	10	200*1	—	ns
ϕCLP, ϕLH pulse timing	t13	5	50*1	—	ns
ϕCLP pulse rise time	t14	0	10	30	ns
ϕCL pulse fall time	t15	0	10	30	ns
Signal output delay time	t16	—	8	—	ns
	t17	—	15	—	ns

*1 These timing is the recommended condition under fϕ1 = 1MHz.

Application Circuit*1

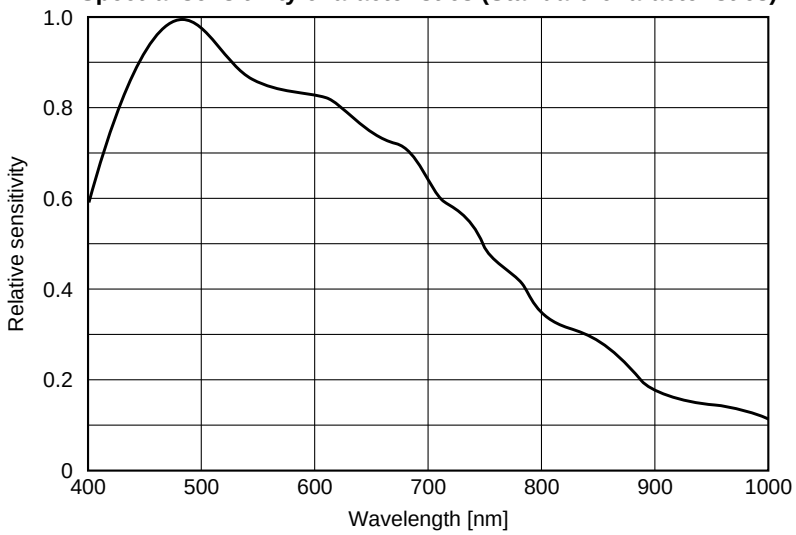


*1 Data rate $f_{\phi R}$ = 2MHz.

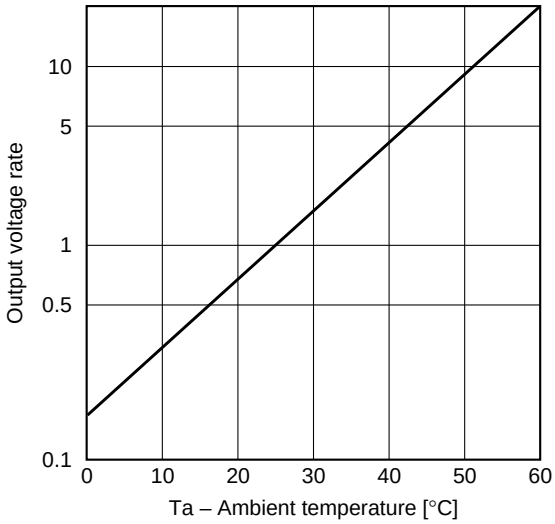
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 12V, Ta = 25°C)

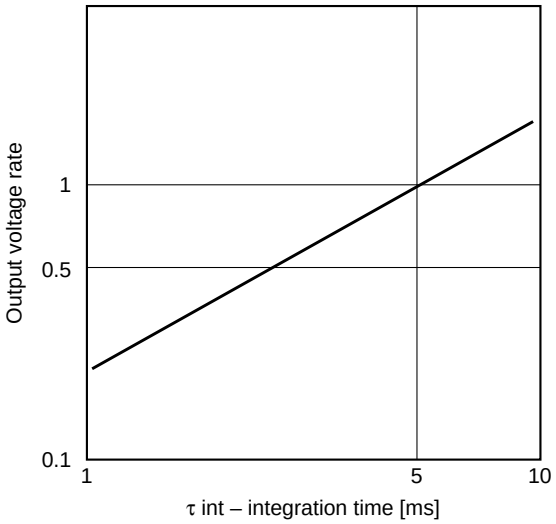
Spectral sensitivity characteristics (Standard characteristics)



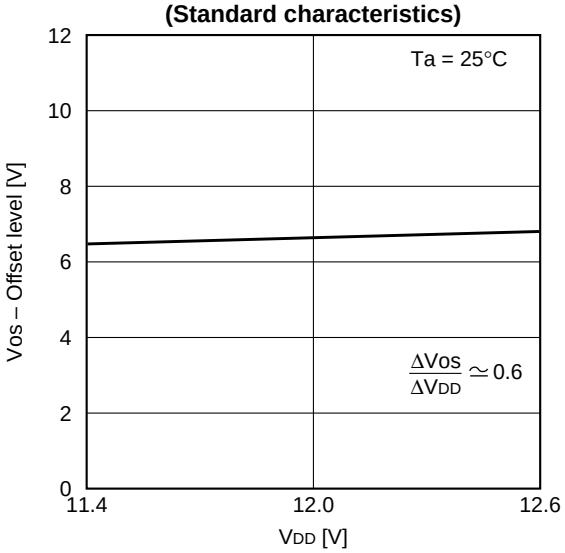
Dark signal output temperature characteristics (Standard characteristics)



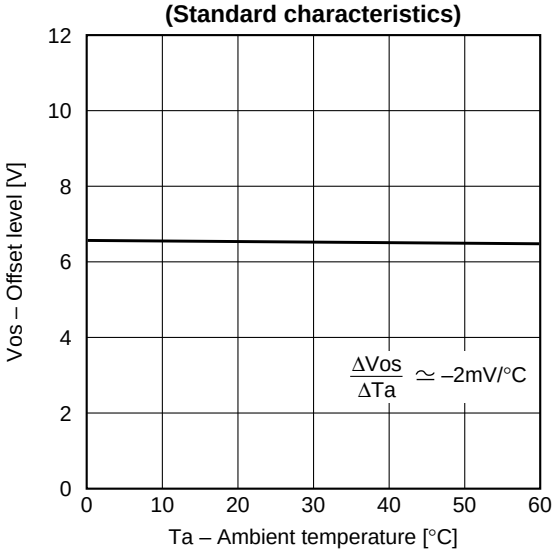
Integration time output voltage characteristics (Standard characteristics)



Offset level vs. V_{DD} characteristics (Standard characteristics)



Offset level vs. Temperature characteristics (Standard characteristics)



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material.
Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

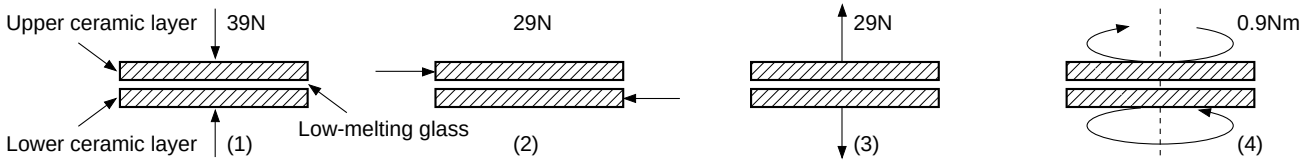
2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

a) Remain within the following limits when applying static load to the ceramic portion of the package:

(1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
(2) Shearing strength: 29N/surface
(3) Tensile strength: 29N/surface
(4) Torsional strength: 0.9Nm

b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.



c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,
(1) Applying repetitive bending stress to the external leads.
(2) Applying heat to the external leads for an extended period of time with soldering iron.
(3) Rapid cooling or heating.
(4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

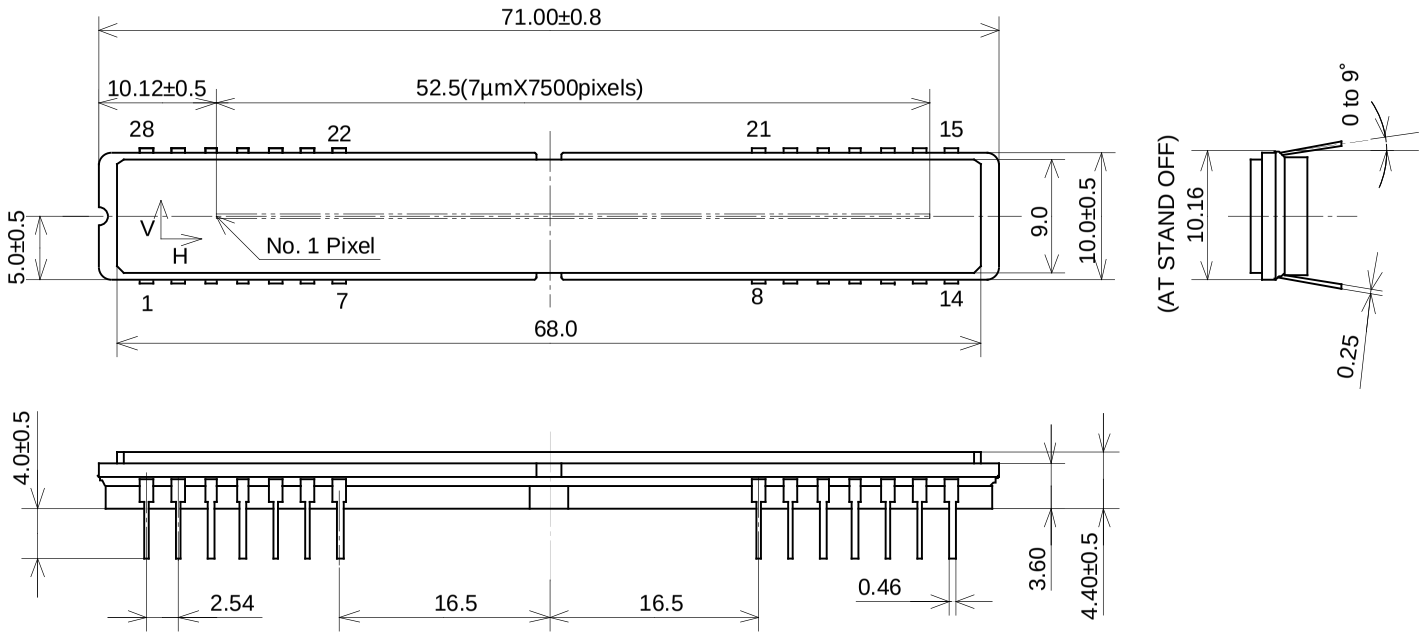
4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

28pin DIP (400mil)



1. The height from the bottom to the sensor surface is 2.4mm±0.3.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.
3. The notches of the package must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.8g
DRAWING NUMBER	LS-C5(E)