LDIP-IPM IM13400

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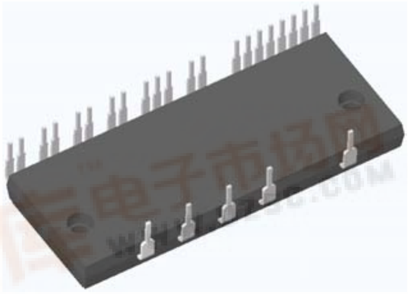
Description

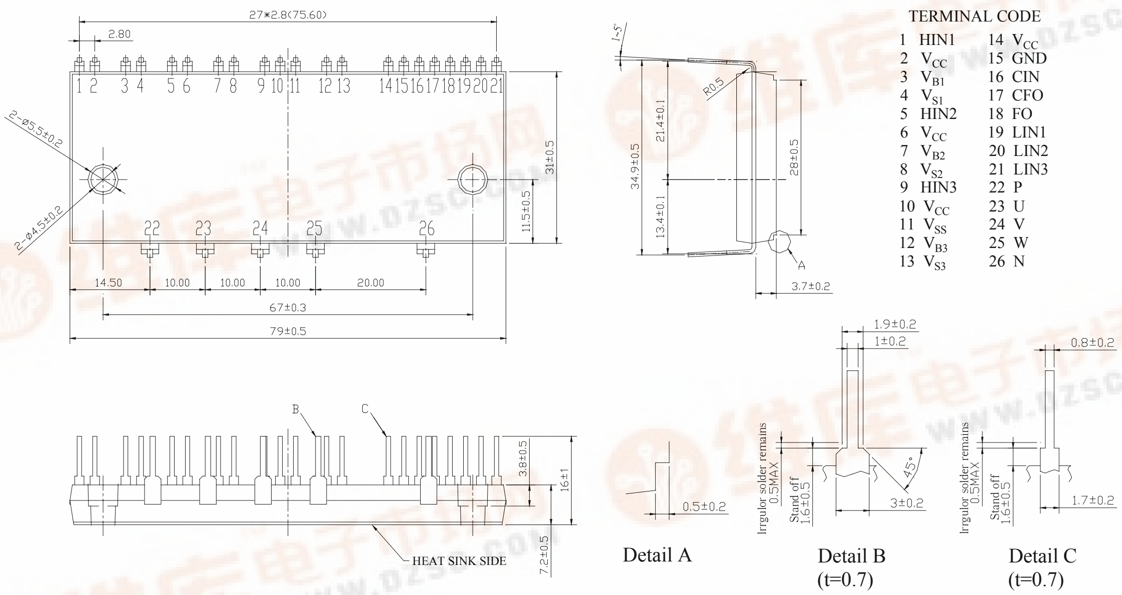
Cyntec IPM is integrated drive, protection and system control functions that is designed for high performance 3-phase motor driver application like：

- Home appliances applications.
- Inverter drive parts for AC/DC motor driving.



Features

- High latch-up immunity.
- Low switching loss and higher short-circuit withstanding capability.
- Low temperature coefficient effect both for driver and IGBT.
- Integrated driver IC to reduce the PCB size and layout effort.
- High noise rejection capability.
- Under-voltage lockout protection both for high and low side IGBT.
- High Vcc and Input signal port voltage rating.
- Good thermal performance.
- Matched propagation delay for three arms.
- Automatic shut-off the high and low side IGBT to avoid shoot-through conduction in case the driving signal is abnormal.
- Provided a fault signal (FO pin) and shut-off internal IGBT, when OC/SC and under-voltage situation are occurred.



TERMINAL CODE

1	HIN1	14	V_{CC}
2	V_{CC}	15	GND
3	V_{B1}	16	CIN
4	V_{S1}	17	CFO
5	HIN2	18	FO
6	V_{CC}	19	LIN1
7	V_{B2}	20	LIN2
8	V_{S2}	21	LIN3
9	HIN3	22	P
10	V_{CC}	23	U
11	V_{SS}	24	V
12	V_{B3}	25	W
13	V_{S3}	26	N

Figure 1.　Package Outlines

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Table 1. Pin Descriptions

No.	Symbol	Pin Description
1	HIN1	Signal Input Terminal for High-side U Phase
2	V_{CC}	Supply Voltage Terminal for Driver IC
3	V_{B1}	High -side Bias Voltage for U Phase IGBT Driving
4	V_{S1}	High -side Bias Voltage Ground for U Phase IGBT Driving
5	HIN2	Signal Input Terminal for High-side V Phase
6	V_{CC}	Supply Voltage Terminal for Driver IC
7	V_{B2}	High -side Bias Voltage for V Phase IGBT Driving
8	V_{S2}	High -side Bias Voltage Ground for V Phase IGBT Driving
9	HIN3	Signal Input Terminal for High-side W Phase
10	V_{CC}	Supply Voltage Terminal for Driver IC
11	GND	Signal Ground
12	V_{B3}	High -side Bias Voltage for W Phase IGBT Driving
13	V_{S3}	High -side Bias Voltage Ground for W Phase IGBT Driving
14	V_{CC}	Supply Voltage Terminal for Driver IC
15	GND	Signal Ground
16	CIN	Comparator Input
17	CFO	Capacitor for Fault Output Duration Time Selection
18	FO	Fault Output Terminal
19	LIN1	Signal Input Terminal for Low-side U Phase
20	LIN2	Signal Input Terminal for Low-side V Phase
21	LIN3	Signal Input Terminal for Low-side W Phase
22	P	Positive DC-Bus Input Terminal
23	U	Output Terminal for U Phase
24	V	Output Terminal for V Phase
25	W	Output Terminal for W Phase
26	N	Negative DC-Bus Input Terminal

LDIP-IPM Internal Block Diagram

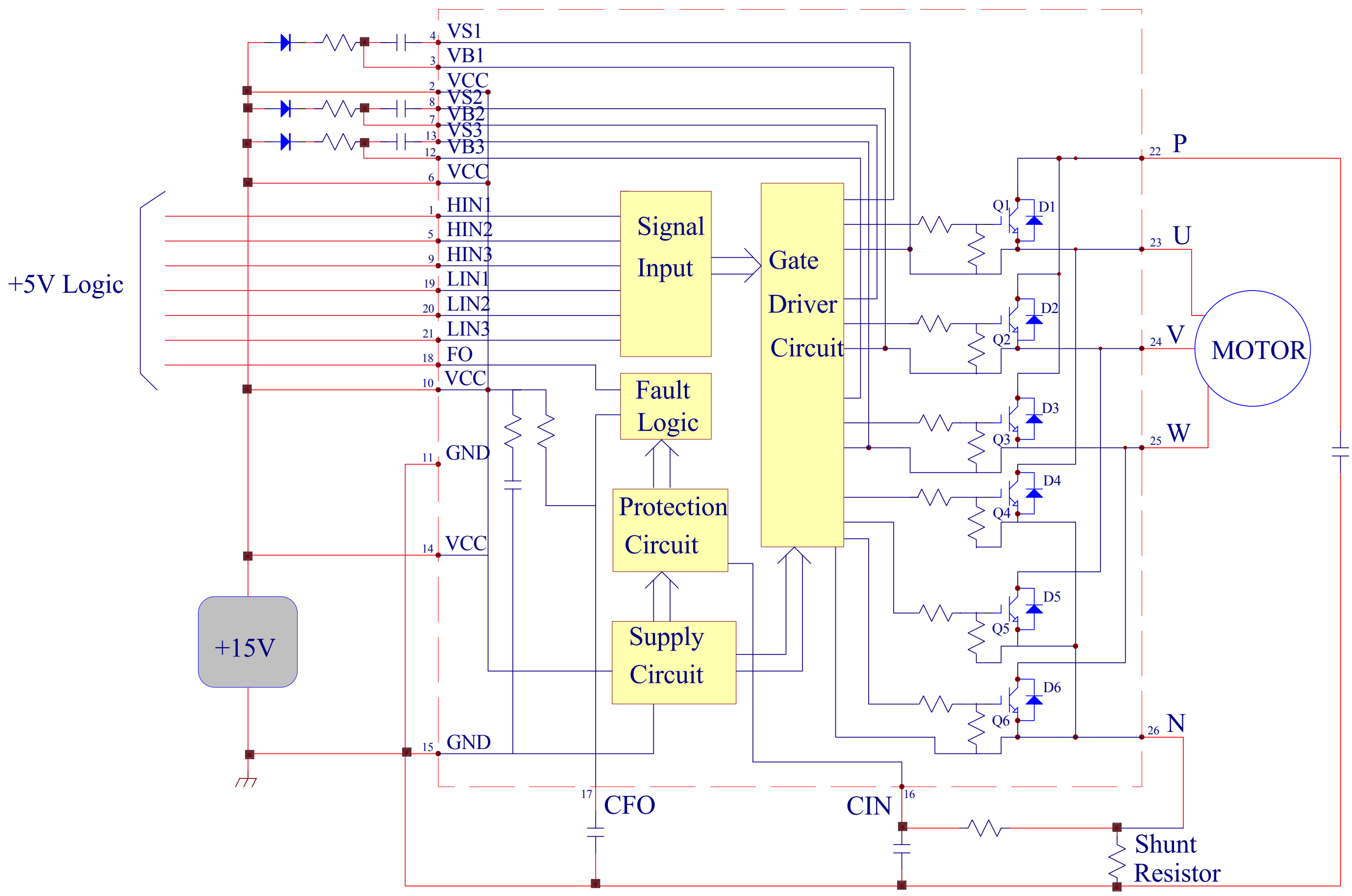

Figure 2.   LDIP-IPM Internal Block Diagram

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MAXIMUM RATINGS (T_j = 25℃)

INVERTER PART

Item	Symbol	Min.	Max.	Unit
Between collector to emitter voltage	V_{CES}	-	600	V
Each IGBT collector current	± I_C (Tc = 25℃)	-	20	A
Each IGBT collector current (peak)	± I_{CP} (Tc = 25℃, pulse)	-	40	A
Junction temperature	T_j	-20	+150	℃

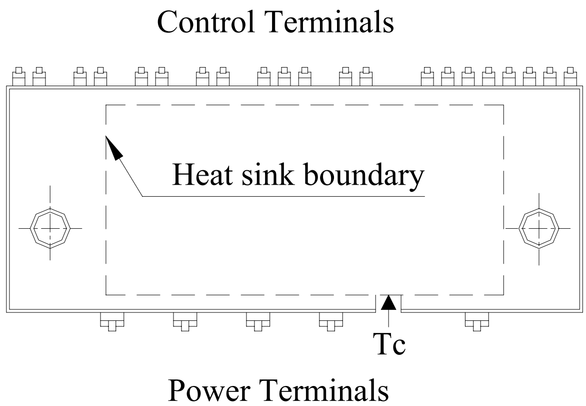
CONTROL PART

Item	Symbol	Min.	Max.	Unit
Driver IC supply voltage	V_{CC}	-0.3	25	V
P- side floating supply voltage	$V_{B1S1,B2S2,B3S3}$	-0.3	20	V
Current sensing input voltage	V_{CIN}	-0.3	25	V
Logic input voltage	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3	-0.3	25	V
Fault output voltage	V_{FO}	-0.3	25	V

TOTAL SYSTEM

Item	Symbol	Min.	Max.	Unit
Module case operating temperature	T_C **(Note 1)**	-20	+100	℃
Storage temperature	T_{stg}	-40	+150	℃
Isolation voltage (60Hz Sinusoidal, AC 1 minute, pins to heat-sink plate)	V_{iso}	-	2500	Vrms

Note 1：Tc Measurement Point.



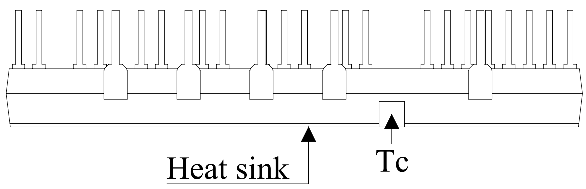


Figure 3.　Tc Measurement Point

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ELECTRICAL CHARACTERISTICS (T_j = 25℃)

INVERTER PART

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE\ (sat)}$	$V_{CC} = V_{B1S1,B2S2,B3S3}$ = 15V, I_C =20A, V_{CIN} = 0V	T_j=25℃	-	2.3	2.8	V
FWD forward voltage drop	V_F	T_j = 25℃, - I_C = 20A, V_{CIN} = 5V		-	2.0	2.4	V
Switching times **(Fig. 4)**	T_{on}	V_D = 300V, $V_{CC} = V_{B1S1,B2S2,B3S3}$ = 15V, I_C = 20A, T_j =25℃, V_{HIN} =5V<—> 0V, V_{CIN} = 0V, Inductive Load		-	0.6	0.8	μs
	T_r			-	0.06	0.12	
	T_{off}			-	1.0	1.2	
	T_f			-	0.05	0.1	
Collector-emitter cut-off current	I_{CES}	V_{CE} =V_{CES}		-	-	0.32	mA

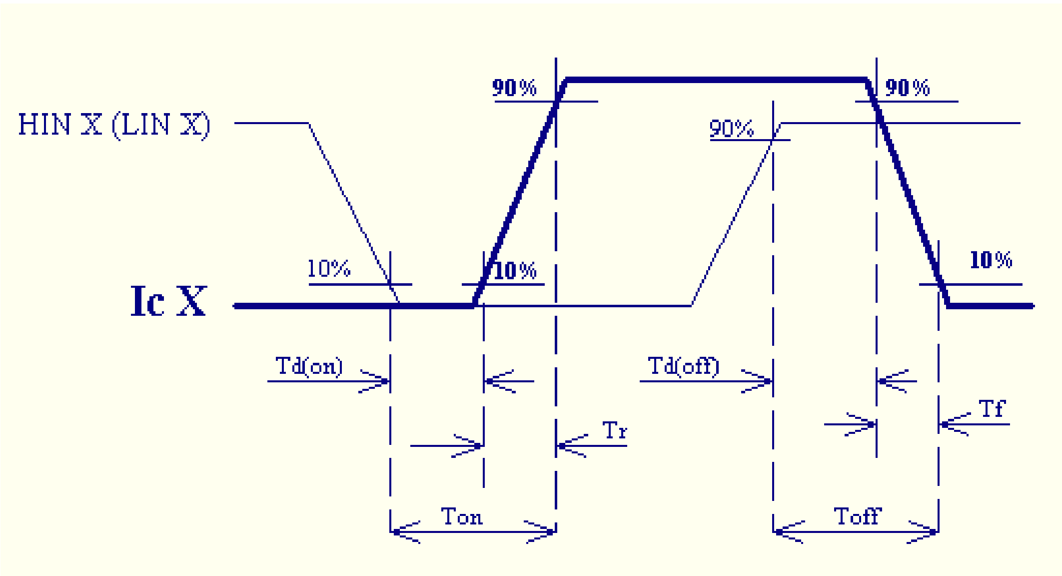

Figure 4. Switching Time Define

Test condition：Vdc =300V, Ic = 20A, Vcc = 15V, Vin = 0V→5V (Inductive Load), TC = 25℃

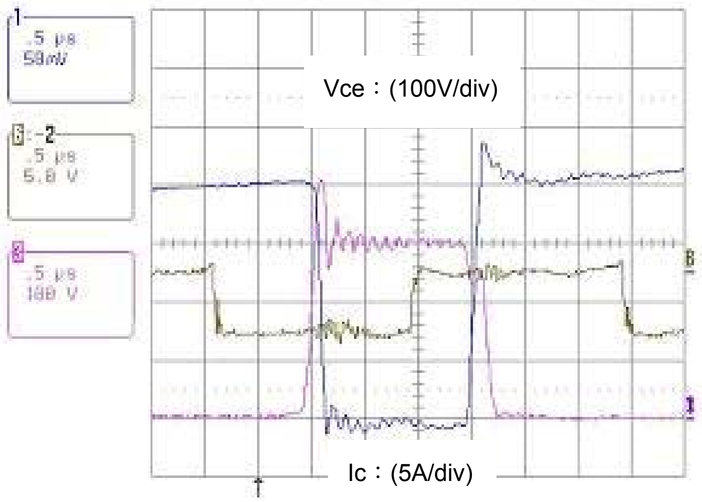

Figure 5.　Testing Switching Waveform

CONTROL PART (T_j = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HIN1,2,3 , LIN1,2,3 ON threshold voltage	$V_{th(on)}$		1.4-	1.7	2.0	V
HIN1,2,3 , LIN1,2,3 OFF threshold voltage	$V_{th(off)}$		2.2	2.5	2.8	V
HIN1,2,3 input current	$I_{HIN(HI)}$	$V_{HIN1,2,3}$ = 5V	-	-	220	μA
	$I_{HIN(LO)}$	$V_{HIN1,2,3}$ = 0V	-	-	300	
LIN1,2,3 input current	$I_{LIN(HI)}$	$V_{LIN1,2,3}$ = 5V	-	-	220	μA
	$I_{LIN(LO)}$	$V_{LIN1,2,3}$ = 0V	-	-	300	
Driver IC supply voltage	V_{CC}		13.5	15.0	16.5	V
P-side floating supply voltage	$V_{B1S1,B2S2,B3S3}$		13.5	15.0	16.5	V
V_{CC} terminal input current	I_C		-	-	2.3	mA
Fault output voltage	V_{FOH}	V_{CIN} =0V **(Note 2)**	4.9	-	-	V
	V_{FOL}	V_{CIN} =1V **(Note 2)**	-	-	200	mV
Short circuit trip level	$V_{SC(ref)}$	V_{CC}=15V, T_j = 25℃	0.37	0.46	0.55	V
Fault output pulse width	t_{FO}	C_{FO} =22nF ~ 33nF **(Note 3)**	-	1.8	-	ms
Supply circuit under voltage protection	UVT_{VCC}	Trip level	10.4	10.9	11.4	V
	UVR_{VCC}	Reset level	10.6	11.1	11.6	V
	UVH	Hysteresis	-	0.2	-	V

Note 2 : FO output is open collector type, so this signal line should be pulled up to the +5V power supply with approximately 5.1KΩ.

Note 3：C_{FO} need to adjust if output can not fit 1.8 ms demand.

THERMAL RESISTANCE

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance	$R_{th(j-c)Q}$	IGBT part (1/6)	-	-	1.1	℃/W
	$R_{th(j-c)F}$	FWD part (1/6)	-	-	1.6	

RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DC_ Link Supply voltage	V_D	Applied between P-N	0	300	400	V
Control supply voltage	V_{CC}	Applied between V_{CC} - GND	13.5	15.0	16.5	V
Control supply voltage	$V_{B1S1,B2S2,B3S3}$	Applied between $V_{B1,2,3}$ – $V_{S1,2,3}$	13.5	15.0	16.5	V
Input ON threshold voltage	$V_{CIN(ON)}$	Applied between HIN1,2,3 - GND and LIN1,2,3 - GND	0 ~ 0.65			V
Input OFF threshold voltage	$V_{CIN(OFF)}$		4.0 ~ 5.5			V
Supply voltage ripple	ΔV_D , ΔV_{DB}		-1	-	1	V/μs
Arm shoot-through blocking time	t_{dead}	**(Note 4)**	2	-	-	μs
PWM Input frequency	f_{PWM}	$T_C \leqq 100$℃, $T_j \leqq 125$℃	-	15	-	kHz

Note 4：To prevent high and low side IGBT occurred shoot-through.

MECHANICAL CHARACTERISTICS AND RATINGS

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw：M4	Recommended 1.18 N・m	0.98	1.18	1.37	N-m
Weight		--	-	75	-	g
Heat-sink flatness	**(Note 5)**	--	-50	-	100	μm

Note 5：Measurement point of heat-sink flatness.

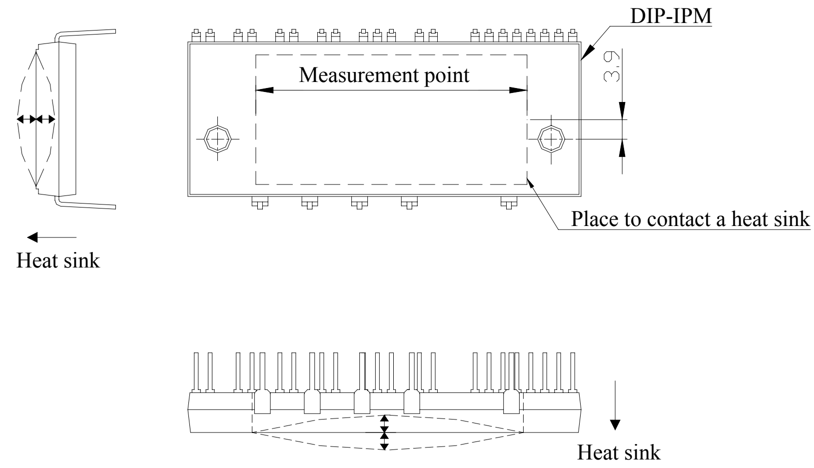

Figure 6.　Measurement Point of Heat-sink Flatness

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Input/Output Timing Diagram

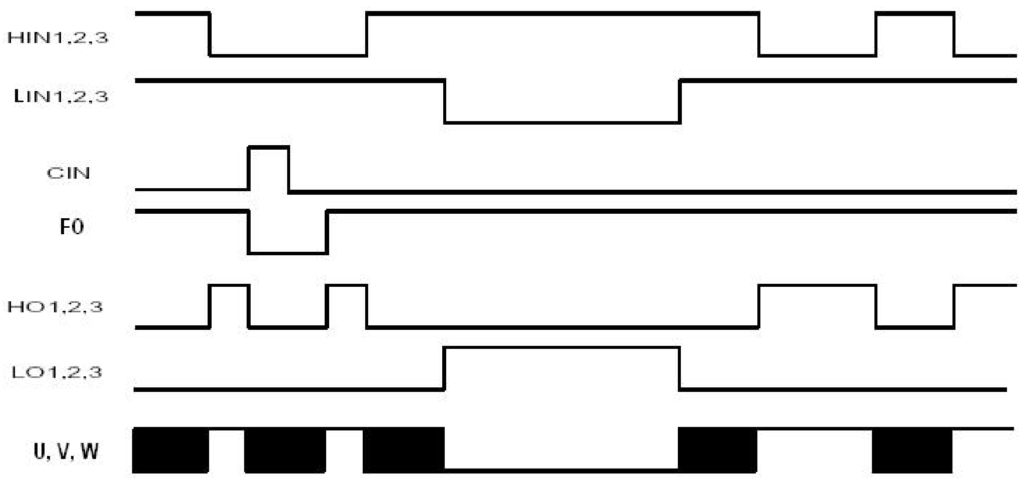
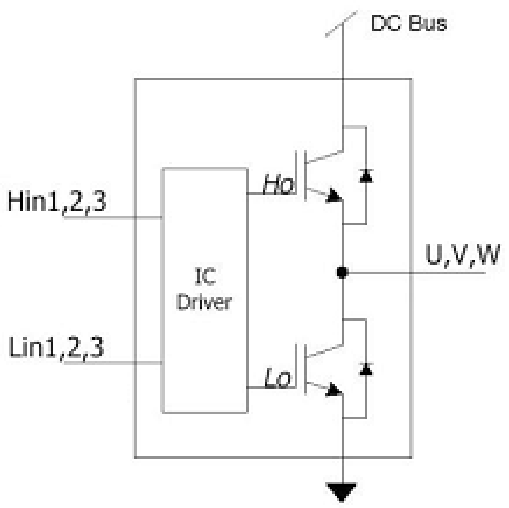


Figure 7. Input/Output Timing Diagram

Note 6：The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.



CIN	HIN1,2,3	LIN1,2,3	U,V,W
0	0	1	DC Bus
0	1	0	0
0	1	1	X
1	X	X	X

Figure 8. Input/Output Signal Circuit

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LDIP-IPM Short-Circuit Protection Function

S1. Normal operation：IGBT ON and carrying current.
S2. Short circuit current detection (SC trigger).
S3. IGBT gate interrupt and FO signal starts.
S4. IGBT turns OFF.
S5. IGBT OFF state.
S6. FO signal reset.
S7. Normal operation.

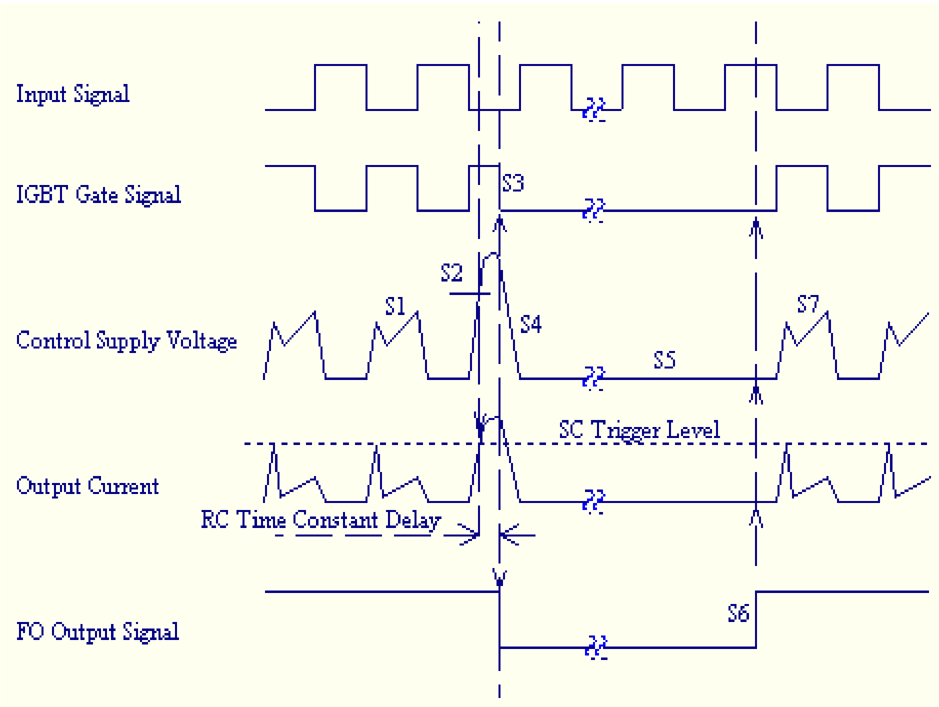

Figure 9. Timing Chart of SC Operation

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LDIP-IPM Under-Voltage Protection Function

S1. Normal operation：IGBT ON and carrying current.
S2. Under-Voltage detection.
S3. IGBT gate interrupt.
S4. IGBT OFF state.
S5. Under-Voltage reset.
S6. Normal operation.

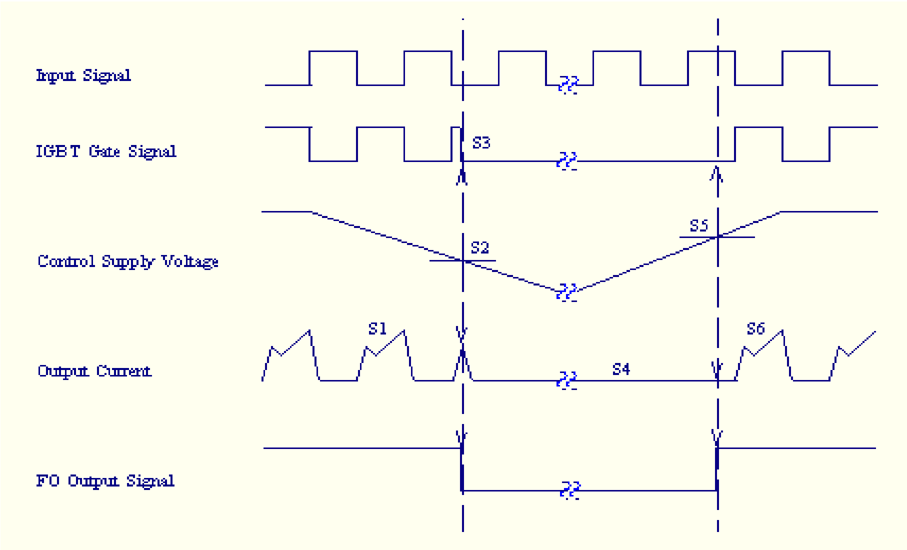

Figure 10.　Timing Chart of Under-Voltage Operation

Recommended CPU I/O Interface Circuit

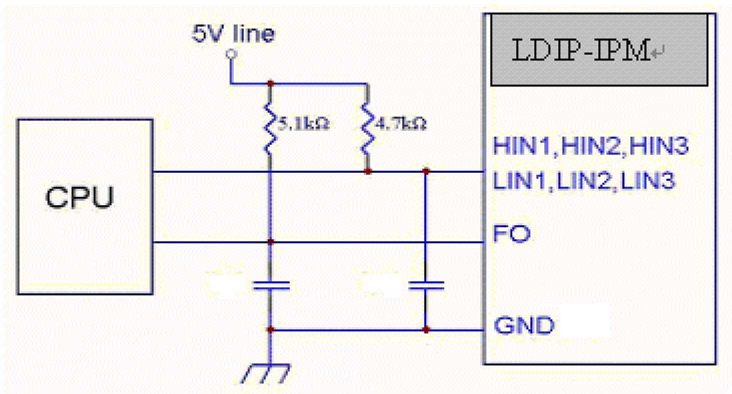

Figure 11.　I/O Interface Circuit

Note 7：Depending on the wiring impedances and the PWM control circuit of the application's PCB, the RC coupling at each input may be changed.

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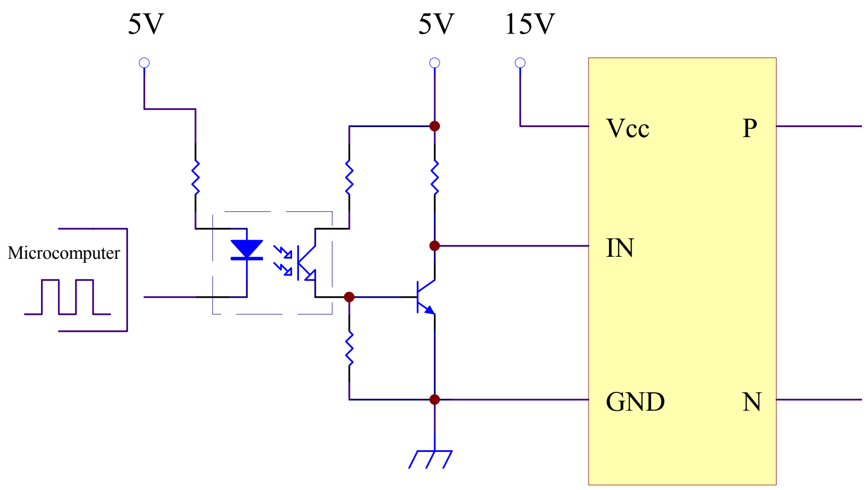
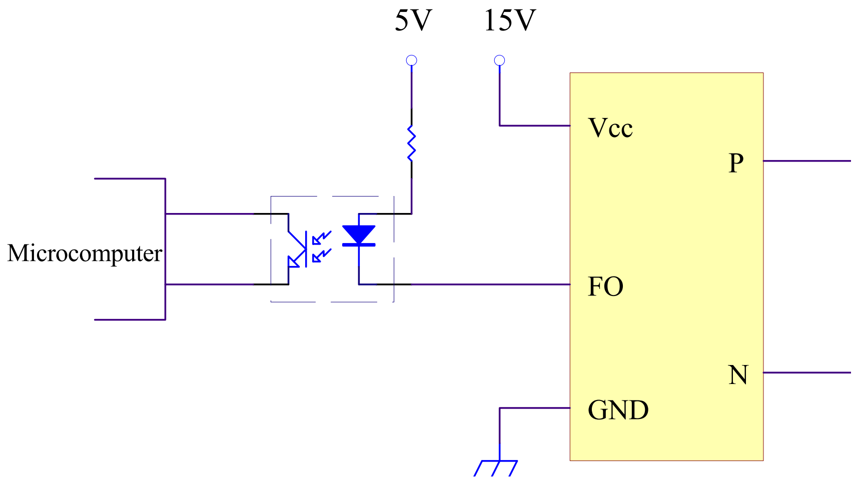
Recommended Circuit Example When Using a Photo Coupler



(a) IPM input pin (high-side 3-phase and low-side 3-phase)



(b) Fault output pin

Figure 12. I/O Interface Circuit When Using Photo Coupler

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Direct Input (without Photo-Coupler) Interface Example

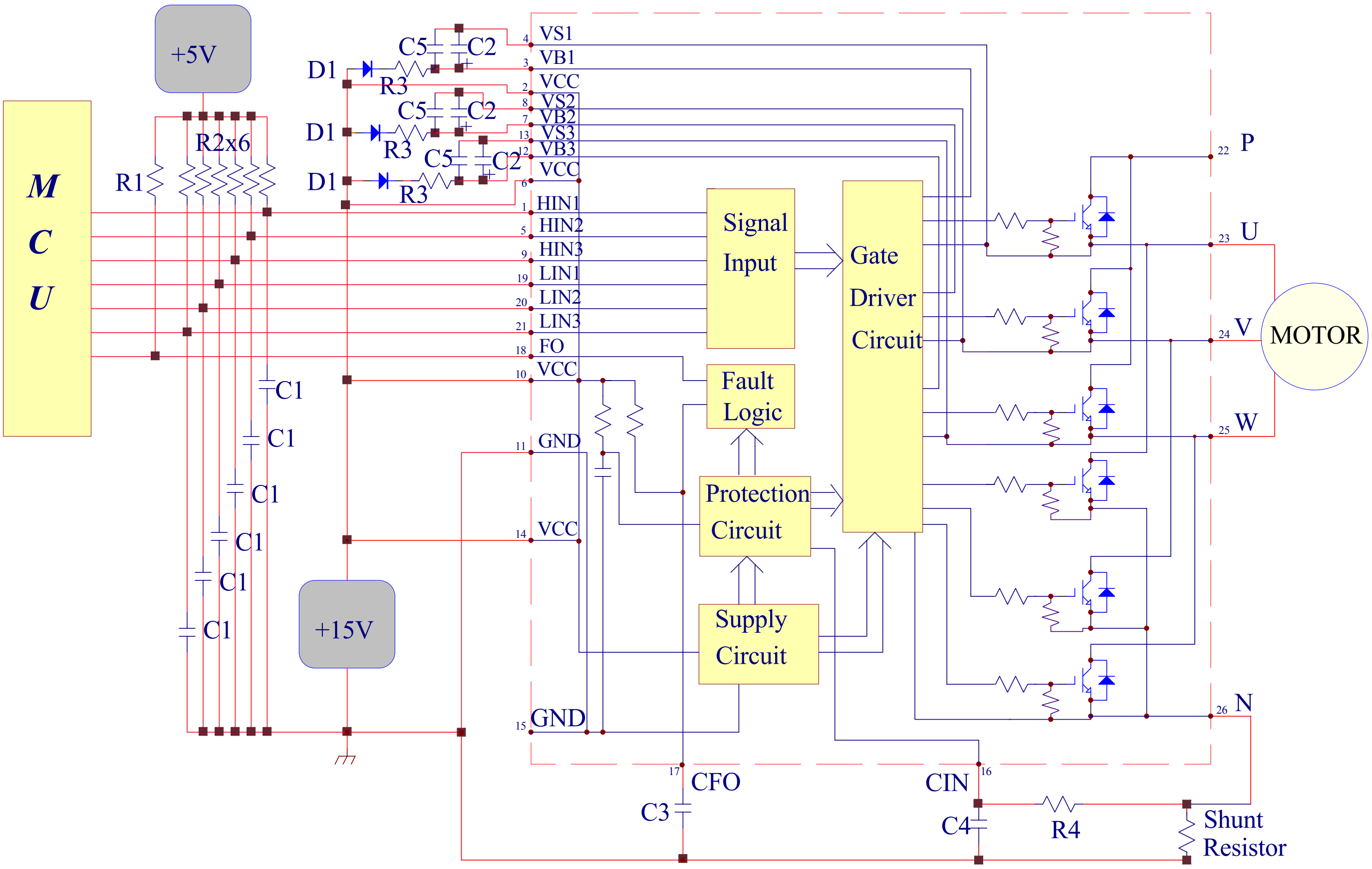

Figure 13. Typical Application Circuit Interface Example with Direct Input

Component selection :

1. R1 : 5.1KΩ (FO output is open collector type. It is necessary to apply a resistor.)
2. R2 : 4.7KΩ
3. R3 : 20Ω (It could be adjusted depending on the PWM frequency.)
4. R4 : 100Ω (Recommended the time constant R4xC4 is 2μS.)
5. C1 : 100 ~ 1000pF (Ceramic) (The capacitor could filter the noise, but should be careful to the dead time)
6. C2 : 10 ~ 100μF (Electrolytic, low impendence)
7. C3 : 22nF (Ceramic)
8. C4 : 0.02μF (Ceramic)
9. C5 : 0.22 ~ 2μF (Ceramic)
10. D1 : 600V/1A (Ultra-Fast recovery diode)

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Interface Example when a Photo-Coupler is used

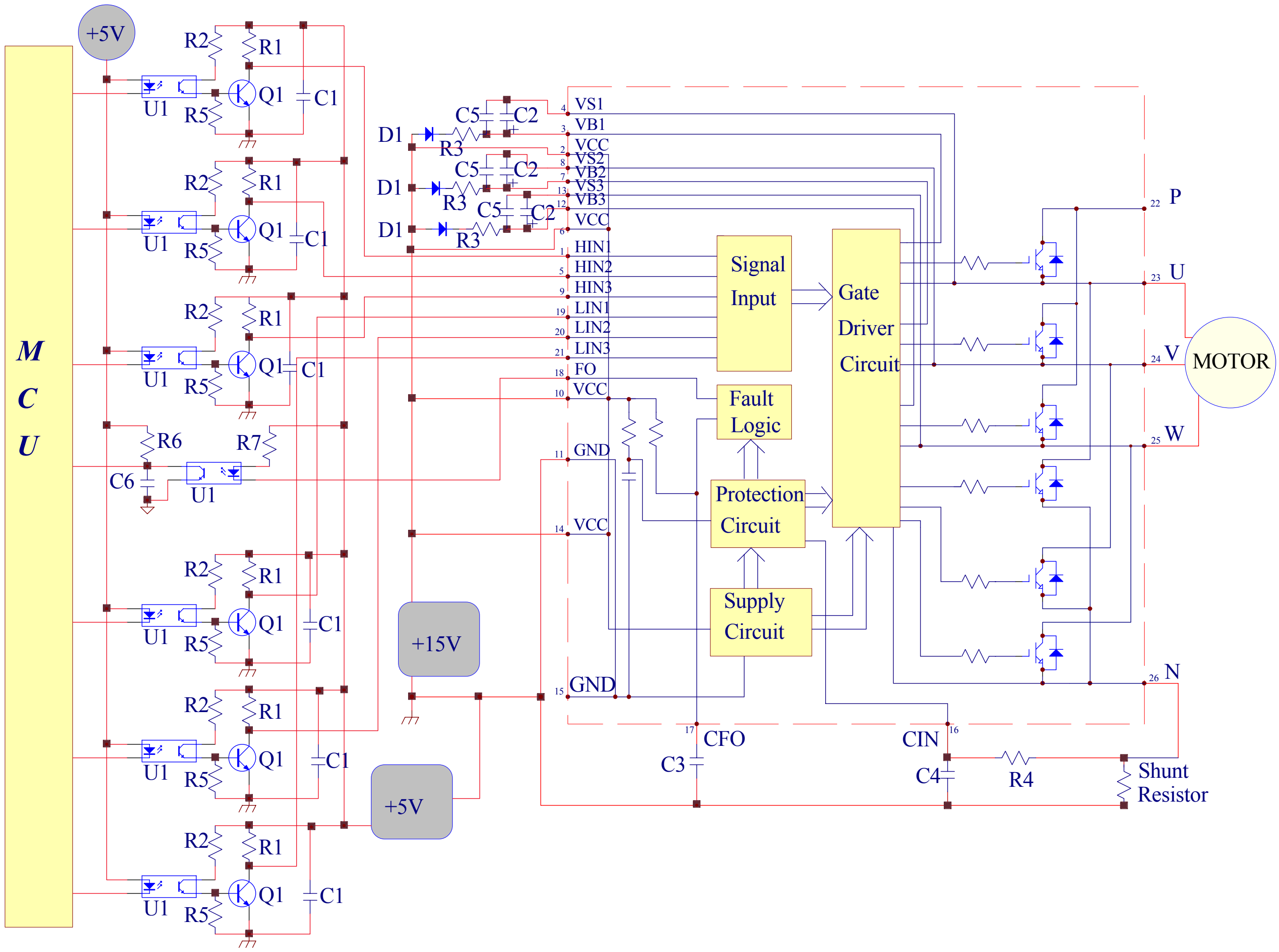

Figure 14. Typical Application Circuit Interface Example with Photo Coupler

Component selection :

1. R1 : 4.7KΩ
2. R2 : 150Ω
3. R3 : 20Ω (It could be adjusted depending on the PWM frequency.)
4. R4 : 100Ω (Recommended the time constant R4xC4 is 2 μS.)
5. R5 : 1KΩ
6. R6 : 1KΩ
7. R7 : 1KΩ
8. C1 : 0.1 μF
9. C2 : 10 ~ 100 μF (Electrolytic, low impendence)
10. C3 : 22nF (Ceramic)
11. C4 : 0.02 μF (Ceramic)
12. C5 : 0.22 ~ 2 μF (Ceramic)
13. C6 : 0.1 μF
14. D1 : 600V/1A (Ultra-Fast recovery diode)
15. Q1 : NPN transistor 2N3904
16. U1 : Photo coupler TLP521

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Precautions on Electrostatic Electricity

(1) Operators must wear anti-static clothing and conductive shoes (or a leg or heel strap).

(2) Operators must wear a wrist strap grounded to earth via a resistor of about 1 MΩ.

(3) Soldering irons must be grounded from iron tip to earth, and must be used only at low voltages.

(4) If the tweezers you use are likely to touch the device terminals, use anti-static tweezers and in particular avoid metallic tweezers. If a charged device touches a low-resistance tool, rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pat to the tip, and connect it to a dedicated ground used especially for anti-static purposes (suggested resistance value: 10^4 to $10^8 \Omega$).

(5) Do not place devices or their containers near sources of strong electrical fields (such as above a CRT).

(6) When storing printed circuit boards which have devices mounted on them, use a board container or bag that's protected against static charge. To avoid the occurrence of static charge or discharge due to friction, keep the boards separate from one other and do not stack them directly on top of one another.

(7) Ensure, if possible, that any articles (such as clipboards) which are brought to any location where the level of static electricity must be closely controlled are constructed of anti-static materials.

(8) In cases where the human body comes into direct contact with a device, be sure to wear anti-static finger covers or gloves (suggested resistance value: $10^8 \Omega$ or less).

(9) Equipment safety covers installed near devices should have resistance ratings of $10^9 \Omega$ or less.

(10) If a wrist strap cannot be used for some reason, and there is a possibility of imparting friction to devices, use an ionizer.