

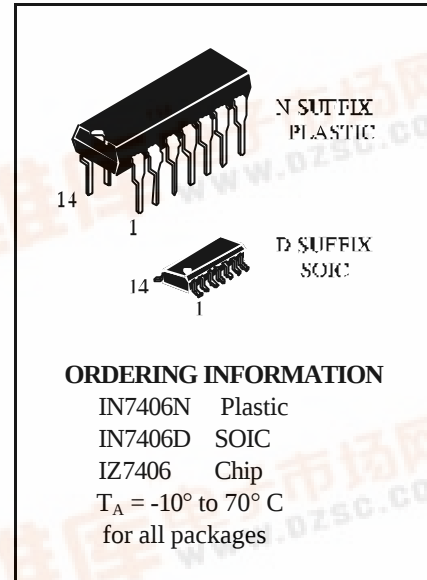
## TECHNICAL DATA

### IN7406

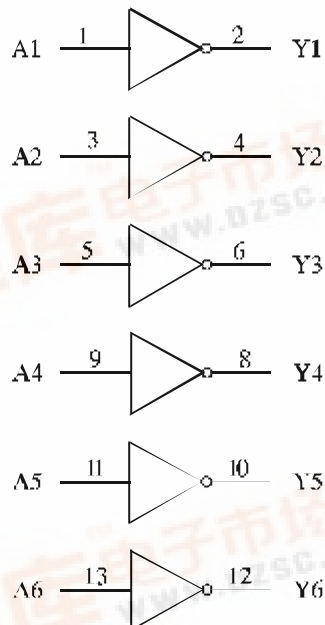
## Hex Inverter Buffers/Drivers with Open-Collector High-Voltage Outputs

The IN7406 monolithic TTL hex inverter buffers/drivers feature high-voltage open collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs.

- Minimum breakdown Voltages is 30 V
- Maximum sink Current is 40 mA
- Converts TTL Voltage Levels to MOS Levels
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible with MOST TTL Circuits.

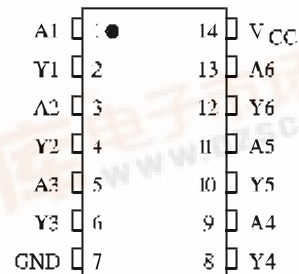


### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
PIN 7 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

| Inputs | Output |
|--------|--------|
| A      | Y      |
| L      | Z      |
| H      | L      |

Z = High Impedance

**MAXIMUM RATINGS\***

| Symbol    | Parameter                 | Value       | Unit |
|-----------|---------------------------|-------------|------|
| $V_{CC}$  | Supply Voltage            | 7.0         | V    |
| $V_{IN}$  | Input Voltage             | 5.5         | V    |
| $V_{OUT}$ | Output Voltage            | 30          | V    |
| Tstg      | Storage Temperature Range | -65 to +150 | °C   |

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol   | Parameter                 | Min  | Max  | Unit |
|----------|---------------------------|------|------|------|
| $V_{CC}$ | Supply Voltage            | 4.75 | 5.25 | V    |
| $V_{IH}$ | High Level Input Voltage  | 2.0  |      | V    |
| $V_{IL}$ | Low Level Input Voltage   |      | 0.8  | V    |
| $U_{OH}$ | High Level Output Voltage |      | 30   | V    |
| $I_{OL}$ | Low Level Output Current  |      | 40   | mA   |
| $T_A$    | Ambient Temperature Range | -10  | +70  | °C   |

**DC ELECTRICAL CHARACTERISTICS**

| Symbol   | Parameter                 | Test Conditions                          | Guaranteed Limit |      | Unit |
|----------|---------------------------|------------------------------------------|------------------|------|------|
|          |                           |                                          | Min              | Max  |      |
| $V_{IK}$ | Input Clamp Voltage       | $V_{CC} = 4.75V, I_{IN} = -12\text{ mA}$ |                  | -1.5 | V    |
| $I_{OH}$ | High Level Output Current | $V_{CC} = 4.75V, V_{OH} = 30V$           |                  | 0.25 | mA   |
| $V_{OL}$ | Low Level Output Voltage  | $V_{CC} = 4.75V, I_{OL} = 16\text{ mA}$  |                  | 0.4  | V    |
|          |                           | $V_{CC} = 4.75V, I_{OL} = 40\text{ mA}$  |                  | 0.7  |      |
| $I_{IH}$ | High Level Input Current  | $V_{CC} = 5.25V, V_{IN} = 2.4\text{ V}$  |                  | 0.04 | mA   |
| $I_{IL}$ | Low Level Input Current   | $V_{CC} = 5.25V, V_{IN} = 0.4\text{ V}$  |                  | -1.6 | mA   |
| $I_{CC}$ | Supply Current            | $V_{CC} = 5.25V$                         | Outputs High     | 48   | mA   |
|          |                           |                                          | Outputs Low      | 51   |      |

**AC ELECTRICAL CHARACTERISTICS** ( $T = 25^{\circ}\text{C}$ ,  $V_{\text{CC}} = 5.0\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  
 $R_L = 110\ \Omega$ , Input  $t_r = t_f = 10\text{ ns}$ )

| Symbol           | Parameter                                                               | Min | Max | Unit |
|------------------|-------------------------------------------------------------------------|-----|-----|------|
| $t_{\text{PLH}}$ | Propagation Delay Time, Low to High Level Output (from Input to Output) |     | 18  | ns   |
| $t_{\text{PHL}}$ | Propagation Delay Time, High to Low Level Output (from Input to Output) |     | 28  | ns   |

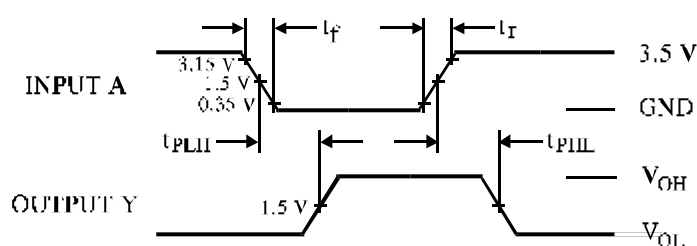
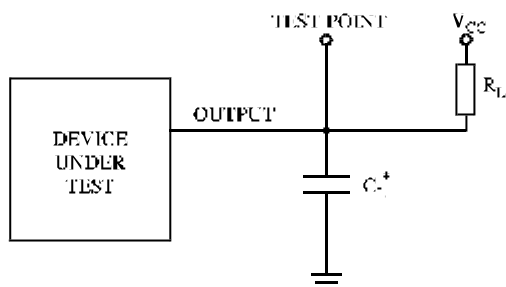


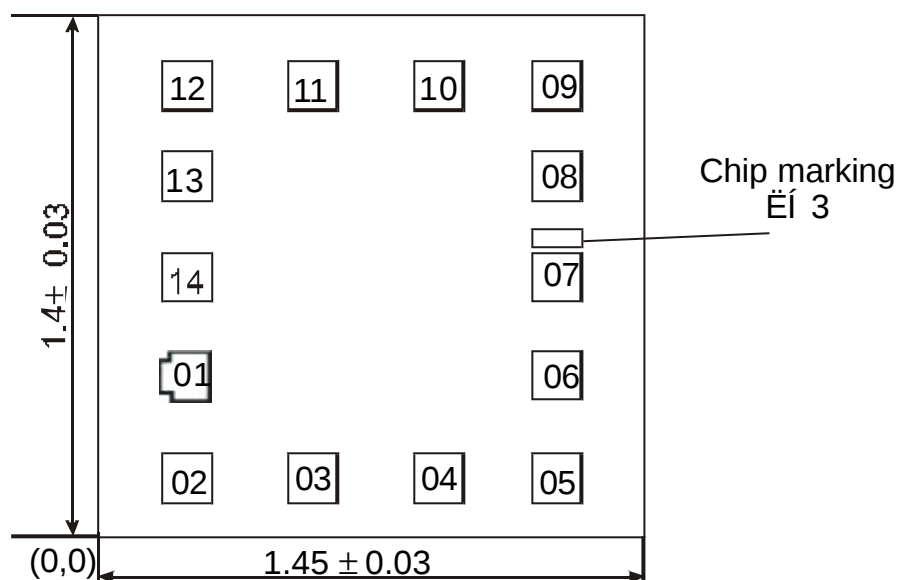
Figure 1. Switching Waveforms



\* Includes all probe and jig capacitance

Figure 2. Test Circuit

## CHIP PAD DIAGRAM IZ7406



Pad size 0.140 x 0.140 mm (Pad size is given as per metallization layer)

Thickness of chip 0,46±0,02 mm

## PAD LOCATION

| Pad No | Symbol          | X     | Y     |
|--------|-----------------|-------|-------|
| 01     | A1              | 0.090 | 0.380 |
| 02     | Y1              | 0.090 | 0.090 |
| 03     | A2              | 0.460 | 0.090 |
| 04     | Y2              | 0.830 | 0.090 |
| 05     | A3              | 1.220 | 0.090 |
| 06     | Y3              | 1.220 | 0.380 |
| 07     | GND             | 1.220 | 0.630 |
| 08     | Y4              | 1.220 | 0.880 |
| 09     | A4              | 1.220 | 1.170 |
| 10     | Y5              | 0.830 | 1.170 |
| 11     | A5              | 0.460 | 1.170 |
| 12     | Y6              | 0.090 | 1.170 |
| 13     | A6              | 0.090 | 0.880 |
| 14     | V <sub>CC</sub> | 0.090 | 0.630 |