SBAS344A − AUGUST 2005 − REVISED SEPTEMBER 2005

16-Bit, 10MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- High-Speed, Wide Bandwidth ΔΣ ADC
- 10MSPS Output Data Rate
- 4.9MHz Signal Bandwidth
- 86dBFS Signal-to-Noise Ratio
- −94dB Total Harmonic Distortion
- 95dB Spurious-Free Dynamic Range
- On-Chip Digital Filter Simplifies Anti-Alias Requirements
- $\overline{\text{SYNC}}$ Pin for Simultaneous Sampling with Multiple ADS1610s
- Low 3μs Group Delay
- Parallel Interface
- Directly Connects to TMS320 DSPs
- Out-of-Range Alert Pin
- Pin-Compatible with ADS1605 (5MSPS ADC)

APPLICATIONS

- Scientific Instruments
- Test Equipment
- Communications

DESCRIPTION

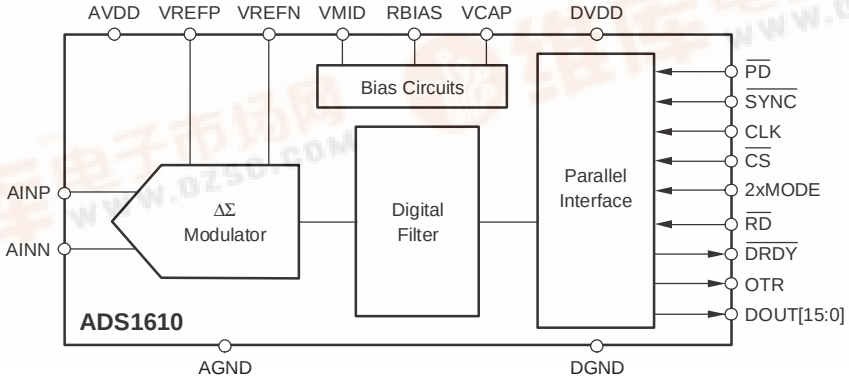
The ADS1610 is a high-speed, high-precision, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with 16-bit resolution operating from a +5V analog and a +3V digital supply. Featuring an advanced multi-stage analog modulator combined with an on-chip digital decimation filter, the ADS1610 achieves 86dBFS signal-to-noise ratio (SNR) in a 5MHz signal bandwidth. The device offers outstanding performance at these speeds with a total harmonic distortion of −94dB.

The ADS1610 ΔΣ topology provides key system-level design advantages with respect to anti-alias filtering and clock jitter. The design of the anti-alias filter is simplified since the on-chip digital filter greatly attenuates out-of-band signals. The ADS1601s filter has a *brick wall* response with a very flat passband (±0.0002dB of ripple) followed immediately by a very wide stop band (5MHz to 55MHz). Clock jitter becomes especially critical when digitizing high frequency, large-amplitude signals. The ADS1610 significantly reduces clock jitter sensitivity by an effective averaging of clock jitter as a result of oversampling the input signal.

Output data is supplied over a parallel interface and easily connects to TMS320 digital signal processors (DSPs). The power dissipation can be adjusted with an external resistor, allowing for reduction at lower operating speeds.

With its outstanding high-speed performance, the ADS1610 is well-suited for demanding applications in data acquisition, scientific instruments, test and measurement equipment, and communications. The ADS1610 is offered in a TQFP-64 package and is specified from −40°C to +85°C.

PRODUCT PREVIEW



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1610	UNIT
AVDD to AGND	−0.3 to +6	V
DVDD to DGND	−0.3 to +3.6	V
AGND to DGND	−0.3 to +0.3	V
Input Current	100mA, Momentary	
Input Current	10mA, Continuous	
Analog I/O to AGND	−0.3 to AVDD + 0.3	V
Digital I/O to DGND	−0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	−40 to +105	°C
Storage Temperature Range	−60 to +150	°C
Lead Temperature (soldering, 10s)	+260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

All specifications at −40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = +3V, 2xMODE = low, V_{CM} = 2.5V, and RBIAS = 18kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1610 MIN	ADS1610 TYP	ADS1610 MAX	UNIT
Analog Input					
Differential input voltage (V_{IN}) (AINP − AINN)			$\pm V_{REF}$		V
Common-mode input voltage (V_{CM}) (AINP + AINN)/2			2.5		V
Absolute input voltage (AINP or AINN with respect to AGND)		−0.1		4.2	V
Dynamic Specifications					
Data rate			$10\left(\frac{f_{CLK}}{60MHz}\right)$		MSPS
Signal-to-noise ratio (SNR)	f_{SIG} = 100kHz, −2dBFS		86		dBFS
	f_{SIG} = 1MHz, −2dBFS		85		dBFS
	f_{SIG} = 4MHz, −2dBFS		85		dBFS
Total harmonic distortion (THD)	f_{SIG} = 100kHz, −2dBFS		−90		dB
	f_{SIG} = 100kHz, −6dBFS		−95		dB
	f_{SIG} = 100kHz, −20dBFS		−95		dB
	f_{SIG} = 1MHz, −2dBFS		−89		dB
	f_{SIG} = 1MHz, −6dBFS		−93		dB
	f_{SIG} = 1MHz, −20dBFS		−95		dB
	f_{SIG} = 4MHz, −2dBFS		−109		dB
	f_{SIG} = 4MHz, −6dBFS		−105		dB
	f_{SIG} = 4MHz, −20dBFS		−95		dB
Signal-to-noise and distortion (SINAD)	f_{SIG} = 100kHz, −2dBFS		85		dBFS
	f_{SIG} = 1MHz, −2dBFS		84		dBFS
	f_{SIG} = 4MHz, −2dBFS		85		dBFS
Spurious-free dynamic range (SFDR)	f_{SIG} = 100kHz, −2dBFS		90		dB
	f_{SIG} = 100kHz, −6dBFS		96		dB
	f_{SIG} = 100kHz, −20dBFS		96		dB
	f_{SIG} = 1MHz, −2dBFS		91		dB
	f_{SIG} = 1MHz, −6dBFS		93		dB
	f_{SIG} = 1MHz, −20dBFS		96		dB
	f_{SIG} = 4MHz, −2dBFS		109		dB
	f_{SIG} = 4MHz, −6dBFS		105		dB
	f_{SIG} = 4MHz, −20dBFS		95		dB
Intermodulation distortion	f_1 = 3.8MHz, −8dBFS f_2 = 4MHz, −8dBFS		TBD		dB
Aperture jitter	Excludes jitter of CLK source		2		ps, rms
Aperture delay			4		ns

PRODUCT PREVIEW

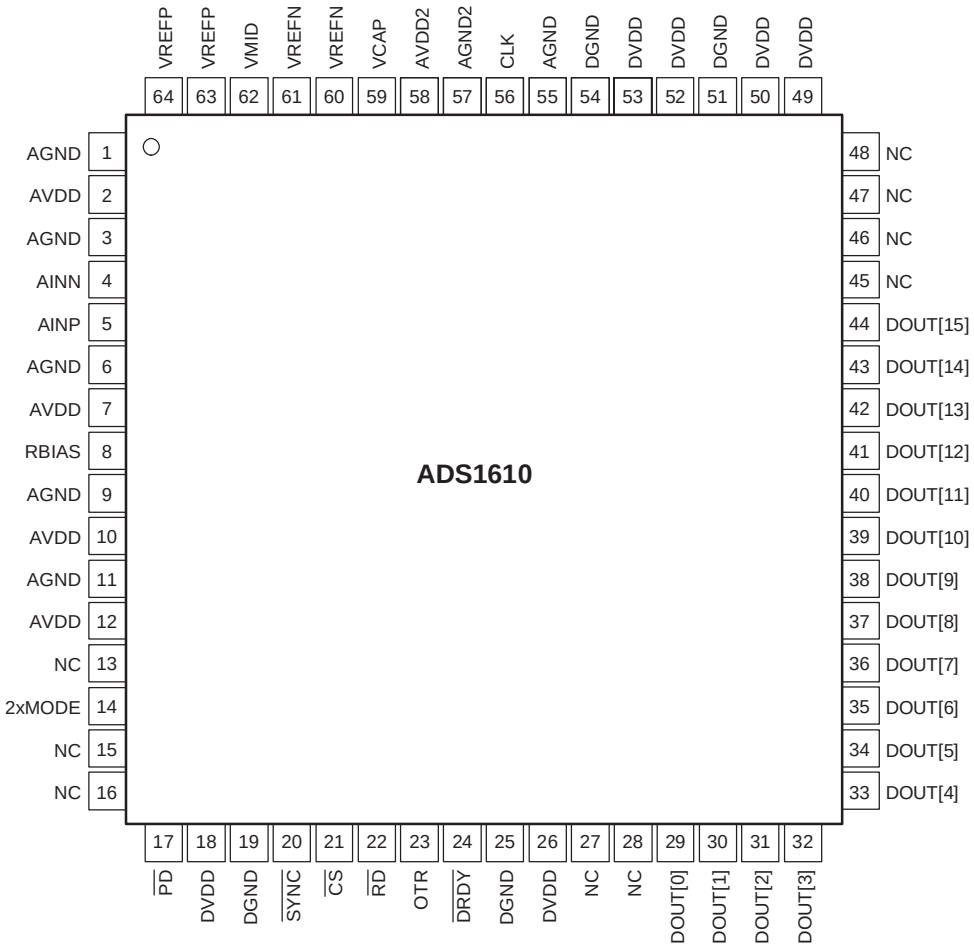
ELECTRICAL CHARACTERISTICS (continued)

All specifications at −40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = +3V, 2xMODE = low, V_{CM} = 2.5V, and RBIAS = 18kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1610 MIN	ADS1610 TYP	ADS1610 MAX	UNIT
Digital Filter Characteristics					
Passband		0		$4.4\left(\frac{f_{CLK}}{60MHz}\right)$	MHz
Passband ripple				±0.0002	dB
Passband transition	−0.1dB attenuation		$4.6\left(\frac{f_{CLK}}{60MHz}\right)$		MHz
	−3.0dB attenuation		$4.9\left(\frac{f_{CLK}}{60MHz}\right)$		MHz
Stop band		5.6		54.4	MHz
Stop band attenuation		80	(see Figure 14)		dB
Group delay			$3.0\left(\frac{60MHz}{f_{CLK}}\right)$		µs
Settling time	To ±0.001%		5.5		µs
Static Specifications					
Resolution	No missing codes	16			Bits
Input referred noise			TBD		µV, rms
Integral nonlinearity	End-point fit, −2dBFS signal		±0.75		LSB
Differential nonlinearity			±0.5		LSB
Offset error	T = +25°C		TBD		mV
Offset drift			TBD		µV/°C
Gain error	T = +25°C		TBD		%
Gain drift	Excluding reference drift		TBD		ppm/°C
Common-mode rejection	At DC		TBD		dB
Power-supply rejection	At DC		TBD		dB
Voltage Reference					
V_{REF} (VREFP − VREFN)		2.9	3.0	3.1	V
VREFP		3.6	4.0	4.4	V
VREFN		0.9	1.0	1.1	V
VMID		2.2	2.5	3.8	V
Digital Input/Output					
V_{IH}		0.7 DVDD		DVDD	V
V_{IL}		DGND		0.3 DVDD	V
V_{OH}	I_{OH} = −50µA	0.8 DVDD			V
V_{OL}	I_{OL} = 50µA			0.2 DVDD	V
Input leakage	DGND < $V_{DIGITAL\ INPUT}$ < DVDD			±10	µA
Power-Supply Requirements					
AVDD		4.9	5.0	5.1	V
DVDD		2.7	3.0	3.6	V
AVDD current			150		mA
DVDD current			70		mA
Power dissipation			960		mW

PIN CONFIGURATION

Top View **HTQFP**



PRODUCT PREVIEW

PIN FUNCTION DESCRIPTION

PIN NAME	PIN #	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
AGND	1, 3, 6, 9, 11, 55	Analog	Analog Ground
AVDD	2, 7, 10, 12	Analog	Analog Supply
AINN	4	Analog Input	Negative Analog Input
AINP	5	Analog Input	Positive Analog Input
RBIAS	8	Analog	Analog Bias Setting Resistor
NC	13, 15, 16, 27, 28, 45-48	—	Must be left unconnected.
2xMODE	14	Digital Input; Active High	2xMODE (20MSPS)
$\overline{PD}$	17	Digital Input; Active Low	Power-Down
DVDD	18, 26, 49, 50, 52, 53	Digital	Digital Supply
DGND	19, 25, 51, 54	Digital	Digital Ground
$\overline{SYNC}$	20	Digital Input; Active Low	Digital Reset
$\overline{CS}$	21	Digital Input; Active Low	Chip-Select
$\overline{RD}$	22	Digital Input; Active Low	Read Enable
OTR	23	Digital Output	Analog Inputs Out-Of-Range
$\overline{DRDY}$	24	Digital Output	Data Ready
DOUT[15:0]	29-44	Digital Output	Data Output. DOUT[15] is the MSB and DOUT[0] is the LSB.
CLK	56	Digital Input	Clock Input
AGND2	57	Analog	Analog Ground for AVDD2
AVDD2	58	Analog	Analog Supply for Modulator Clocking
VCAP	59	Analog	Bypass Capacitor
VREFN	60, 61	Analog	Negative Reference Voltage
VMID	62	Analog	Midpoint Voltage
VREFP	63, 64	Analog	Positive Reference Voltage

TIMING SPECIFICATIONS

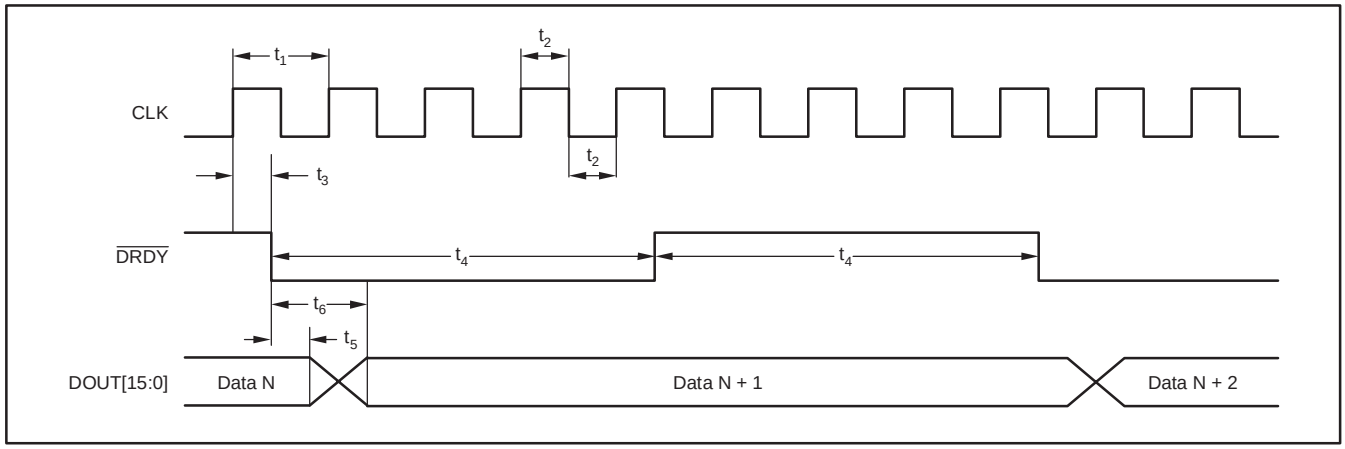


Figure 1. Data Retrieval Timing

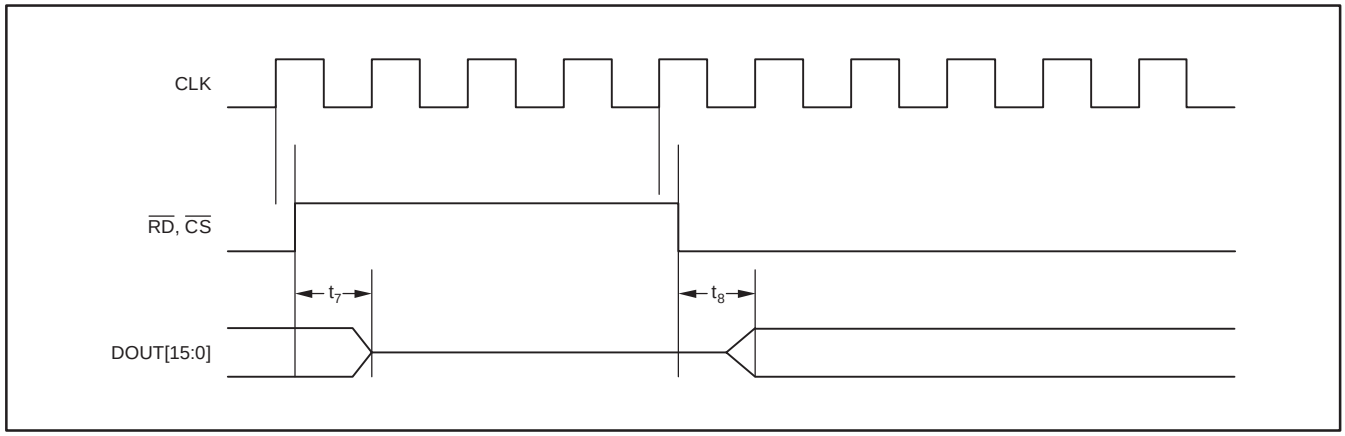


Figure 2. DOUT Inactive/Active Timing

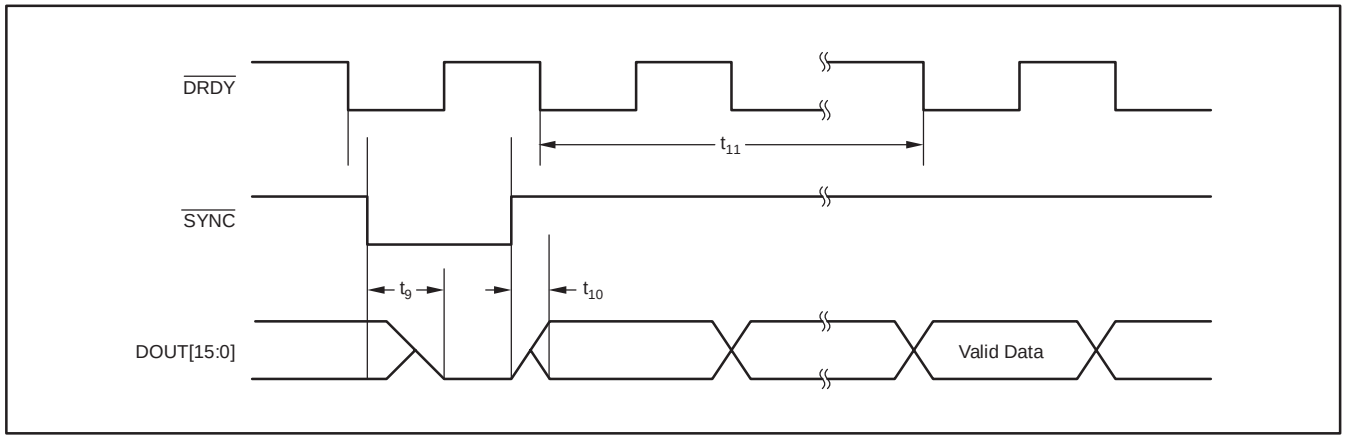


Figure 3. Reset Timing

PRODUCT PREVIEW

Timing Specifications

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	CLK Period ($1/f_{CLK}$)	TBD	16.667		ns
$1/t_1$	f_{CLK}		60	TBD	MHz
t_2	CLK Pulse Width, High or Low	TBD			ns
t_3	CLK to $\overline{DRDY}$ High (propagation delay)		10		ns
t_4	$\overline{DRDY}$ Pulse Width, High or Low		$4\ t_1$		ns
t_5	Previous Data Valid (hold time)	TBD			ns
t_6	New Data Valid (setup time)			TBD	ns
t_7	First Rising Edge CLK After $\overline{RD}$ and/or $\overline{CS}$ Inactive (high) to DOUT High Impedance		TBD		ns
t_8	First Rising Edge CLK After $\overline{RD}$ and/or $\overline{CS}$ Active (low) to DOUT Active		TBD		ns
t_9	Delay from $\overline{SYNC}$ Active (low) to All-Zero DOUT[15:0]		TBD		ns
t_{10}	Delay from $\overline{SYNC}$ Inactive (high) to Non-Zero DOUT[15:0]			TBD	ns
t_{11}	Delay from Non-Zero DOUT[15:0] to Valid DOUT[15:0] (time – 55 $\overline{DRDY}$ cycles; required for digital filter to settle).		5.5		µs

(1) Output load = 10pF ||500kΩ.

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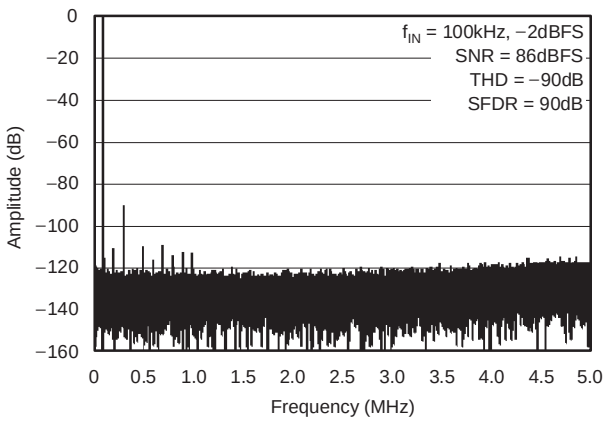
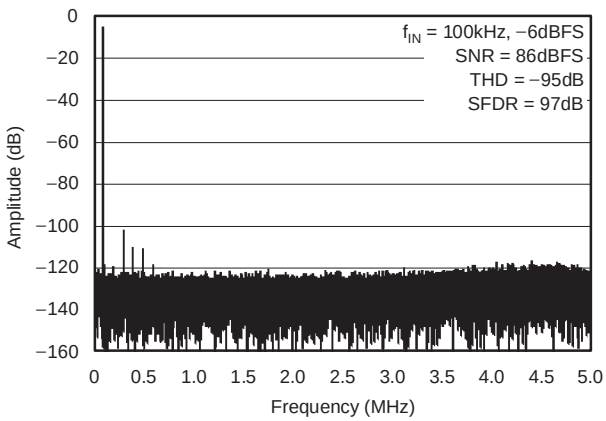
TYPICAL CHARACTERISTICS

At T_A = +25°C, R_{BIAS} = 18kΩ, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, and V_{CM} = 2.5V, unless otherwise noted.

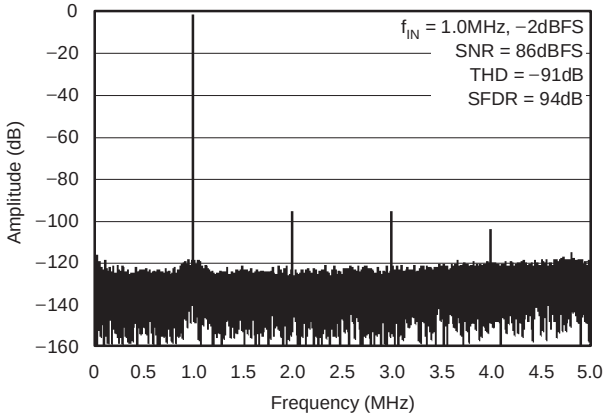
SPECTRAL RESPONSE



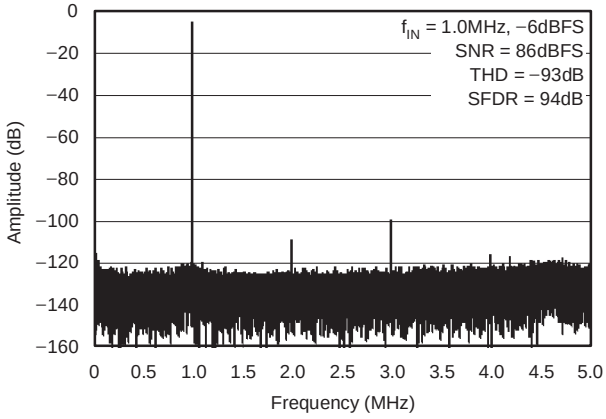
SPECTRAL RESPONSE



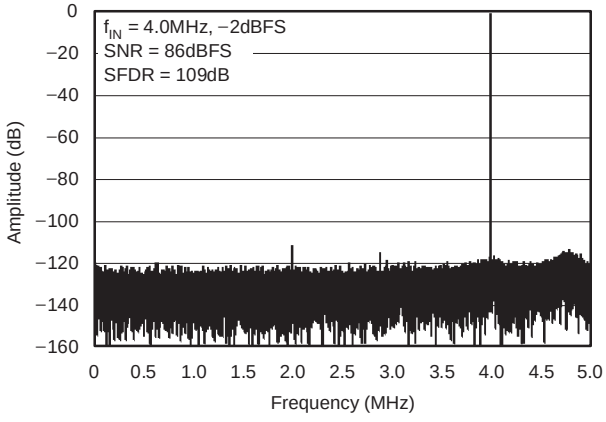
SPECTRAL RESPONSE



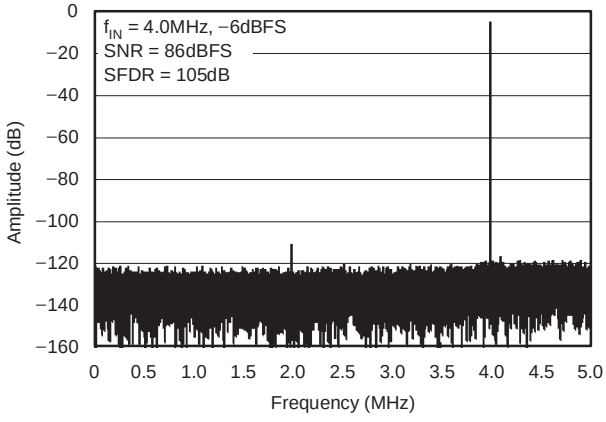
SPECTRAL RESPONSE



SPECTRAL RESPONSE



SPECTRAL RESPONSE

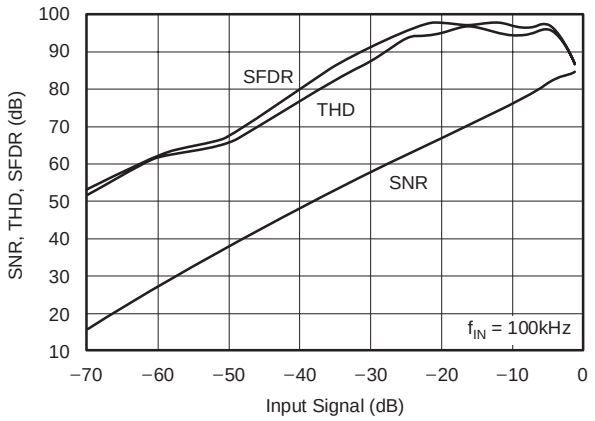


PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_{BIAS} = 18kΩ, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, and V_{CM} = 2.5V, unless otherwise noted.

SIGNAL−TO−NOISE RATIO,
TOTAL HARMONIC DISTORTION, AND
SPURIOUS−FREE DYNAMIC RANGE vs INPUT
SIGNAL AMPLITUDE



PRODUCT PREVIEW

OVERVIEW

The ADS1610 is a high-performance, delta-sigma ADC. The modulator uses an inherently stable, pipelined, delta-sigma modulator architecture incorporating proprietary circuitry that allows for very linear high-speed operation. The modulator samples the input signal at 60MSPS (when f_{CLK} = 60MHz). A low-ripple linear phase digital filter decimates the modulator output by 6 to provide data output word rates of 10MSPS with a signal passband out to 4.9MHz. The *double speed* mode, enabled by digital I/O pin 2xMODE, doubles the data rate to 20MSPS by reducing the oversampling ratio to 3. See the *2x Mode* section on page 19 for more detail.

Conceptually, the modulator and digital filter measure the differential input signal, V_{IN} = (AINP − AINN), against the differential reference, V_{REF} = (VREFP − VREFN), as shown in Figure 4. A 16-bit parallel data bus, designed for direct connection to DSPs, outputs the data. A separate power supply for the I/O allows flexibility for interfacing to different logic families. Out-of-range conditions are indicated with a dedicated digital output pin. Analog power dissipation is controlled using an external resistor. This allows reduced dissipation when operating at slower speeds. When not in use, power consumption can be dramatically reduced using the $\overline{PD}$ pin.

ANALOG INPUTS (AINP, AINN)

The ADS1610 measures the differential signal, V_{IN} = (AINP − AINN), against the differential reference, V_{REF} = (VREFP − VREFN).

The ADS1610 supports a very wide range of input signals. Having such a wide input range makes out-of-range signals unlikely. However, should an out-of-range signal occur, the digital output OTR will go high.

To achieve the highest analog performance, it is recommended that the inputs be limited to $0.891V_{REF}$ (−1dBFS). For V_{REF} = 3V, the corresponding recommended input range is ±2.67.

The analog inputs must be driven with a differential signal to achieve optimum performance. The recommended common-mode voltage of the input signal, $V_{CM} = \frac{AINP + AINN}{2}$, is 2.5V.

In addition to the differential and common-mode input voltages, the absolute input voltage is also important. This is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

$$-0.1V < (AINN \text{ or } AINP) < 4.2V \quad (1)$$

If either input is taken below −0.1V, ESD protection diodes on the inputs will turn on. Exceeding 4.2V on either input will result in linearity performance degradation. ESD protection diodes will also turn on if the inputs are taken above AVDD (+5V).

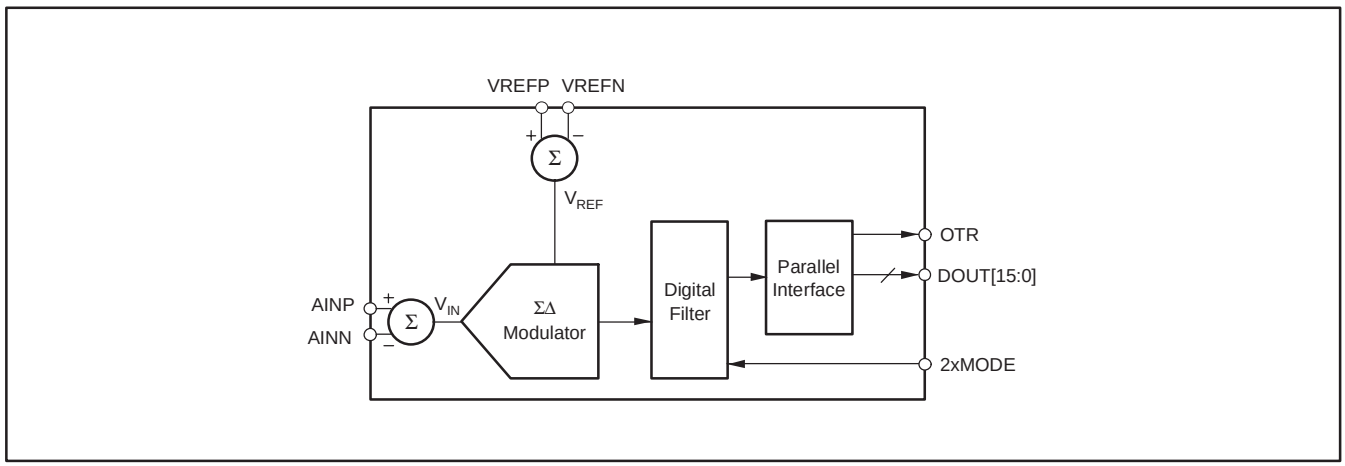


Figure 4. Conceptual Block Diagram

PRODUCT PREVIEW

INPUT CIRCUITRY

The ADS1610 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged internally with this cycle repeating at the frequency of CLK. Figure 5 shows a conceptual diagram of these circuits. Switches S_2 represent the net effect of the modulator circuitry in discharging the sampling capacitors, the actual implementation is different. The timing for switches S_1 and S_2 is shown in Figure 6.

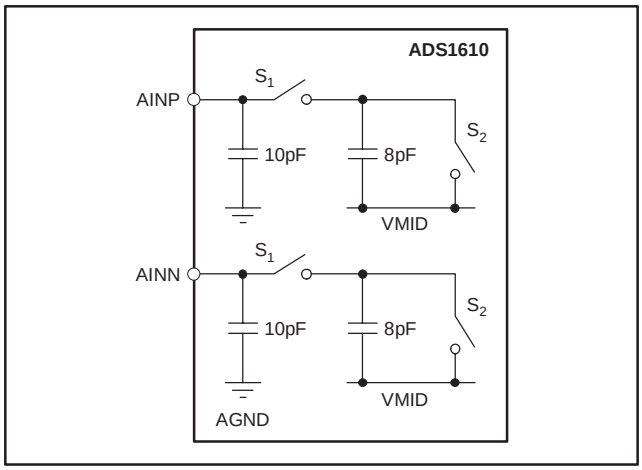


Figure 5. Conceptual Diagram of Internal Circuitry Connected to the Analog Inputs

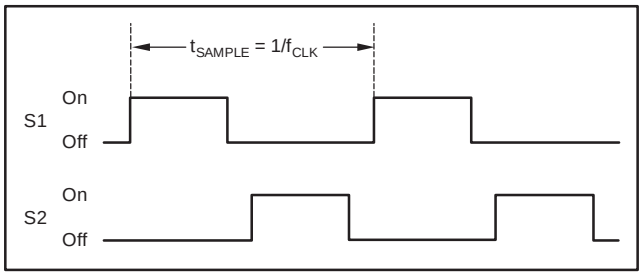


Figure 6. Timing for the Switches in Figure 2

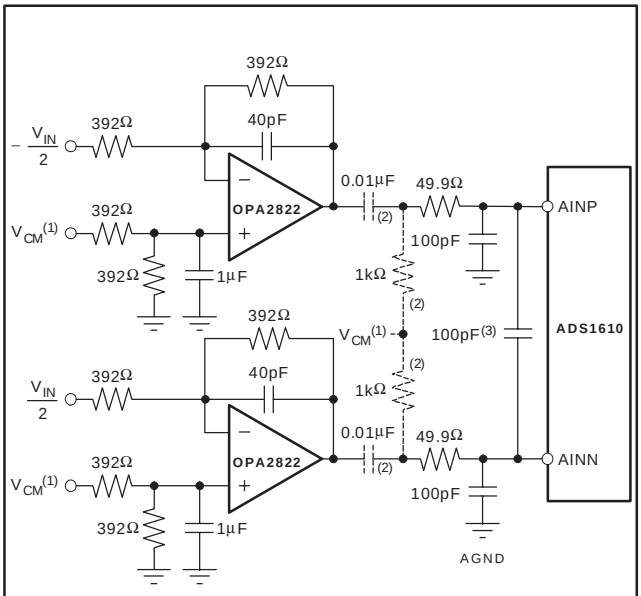
DRIVING THE INPUTS

The external circuits driving the ADS1610 inputs must be able to handle the load presented by the switching capacitors within the ADS1610. The input switches S1 in Figure 5 are closed approximately one half of the sampling period, t_{SAMPLE}, allowing only ~8ns for the internal capacitors to be charged by the inputs, when f_{CLK} = 60MHz.

Figure 7 and Figure 8 show the recommended circuits when using single-ended or differential op amps, respectively. The analog inputs must be driven differentially to achieve optimum performance. If only a single-ended input signal is available, the configuration in Figure 8 can be used by shorting $-V_{IN}$ to ground.

This configuration would implement the single-ended to differential conversion.

The external capacitors, between the inputs and from each input to AGND, improve linearity and should be placed as close to the pins as possible. Place the drivers close to the inputs and use good capacitor bypass techniques on their supplies; usually a smaller high-quality ceramic capacitor in parallel with a larger capacitor. Keep the resistances used in the driver circuits low-thermal noise in the driver circuits degrades the overall noise performance. When the signal can be AC-coupled to the ADS1610 inputs, a simple RC filter can set the input common mode voltage. The ADS1610 is a high-speed, high-performance ADC. Special care must be taken when selecting the test equipment and setup used with this device. Pay particular attention to the signal sources to ensure they do not limit performance when measuring the ADS1610.



(1) Recommended V_{CM} = 2.5V.
(2) Optional ac-coupling circuit provides common-mode input voltage.
(3) Increase to 390pF when $f_{IN} \leq$ 100kHz for improved SNR and THD.

Figure 7. Recommended Driver Circuit Using the OPA2822

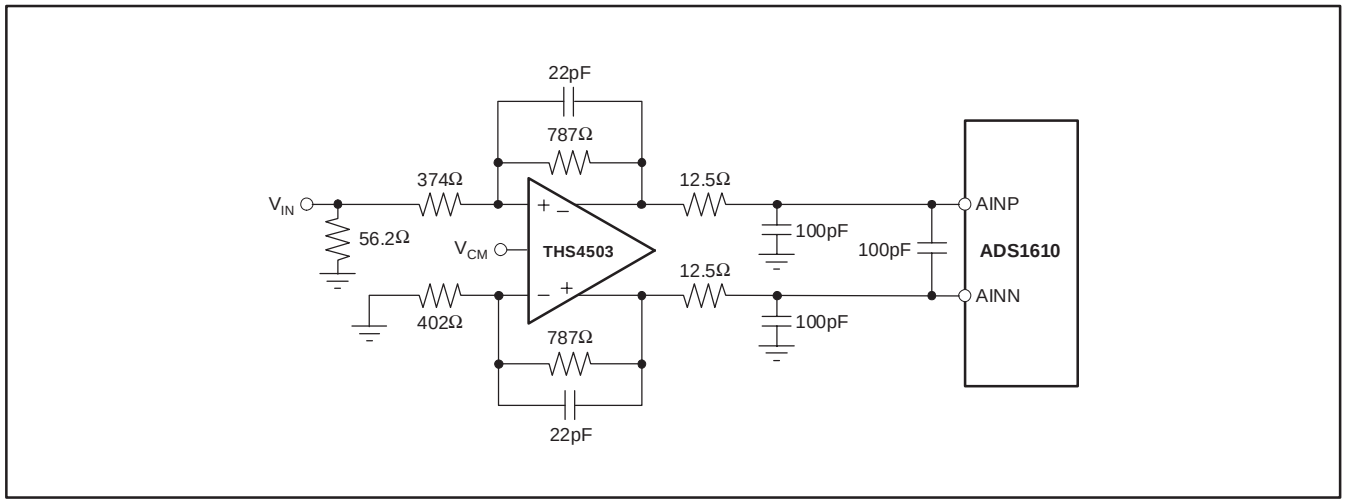


Figure 8. Recommended Single-Ended to Differential Conversion Circuit Using the THS4503 Differential Amplifier

REFERENCE INPUTS (VREFN, VREFP, VMID)

The ADS1610 operates from an external voltage reference. The reference voltage V_{REF} is set by the differential voltage between VREFN and VREFP: V_{REF} = (VREFP − VREFN). VREFP and VREFN each use two pins, which should be shorted together. VMID equals approximately 2.5V and is used by the modulator. VCAP connects to an internal node and must also be bypassed with an external capacitor.

The voltages applied to these pins must be within the values specified in the Electrical Characteristics table. Typically VREFP = 4V, VMID = 2.5V, and VREFN = 1V. The external circuitry must be capable of providing both a DC and a transient current. Figure 9 shows a simplified diagram of the internal circuitry of the reference. As with the input circuitry, switches S_1 and S_2 open and close as shown in Figure 6.

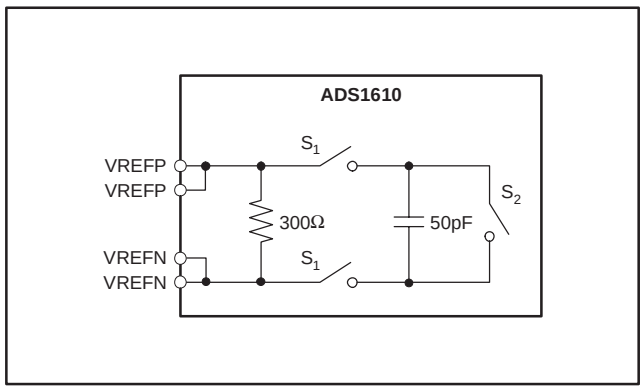


Figure 9. Conceptual Circuitry for the Reference Inputs

Figure 10 shows the recommended circuitry for driving these reference inputs. Keep the resistances used in the buffer circuits low to prevent excessive thermal noise from degrading performance. Layout of these circuits is critical, make sure to follow good high-speed layout practices. Place the buffers and especially the bypass capacitors as close to the pins as possible.

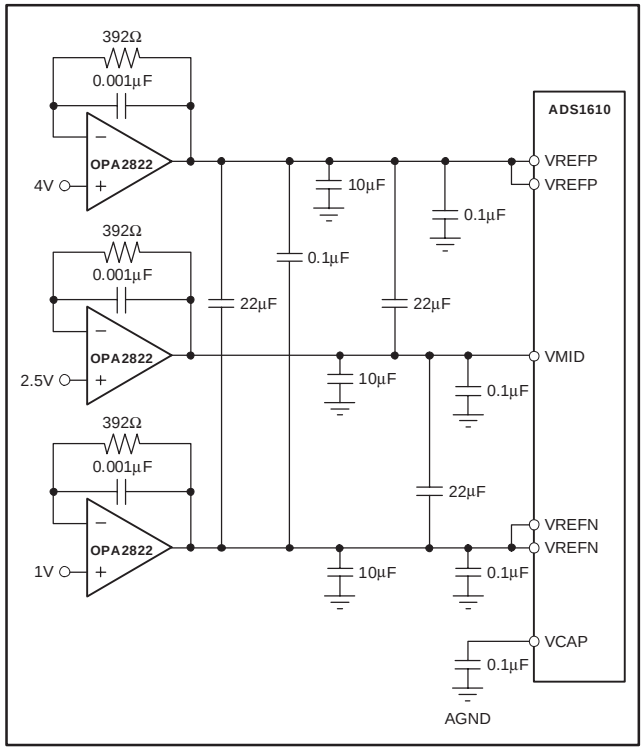


Figure 10. Recommended Reference Buffer Circuit

PRODUCT PREVIEW

CLOCK INPUT (CLK)

The ADS1610 uses an external clock signal to be applied to the CLK input pin. The sampling of the modulator is controlled by this clock signal. As with any high-speed data converter, a high quality clock is essential for optimum performance. Crystal clock oscillators are the recommended CLK source; other sources, such as frequency synthesizers are usually not adequate. Make sure to avoid excess ringing on the CLK input; keeping the trace as short as possible will help.

Measuring high-frequency, large-amplitude signals requires tight control of clock jitter. The uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. This effect becomes more pronounced with higher frequency and larger magnitude inputs. Fortunately, the ADS1610 oversampling topology reduces clock jitter sensitivity over that of Nyquist rate converters like pipeline and successive approximation converters by a factor of $\sqrt{6}$.

In order to not limit the ADS1610 SNR performance, keep the jitter on the clock source below the values shown in Table 1. When measuring lower frequency and lower amplitude inputs, more CLK jitter can be tolerated. In determining the allowable clock source jitter, select the worst-case input (highest frequency, largest amplitude) that will be seen in the application.

DATA FORMAT

The 16-bit output data is in binary two's complement format, as shown in Table 2. When the input is positive out-of-range, exceeding the positive full-scale value of V_{REF}, the output clips to all $7FFF_H$ and the OTR output goes high.

Table 1. Maximum Allowable Clock Source Jitter for Different Input Signal Frequencies and Amplitude

INPUT SIGNAL		MAXIMUM ALLOWABLE CLOCK SOURCE JITTER
MAXIMUM FREQUENCY	MAXIMUM AMPLITUDE	
4MHz	−1dB	1.6ps
4MHz	−20dB	14ps
2MHz	−1dB	3.3ps
2MHz	−20dB	29ps
1MHz	−1dB	6.5ps
1MHz	−20dB	58ps
100kHz	−1dB	65ps
100kHz	−20dB	581ps

Table 2. Output Code Versus Input Signal

INPUT SIGNAL (INP – INN)	IDEAL OUTPUT CODE(1)	OTR
$\geq +V_{REF}$ (> 0dB)	$7FFF_H$	1
V_{REF} (0dB)	$7FFF_H$	0
$\frac{+V_{REF}}{2^{15} - 1}$	0001_H	0
0	0000_H	0
$\frac{-V_{REF}}{2^{15} - 1}$	$FFFF_H$	0
$-V_{REF}\left(\frac{2^{15}}{2^{15} - 1}\right)$	8000_H	0
$\leq -V_{REF}\left(\frac{2^{15}}{2^{15} - 1}\right)$	8000_H	1

(1) Excludes effects of noise, INL, offset and gain errors.

Likewise, when the input is negative out-of-range by going below the negative full-scale value of V_{REF}, the output clips to 8000h and the OTR output goes high. The OTR remains high while the input signal is out-of-range.

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OUT-OF-RANGE INDICATION (OTR)

If the output code on DOUT[15:0] exceeds the positive or negative full-scale, the out-of-range digital output (OTR) will go high on the falling edge of $\overline{DRDY}$. When the output code returns within the full-scale range, OTR returns low on the falling edge of $\overline{DRDY}$.

DATA RETRIEVAL

Data retrieval is controlled through a simple parallel interface. The falling edge of the $\overline{DRDY}$ output indicates new data is available. To activate the output bus, both $\overline{CS}$ and $\overline{RD}$ must be low, as shown in Table 3. Make sure the DOUT bus does not drive heavy loads (> 20pF), as this will degrade performance. Use an external buffer when driving an edge connector or cables.

Table 3. Truth Table for $\overline{CS}$ and $\overline{RD}$

$\overline{CS}$	$\overline{RD}$	DOUT[15:0]
0	0	Active
0	1	High impedance
1	0	High impedance
1	1	High impedance

RESETTING THE ADS1610

The ADS1610 is asynchronously reset when the $\overline{SYNC}$ pin is taken low. During reset, all of the digital circuits are cleared, DOUT[15:0] are forced low, and $\overline{DRDY}$ forced high. It is recommended that the $\overline{SYNC}$ pin be released on the falling edge of CLK. Afterwards, $\overline{DRDY}$ goes low on the second rising edge of CLK. Allow 55 $\overline{DRDY}$ cycles for the digital filter to settle before retrieving data. See Figure 3 for the timing specifications.

Reset can be used to synchronize multiple ADS1610s. All devices to be synchronized must use a common CLK input. With the CLK inputs running, pulse $\overline{SYNC}$ on the falling edge of CLK, as shown in Figure 11. Afterwards, the converters will be converting synchronously with the $\overline{DRDY}$ outputs updating simultaneously. After synchronization, allow 55 $\overline{DRDY}$ cycles (t_{12}) for output data to fully settle.

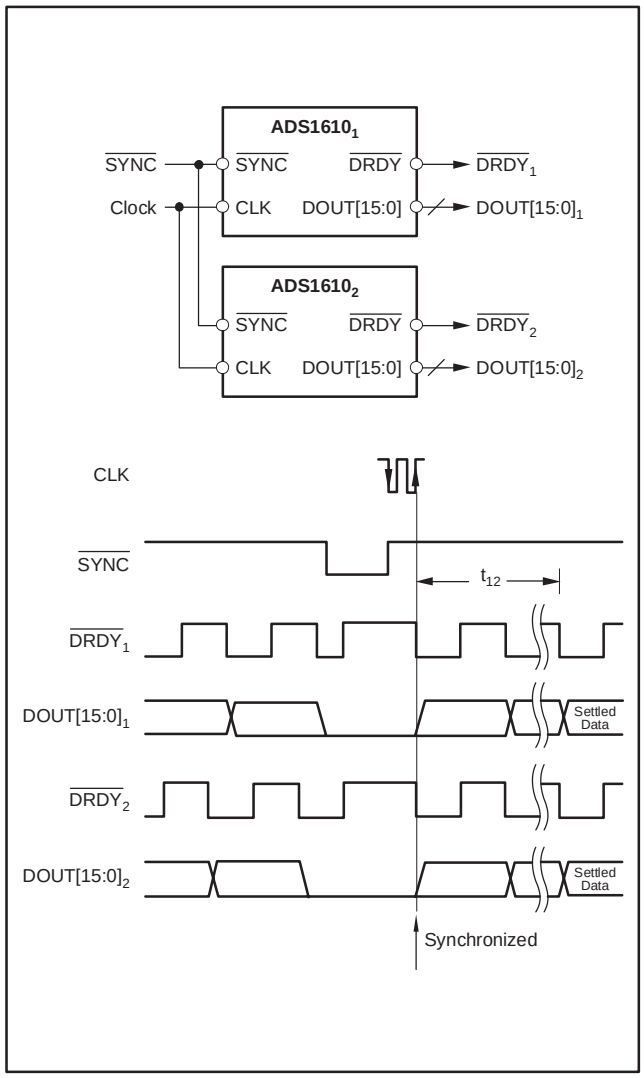

Figure 11. Synchronizing Multiple Converters

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SETTLING TIME

The settling time is an important consideration when measuring signals with large steps or when using a multiplexer in front of the analog inputs. The ADS1610 digital filter requires time for an instantaneous change in signal level to propagate to the output.

Be sure to allow the filter time to settle after applying a large step in the input signal, switching the channel on a multiplexer placed in front of the inputs, resetting the ADS1610, or exiting the power-down mode.

Figure 12 shows the settling error as a function of time for a full-scale signal step applied at t = 0, with 2xMODE = low. This figure uses $\overline{\text{DRDY}}$ cycles for the ADS1610 for the time scale (X-axis). After 55 $\overline{\text{DRDY}}$ cycles, the settling error drops below 0.001%. For f_{CLK} = 60MHz, this corresponds to a settling time of 5.5µs.

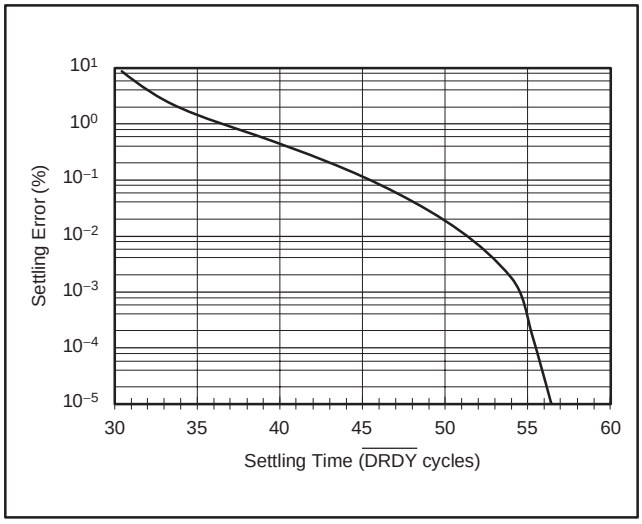

Figure 12. Settling Time

IMPULSE RESPONSE

Figure 13 plots the normalized response for an input applied at t = 0, with 2xMODE = low. The X-axis units of time are $\overline{\text{DRDY}}$ cycles for the ADS1610. As shown in Figure 13, the peak of the impulse takes 30 $\overline{\text{DRDY}}$ cycles to propagate to the output. For f_{CLK} = 60MHz, a $\overline{\text{DRDY}}$ cycle is 0.1µs in duration and the propagation time (or group delay) is 30 × 0.1µs = 3.0µs.

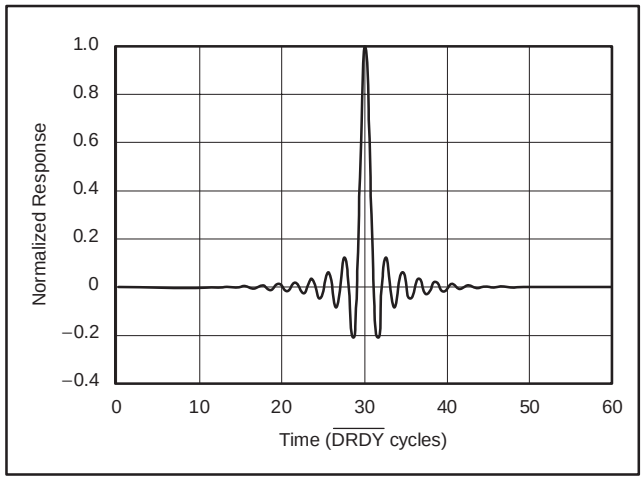

Figure 13. Impulse Response

FREQUENCY RESPONSE

The linear phase FIR digital filter sets the overall frequency response. The decimation rate is set to 6 (2xMODE = low) for all the figures shown in this section. Figure 14 shows the frequency response from DC to 30MHz for f_{CLK} = 60MHz. The frequency response of the ADS1610 filter scales directly with CLK frequency. For example, if the CLK frequency is decreased by half (to 30MHz), the values on the X-axis in Figure 14 would need to be scaled by half, with the span becoming DC to 15MHz.

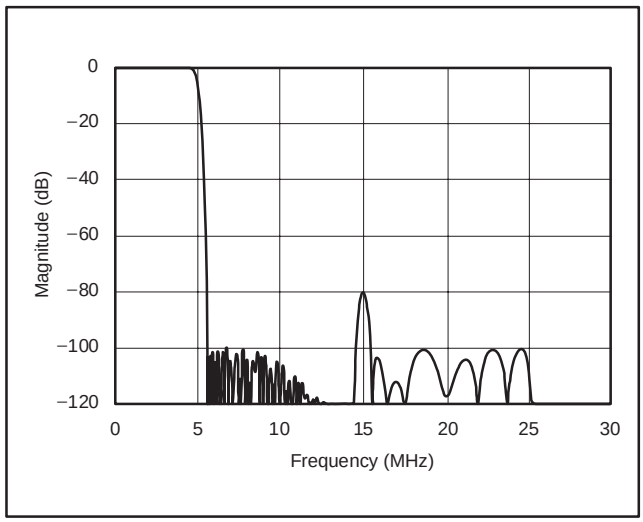

Figure 14. Frequency Response

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Figure 15 shows the passband ripple from DC to 4.4MHz (f_{CLK} = 60MHz). Figure 16 shows a closer view of the passband transition by plotting the response from 4.0MHz to 5.0MHz (f_{CLK} = 60MHz).

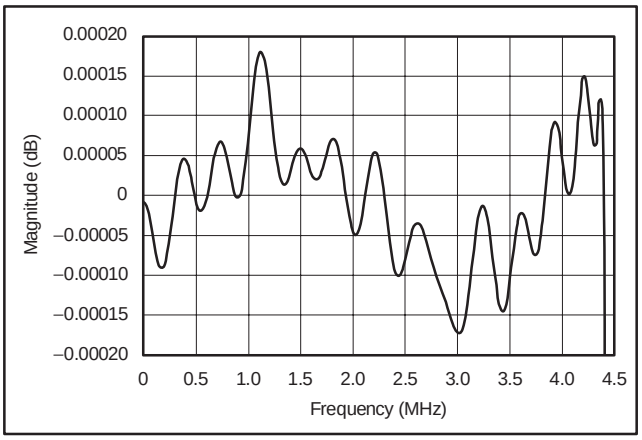

Figure 15. Passband Ripple

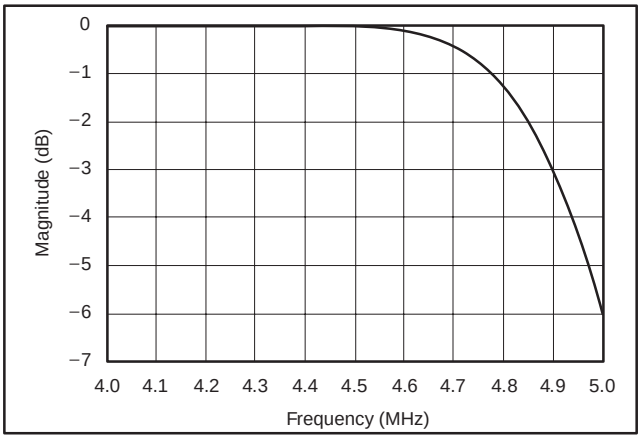

Figure 16. Passband Transition

The overall frequency response repeats at multiples of the CLK frequency. To help illustrate this, Figure 17 shows the response out to 180MHz (f_{CLK} = 60MHz). Notice how the passband response repeats at 60MHz, 120MHz, and 180MHz; it is important to consider this sequence when there is high-frequency noise present with the signal. The modulator bandwidth extends to 100MHz. High-frequency noise around 60MHz and 120MHz will not be attenuated by either the modulator or the digital filter. This noise will alias back in; band and reduce the overall SNR performance unless it is filtered out prior to the ADS1610. To prevent this, place an anti-alias filter in front of the ADS1610 that rolls off before 55MHz.

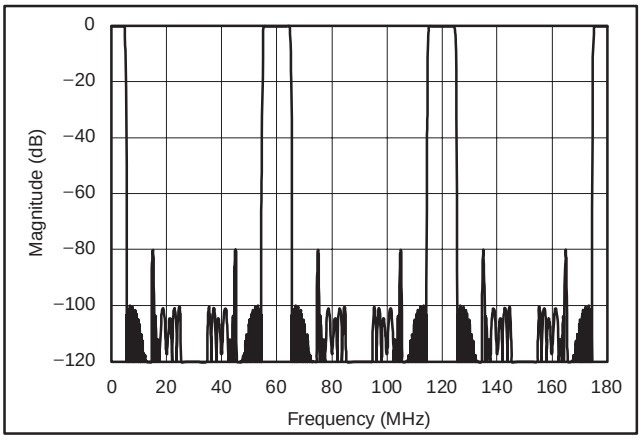

Figure 17. Frequency Response Out to 120MHz

ANALOG POWER DISSIPATION

An external resistor connected between the RBIAS pin and the analog ground sets the analog current level, as shown in Figure 18. The current is inversely proportional to the resistor value. Table 4 shows the recommended values of RBIAS for different CLK frequencies. Notice that the analog current can be reduced when using a slower frequency CLK input because the modulator has more time to settle. Avoid adding any capacitance in parallel to RBIAS, since this will interfere with the internal circuitry used to set the biasing.

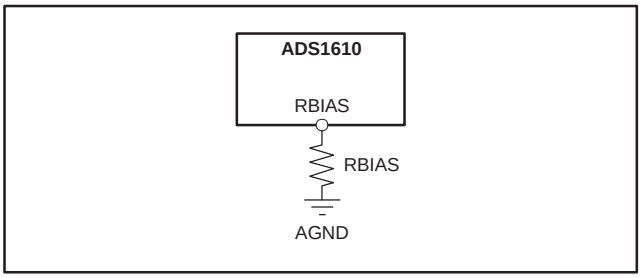

Figure 18. External Resistor Used to Set Analog Power Dissipation

Table 4. Recommended RBIAS Resistor Values for Different CLK Frequencies

f_{CLK}	DATA RATE	RBIAS	TYPICAL POWER DISSIPATION
42MHz	7MHz	TBD	TBD
48MHz	8MHz	TBD	TBD
54MHz	9MHz	TBD	TBD
60MHz	10MHz	18kΩ	960mW

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POWER-DOWN ($\overline{PD}$)

When not in use, the ADS1610 can be powered down by taking the $\overline{PD}$ pin low. All circuitry will be shutdown, including the voltage reference. To minimize the digital current during power down, stop the clock signal supplied to the CLK input. There is an internal pull-up resistor of 170kΩ on the $\overline{PD}$ pin, but it is recommended that this pin be connected to DVDD if not used. Make sure to allow time for the reference to start up after exiting the power-down mode. The internal reference typically requires 15µs. After the reference has stabilized, allow at least 100 $\overline{DRDY}$ cycles for the modulator and digital filter to settle before retrieving data.

POWER SUPPLIES

Two supplies are used on the ADS1610: analog (AVDD), and digital (DVDD). Each supply (other than DVDD pins 49 and 50) must be suitably bypassed to achieve the best performance. It is recommended that a 1µF and 0.1µF ceramic capacitor be placed as close to each supply pin as possible. Connect each supply-pin bypass capacitor to the associated ground, as shown in Figure 19. Each main supply bus should also be bypassed with a bank of capacitors from 47µF to 0.1µF, as shown in Figure 19.

For optimum performance, insert 10Ω at resistors in series with the AVDD2 supply (pin 58). This is the supply for the modulator clocking circuitry, and the resistor decouples switching glitches.

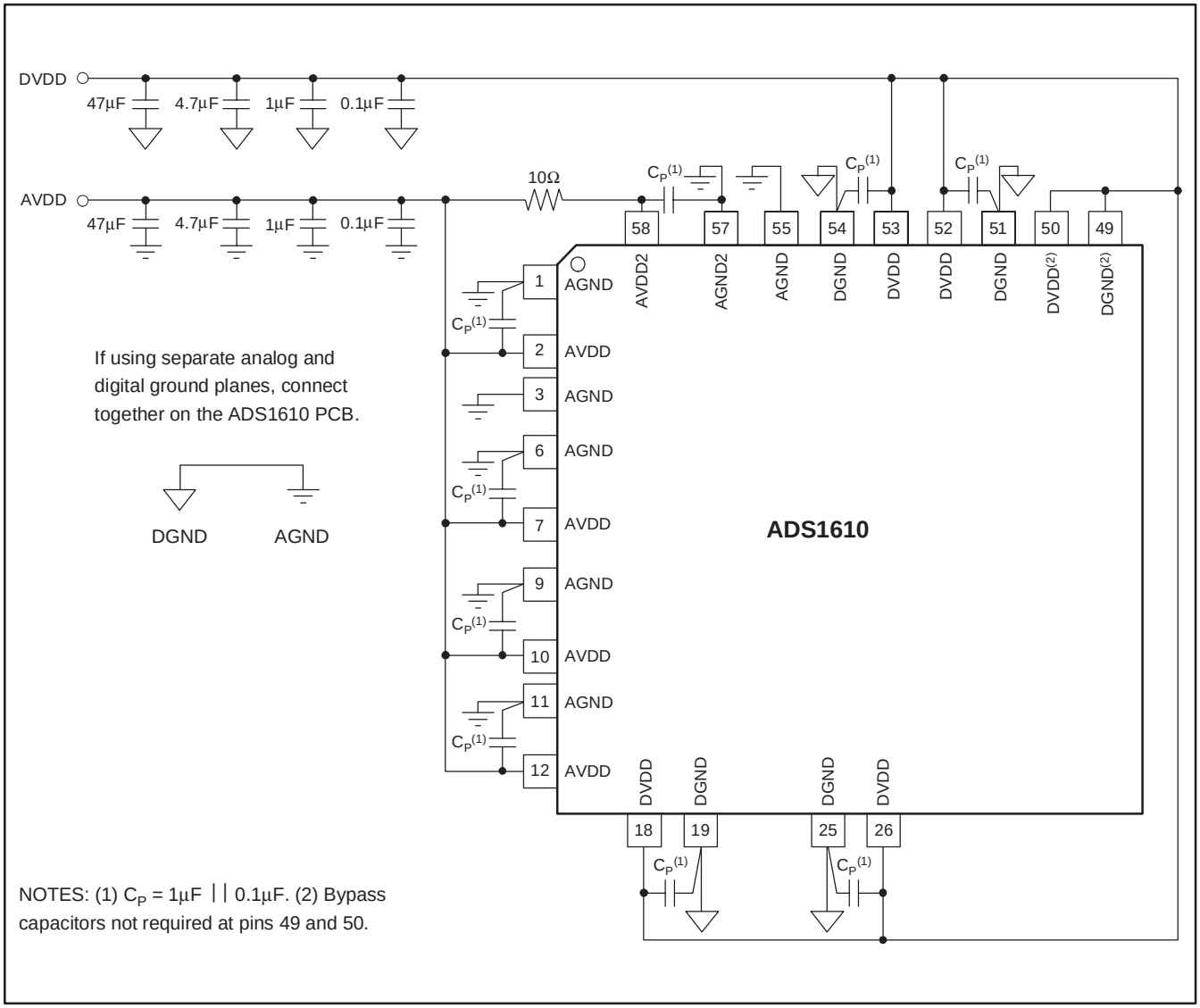

Figure 19. Recommended Power-Supply Bypassing

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2X MODE

The 2xMODE digital input determines the performance (16-bit or 14-bit) by setting the oversampling ratio. When 2xMODE = low, the oversampling ratio = 6 for 16-bit performance. When 2xMODE = high, the oversampling ratio = 3 for 14-bit performance. Note that when 2xMODE is high, all 16 bits of DOUT remain active. Decreasing the oversampling ratio from 8 to 3 doubles the data rate in 2x mode. For f_{CLK} = 60MHz, the data rate then becomes 20MSPS. In addition, the group delay decreases to 0.9µs and the settling time becomes 1.3µs or 13 $\overline{\text{DRDY}}$ cycles. With the reduced oversampling in 2x mode, the noise increases. Typical SNR performance degrades by 14dB. THD remains approximately the same. There is an internal pull-down resistor of 170kΩ on the 2xMODE; however, it is recommended that this pin be forced either high or low.

LAYOUT ISSUES

The ADS1610 is a very high-speed, high-resolution data converter. In order to achieve the maximum performance, careful attention must be given to the printed circuit board (PCB) layout. Use good high-speed techniques for all circuitry. Critical capacitors should be placed close to pins as possible. These include capacitors directly connected to the analog and reference inputs and the power supplies. Make sure to also properly bypass all circuitry driving the inputs and references.

Two approaches can be used for the ground planes: either a single common plane; or two separate planes, one for the analog grounds and one for the digital grounds. When using only one common plane, isolate the flow of current on AGND2 (pin 57) from pin 1; use breaks on the ground plane to accomplish this. AGND2 carries the switching current from the analog clocking for the modulator and can corrupt the quiet analog ground on pin 1. When using two planes, it is recommended that they be tied together right at the PCB. Do not try to connect the ground planes together after running separately through edge connectors or cables as this reduces performance and increases the likelihood of latch-up.

In general, keep the resistances used in the driving circuits for the inputs and reference low to prevent excess thermal noise from degrading overall performance. Avoid having the ADS1610 digital outputs drive heavy loads. Buffers on the outputs are recommended unless the ADS1610 is connected directly to a DSP or controller situated nearby. Additionally, make sure the digital inputs are driven with clean signals as ringing on the inputs can introduce noise.

The ADS1610 uses TI PowerPAD™ technology. The PowerPAD is physically connected to the substrate of the silicon inside the package and must be soldered to the analog ground plane on the PCB using the exposed metal pad underneath the package for proper heat dissipation. Please refer to application report SLMA002, located at www.ti.com, for more details on the PowerPAD package.

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APPLICATIONS INFORMATION

INTERFACING THE ADS1610 TO THE TMS320C6000

Figure 20 illustrates how to directly connect the ADS1610 to the TMS320C6000 DSP. The processor controls reading using output $\overline{ARE}$. The ADS1610 is selected using the DSP control output, $\overline{CE2}$. The ADS1610 16-bit data output bus is directly connected to the TMS320C6000 data bus. The data ready output ($\overline{DRDY}$) from the ADS1610 drives interrupt $\overline{EXT\_INT7}$ on the TMS320C6000.

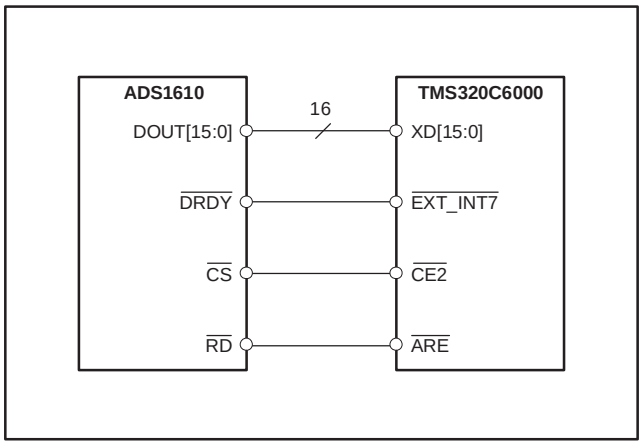

Figure 20. ADS1610—TMS320C6000 Interface Connection

INTERFACING THE ADS1610 TO THE TMS320C5400

Figure 21 illustrates how to connect the ADS1610 to the TMS320C5400 DSP. The processor controls the reading using the outputs R/$\overline{W}$ and $\overline{IS}$. The I/O space-select signal ($\overline{IS}$) is optional and is used to prevent the ADS1610 $\overline{RD}$ input from being strobed when the DSP is accessing other external memory spaces (address or data). This can help reduce the possibility of digital noise coupling into the ADS1610. When not using this signal, replace NAND gate U1 with an inverter between R/$\overline{W}$ and $\overline{RD}$. Two signals, $\overline{IOSTRB}$ and A15, combine using NAND gate U2 to select the ADS1610. If there are no additional devices connected to the TMS320C5400 I/O space, U2 can be eliminated. Simply connect $\overline{IOSTRB}$ directly to $\overline{CS}$. The ADS1610 16-bit data output bus is directly connected to the TMS320C5400 data bus. The data ready output ($\overline{DRDY}$) from the ADS1610 drives interrupt $\overline{INT3}$ on the TMS320C5400.

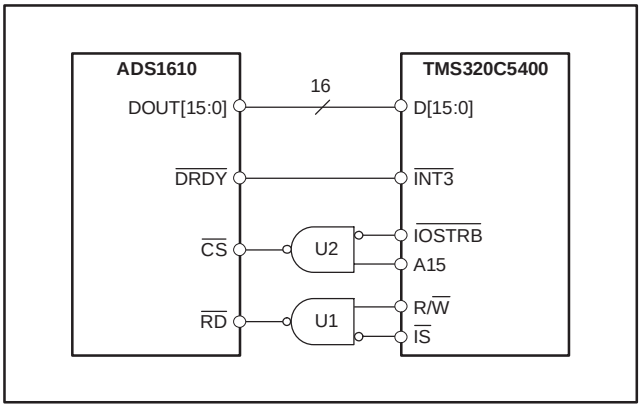

Figure 21. ADS1610—TMS320C5400 Interface Connection

Code Composer Studio, available from TI, provides support for interfacing TI DSPs through a collection of data converter plug-ins. Check the TI website, located at www.ti.com/sc/dcplug-in, for the latest information on ADS1610 support.

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PACKAGE OPTION ADDENDUM

2-Sep-2005

PACKAGING INFORMATION

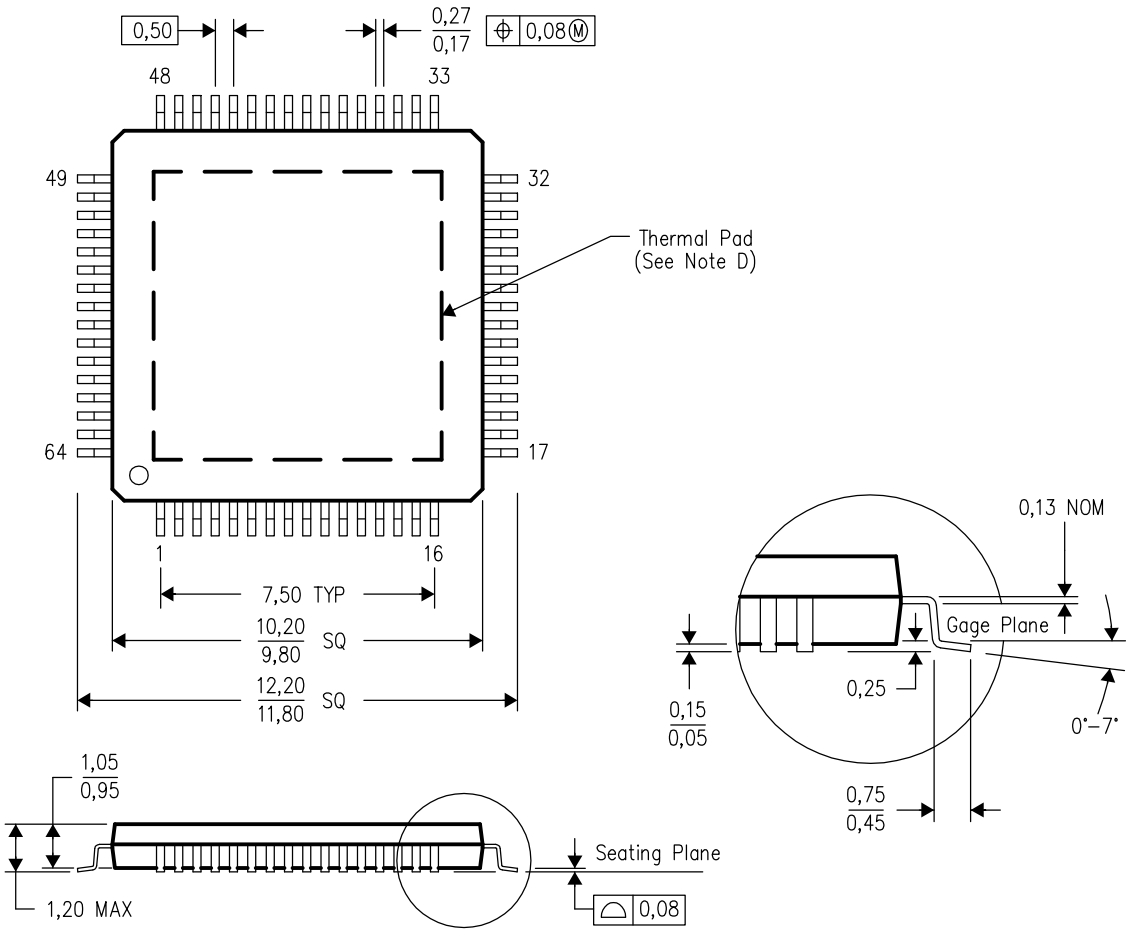
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1610IPAPR	PREVIEW	HTQFP	PAP	64		TBD	Call TI	Call TI
ADS1610IPAPT	PREVIEW	HTQFP	PAP	64		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



4147702/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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