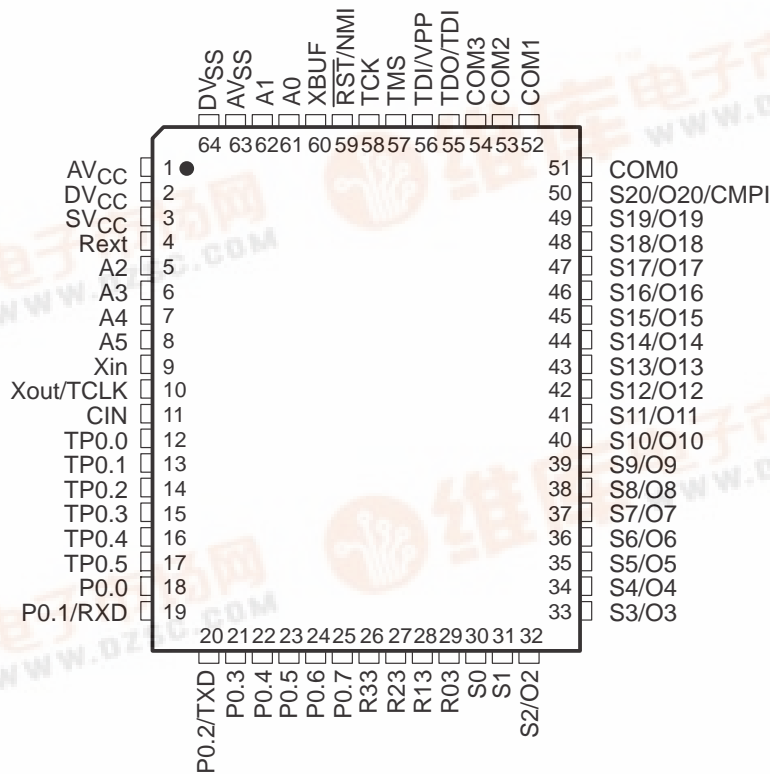


- Low Supply Voltage Range, 2.7 V – 5.5 V
- Low Operation Current, 3 mA at 1 MHz, 3 V
- Ultralow Power Consumption (Standby Mode Down to 0.1 μ A)
- Five Power-Saving Modes
- Wakeup From Standby Mode in 6 μ s
- 16-Bit RISC Architecture, 300 ns Instruction Cycle Time
- Single Common 32 kHz Crystal, Internal System Clock up to 3.3 MHz
- Integrated LCD Driver for up to 84 Segments
- Integrated 12+2 Bit A/D Converter
- Family Members Include:
 - MSP430P325, 16KB OTP, 512 Byte RAM
- EPROM Version Available for Prototyping: PMS430E325
- Serial Onboard Programming
- Programmable Code Protection by Security Fuse
- Available in 64 Pin Quad Flatpack (QFP), 68 Pin Plastic J-Leaded Chip Carrier (PLCC), 68 Pin J-Leaded Ceramic Chip Carrier (JLCC) Package (EPROM Version)

description

The Texas Instruments MSP430 is an ultralow-power mixed-signal microcontroller family consisting of several devices which feature different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for an extended application lifetime. With 16-bit RISC architecture, 16-bit integrated registers on the CPU, and a constant generator, the MSP430 achieves maximum code efficiency. The digitally-controlled oscillator, together with the frequency-locked-loop (FLL), provides a wakeup from a low-power mode to active mode in less than 6 μ s.

PG Package (TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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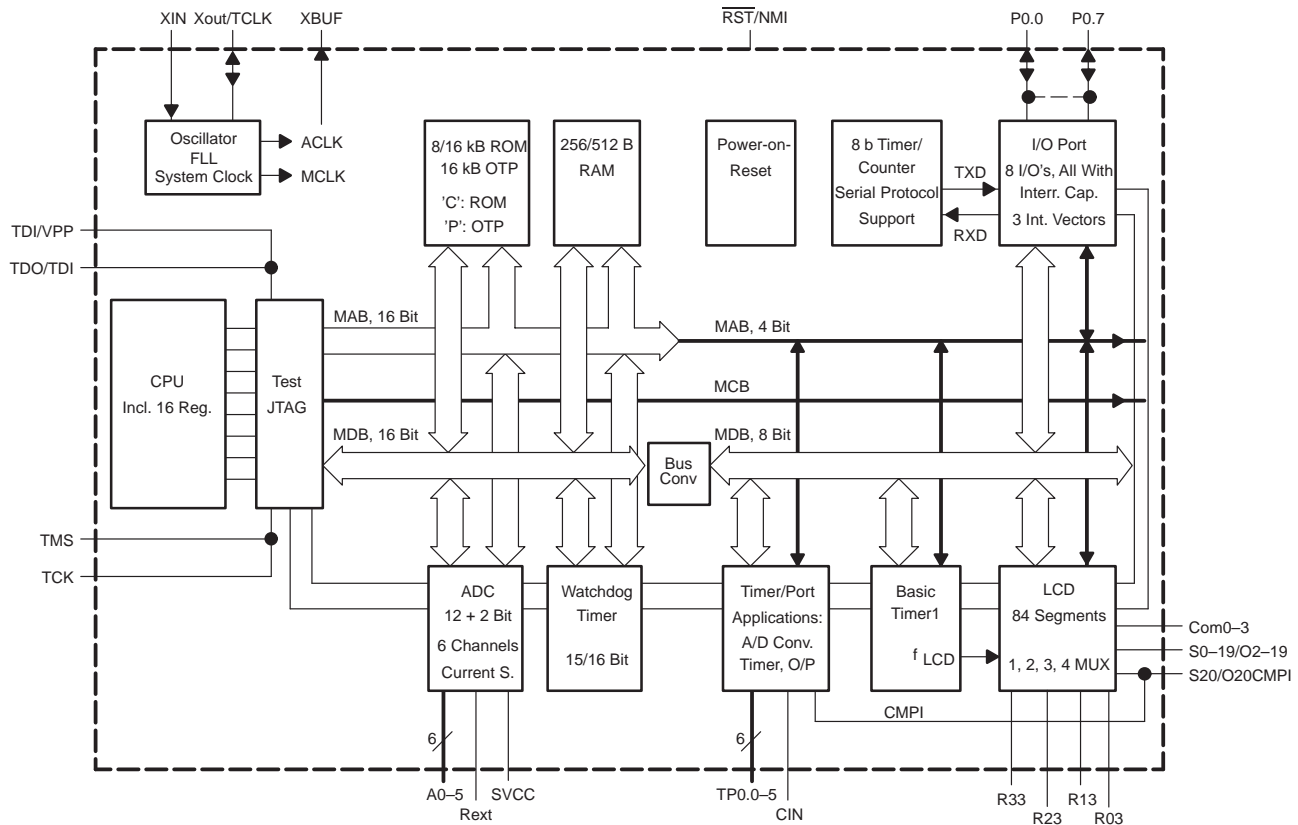
description (continued)

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data and display them or transmit them to a host system. The MSP430x32x offers an integrated 12+2 bit A/D converter with six multiplexed inputs.

AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | |
|----------------|-------------------------|-------------------------|--------------------------|--------------------------|
| | PLASTIC 64-PIN QFP (PG) | PLASTIC 64-PIN QFP (PM) | PLASTIC 68-PIN PLCC (FN) | CERAMIC 68-PIN JLCC (FZ) |
| -40°C to 85°C | MSP430P325IPG | MSP430P325IPM | MSP430P325IFN | — |
| 25°C | — | — | — | PMS430E325FZ |

functional block diagram



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Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------|--------|-----|--|
| AV _{CC} | 1 | | Positive analog supply voltage |
| AV _{SS} | 63 | | Analog ground reference |
| A0 | 61 | I | Analog-to-digital converter input port 0 or digital input port 0 |
| A1 | 62 | I | Analog-to-digital converter input port 1 or digital input port 1 |
| A2–A5 | 5–8 | I | Analog-to-digital converter inputs ports 2–5 or digital inputs ports 2–5 |
| CIN | 11 | I | Input used as enable of counter TPCNT1 – Timer/Port |
| COM0–3 | 51–54 | O | Common outputs, used for LCD backplanes – LCD |
| DV _{CC} | 2 | | Positive digital supply voltage |
| DV _{SS} | 64 | | Digital ground reference |
| P0.0 | 18 | I/O | General-purpose digital I/O |
| P0.1/RXD | 19 | I/O | General-purpose digital I/O, receive digital input port, 8-Bit Timer/Counter |
| P0.2/TXD | 20 | I/O | General-purpose digital I/O, transmit data output port, 8-Bit Timer/Counter |
| P0.3–P0.7 | 21–25 | I/O | Five general-purpose digital I/Os, bit 3 to bit 7 |
| Rext | 4 | I | Programming resistor input of internal current source |
| RST/NMI | 59 | I | Reset input or non-maskable interrupt input |
| R03 | 29 | I | Input of fourth positive analog LCD level (V4) – LCD |
| R13 | 28 | I | Input of third positive analog LCD level (V3) – LCD |
| R23 | 27 | I | Input of second positive analog LCD level (V2) – LCD |
| R33 | 26 | O | Output of first positive analog LCD level (V1) – LCD |
| SV _{CC} | 3 | | Switched AV _{CC} to analog-to-digital converter |
| S0 | 30 | O | Segment line S0 – LCD |
| S1 | 31 | O | Segment line S1 – LCD |
| S2–S5/O2–O5 | 32–35 | O | Segment lines S2 to S5 or digital output ports O2–O5, group 1 – LCD |
| S20/O20/CMPI | 50 | I/O | Segment line S20 can be used as comparator input port CMPI – Timer/Port |
| S6–S9/O6–O9 | 36–39 | O | Segment lines S6 to S9 or digital output ports O6–O9, group 2 – LCD |
| S10–S13/O10–O13 | 40–43 | O | Segment lines S10 to S13 or digital output ports O10–O13, group 3 – LCD |
| S14–S17/O14–O17 | 44–47 | O | Segment lines S14 to S17 or digital output ports O14 to O17, group 4 – LCD |
| S18–S19/O18–O19 | 48, 49 | O | Segment lines S18 and S19 or digital output port O18 and O19, group 5 – LCD |
| TCK | 58 | I | Test clock, clock input terminal for device programming and test |
| TDO/TDI | 55 | I/O | Test data output, data output terminal or data input during programming |
| TDI/VPP | 56 | I | Test data input, data input terminal or input of programming voltage |
| TMS | 57 | I | Test mode select, input terminal for device programming and test |
| TP0.0 | 12 | O | General-purpose 3-state digital output port, bit 0 – Timer/Port |
| TP0.1 | 13 | O | General-purpose 3-state digital output port, bit 1 – Timer/Port |
| TP0.2 | 14 | O | General-purpose 3-state digital output port, bit 2 – Timer/Port |
| TP0.3 | 15 | O | General-purpose 3-state digital output port, bit 3 – Timer/Port |
| TP0.4 | 16 | O | General-purpose 3-state digital output port, bit 4 – Timer/Port |
| TP0.5 | 17 | I/O | General-purpose digital input/output port, bit 5 – Timer/Port |
| XBUF | 60 | O | Clock signal output of system clock MCLK or crystal clock ACLK |
| Xin | 9 | I | Input terminal of crystal oscillator |
| Xout/TCLK | 10 | I/O | Output terminal of crystal oscillator or test clock input |

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short-form description

processing unit

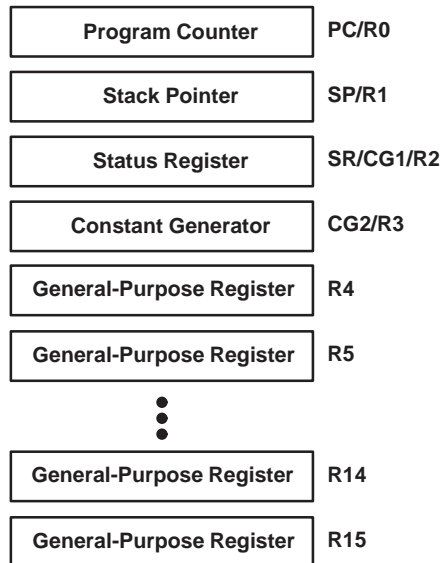
The processing unit is based on a consistent and orthogonally-designed CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development, and it is distinguished by ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU

Sixteen registers are located inside the CPU, providing reduced instruction execution time. This reduces a register-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as a program counter, a stack pointer, a status register, and a constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus and can be handled easily with all instructions for memory manipulation.



instruction set

The instruction set for this register-register architecture provides a powerful and easy-to-use assembler language. The instruction set consists of 51 instructions with three formats and seven addressing modes. Table 1 provides a summation and example of the three types of instruction formats; the addressing modes are listed in Table 2.

Table 1. Instruction Word Formats

| | | |
|-----------------------------------|-----------------|-----------------------|
| Dual operands, source-destination | e.g. ADD R4, R5 | R4 + R5 → R5 |
| Single operands, destination only | e.g. CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, un-/conditional | e.g. JNE | Jump-on equal bit = 0 |

Each instruction that operates on word and byte data is identified by the suffix B.

| | | |
|-----------|---------------------------------|---------------------------------|
| Examples: | Instructions for word operation | Instructions for byte operation |
| | MOV EDE, TONI | MOV.B EDE, TONI |
| | ADD #235h, &MEM | ADD.B #35h, &MEM |
| | PUSH R5 | PUSH.B R5 |
| | SWPB R5 | — |

Table 2. Address Mode Descriptions

| ADDRESS MODE | s | d | SYNTAX | EXAMPLE | OPERATION |
|------------------------|---|---|------------------|-------------------|-----------------------------|
| Register | √ | √ | MOV Rs, Rd | MOV R10, R11 | R10 → R11 |
| Indexed | √ | √ | MOV X(Rn), Y(Rm) | MOV 2(R5), 5(R6) | M(2 + R5) → M(6 + R6) |
| Symbolic (PC relative) | √ | √ | MOV EDE, TONI | | M(EDE) → M(TONI) |
| Absolute | √ | √ | MOV &MEM, &TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | √ | | MOV @Rn, Y(Rm) | MOV @R10, Tab(R6) | M(R10) → M(Tab + R6) |
| Indirect autoincrement | √ | | MOV @Rn+, RM | MOV @R10+, R11 | M(R10) → R11, R10 + 2 → R10 |
| Immediate | √ | | MOV #X, TONI | MOV #45, TONI | #45 → M(TONI) |

NOTE: s = source d = destination

Computed branches (BR) and subroutine calls (CALL) instructions use the same addressing modes as the other instructions. These addressing modes provide *indirect* addressing, ideally suited for computed branches and calls. The full use of this programming capability permits a program structure different from conventional 8- and 16-bit controllers. For example, numerous routines can easily be designed to deal with pointers and stacks instead of using flag type programs for flow control.

operation modes and interrupts

The MSP430 operating modes support various advanced requirements for ultralow power and ultralow energy consumption. This is achieved by the intelligent management of the operations during the different module operation modes and CPU states. The requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the RETI instruction to the mode that was selected before the interrupt event. The clocks used are ACLK and MCLK. ACLK is the crystal frequency and MCLK is a multiple of ACLK and is used as the system clock.

The software can configure five operating modes:

- Active mode (AM). The CPU is enabled with different combinations of active peripheral modules.
- Low power mode 0 (LPM0). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is active.
- Low power mode 1 (LPM1). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is inactive.
- Low power mode 2 (LPM2). The CPU is disabled, peripheral operation continues, ACLK signal is active, and MCLK and loop control for MCLK are inactive.
- Low power mode 3 (LPM3). The CPU is disabled, peripheral operation continues, ACLK signal is active, MCLK and loop control for MCLK are inactive, and the dc generator for the digital controlled oscillator (DCO) (→MCLK generator) is switched off.
- Low power mode 4 (LPM4). The CPU is disabled, peripheral operation continues, ACLK signal is inactive (crystal oscillator stopped), MCLK and loop control for MCLK are inactive, and the dc generator for the DCO is switched off.

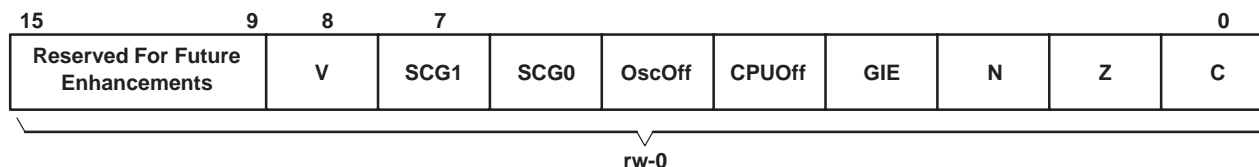
The special function registers (SFR) include module-enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. However, some peripheral current-saving functions are accessed through the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral, which is turned on or off using one register bit.

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operation modes and interrupts (continued)

The most general bits that influence current consumption and support fast turnon from low-power operating modes are located in the status register (SR). Four of these bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.



interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---------------------------------|--------------|-------------|
| Power-up, external reset, watchdog | WDTIFG (see Note 1) | Reset | 0FFFEh | 15, highest |
| NMI, oscillator fault | NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 4) | Non-maskable, (Non)-maskable | 0FFFCh | 14 |
| Dedicated I/O P0.0 | P0.0IFG | Maskable | 0FFFAh | 13 |
| Dedicated I/O P0.1 or 8-Bit Timer/Counter RXD | P0.1IFG | Maskable | 0FFF8h | 12 |
| | | | 0FFF6h | 11 |
| Watchdog Timer | WDTIFG | Maskable | 0FFF4h | 10 |
| | | | 0FFF2h | 9 |
| | | | 0FFF0h | 8 |
| | | | 0FFEEh | 7 |
| | | | 0FFEC | 6 |
| ADC | ADCIFG | Maskable | 0FFEAh | 5 |
| Timer/Port | RC1FG, RC2FG, EN1FG (see Note 2) | Maskable | 0FFE8h | 4 |
| | | | 0FFE6h | 3 |
| | | | 0FFE4h | 2 |
| Basic Timer1 | BTIFG | Maskable | 0FFE2h | 1 |
| I/O port 0, P0.2–7 | P0.27IFG (see Note 1) | Maskable | 0FFE0h | 0, lowest |

- NOTES:
1. Multiple source flags
 2. Timer/Port interrupt flags are located in the T/P registers
 3. Non-maskable: neither the individual nor the general interrupt enable bit will disable an interrupt event.
 4. (Non)-maskable: the individual interrupt enable bit can disable on interrupt event, but the general interrupt enable bit cannot.

operation modes and interrupts (continued)

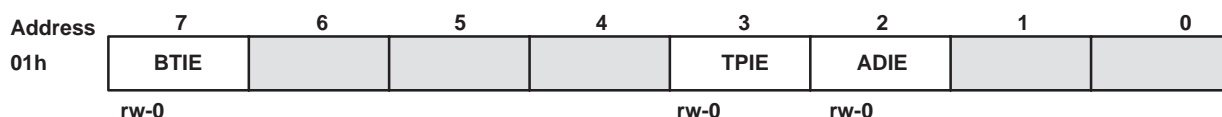
special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple SW access is provided with this arrangement.

interrupt enable 1 and 2

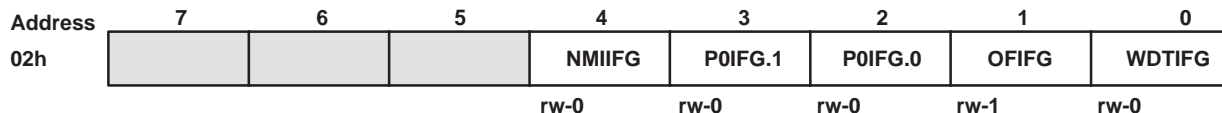


- WDTIE: Watchdog Timer enable signal
- OFIE: Oscillator fault enable signal
- P0IE.0: Dedicated I/O P0.0
- P0IE.1: P0.1 or 8-Bit Timer/Counter, RXD



- ADIE: A/D converter enable signal
- TPIE: Timer/Port enable signal
- BTIE: Basic Timer1 enable signal

interrupt flag register 1 and 2



- WDTIFG: Set on overflow or security key violation
or
Reset on V_{CC} power on or reset condition at $\overline{\text{RST}}$ /NMI-pin
- OFIFG: Flag set on oscillator fault
- P0.0IFG: Dedicated I/O P0.0
- P0.1IFG: P0.1 or 8-Bit Timer/Counter, RXD
- NMIIFG: Signal at $\overline{\text{RST}}$ /NMI-pin



- BTIFG Basic Timer1 flag
- ADIFG Analog-to-digital converter flag

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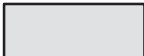
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operation modes and interrupts (continued)

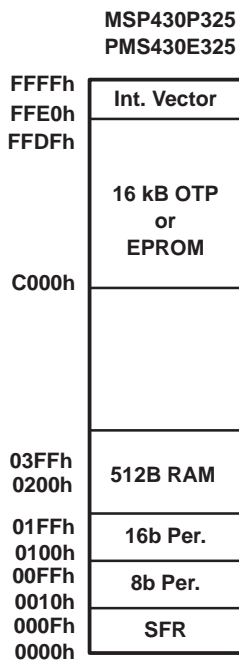
module enable register 1 and 2



Legend

| | |
|---|--|
| rw: | Bit can be read and written. |
| rw-0: | Bit can be read and written. It is reset by PUC. |
|  | SFR bit not present in device. |

memory organization



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peripherals

Peripherals connect to the CPU through data, address, and control busses and can be handled easily with all instructions for memory manipulation.

peripheral file map

| PERIPHERALS WITH WORD ACCESS | | | |
|------------------------------|-------------------------------|---------|-------|
| Watchdog | Watchdog Timer control | WDCTL | 0120h |
| ADC | Data register | ADAT | 0118h |
| | Reserved | | 0116h |
| | Control register | ACTL | 0114h |
| | Input enable register | AEN | 0112h |
| | Input register | AIN | 0110h |
| PERIPHERALS WITH BYTE ACCESS | | | |
| EPROM | EPROM control | EPCTL | 054h |
| Crystal buffer | Crystal buffer control | CBCTL | 053h |
| System clock | SCG frequency control | SCFQCTL | 052h |
| | SCG frequency integrator | SCFI1 | 051h |
| | SCG frequency integrator | SCFI0 | 050h |
| Timer/Port | Timer/Port enable | TPE | 04Fh |
| | Timer/Port data | TPD | 04Eh |
| | Timer/Port counter2 | TPCNT2 | 04Dh |
| | Timer/Port counter1 | TPCNT1 | 04Ch |
| | Timer/Port control | TPCTL | 04Bh |
| 8-Bit Timer/Counter | 8-Bit Timer/Counter data | TCDAT | 044h |
| | 8-Bit Timer/Counter preload | TCPLD | 043h |
| | 8-Bit Timer/Counter control | TCCTL | 042h |
| Basic Timer1 | Basic Timer counter2 | BTCNT2 | 047h |
| | Basic Timer counter1 | BTCNT1 | 046h |
| | Basic Timer control | BTCTL | 040h |
| LCD | LCD memory 15 | LCDM15 | 03Fh |
| | : | : | : |
| | LCD memory 1 | LCDM1 | 031h |
| Port P0 | LCD control & mode | LCDCTL | 030h |
| | Port P0 interrupt enable | P0IE | 015h |
| | Port P0 interrupt edge select | P0IES | 014h |
| | Port P0 interrupt flag | P0IFG | 013h |
| | Port P0 direction | P0DIR | 012h |
| | Port P0 output | P0OUT | 011h |
| Special function | Port P0 input | P0IN | 010h |
| | SFR interrupt flag2 | IFG2 | 003h |
| | SFR interrupt flag1 | IFG1 | 002h |
| | SFR interrupt enable2 | IE2 | 001h |
| | SFR interrupt enable1 | IE1 | 000h |

oscillator and system clock

Two clocks are used in the system, the system (master) clock (MCLK) and the auxiliary clock (ACLK). The MCLK is a multiple of the ACLK. The ACLK runs with the crystal oscillator frequency. The special design of the oscillator supports the feature of low current consumption and the use of a 32 768 Hz crystal. The crystal is connected across two terminals without any other external components being required.

The oscillator starts after applying VCC, due to a reset of the control bit (OscOff) in the status register (SR). It can be stopped by setting the OscOff bit to a 1. The enabled clock signals ACLK, ACLK/2, ACLK/4, or MCLK are accessible for use by external devices at output terminal XBUF.

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oscillator and system clock (continued)

The controller system clock has to operate with different requirements according to the application and system conditions. Requirements include:

- High frequency in order to react quickly to system hardware requests or events
- Low frequency in order to minimize current consumption, EMI, etc.
- Stable frequency for timer applications e.g. real-time clock (RTC)
- Enable start-stop operation with a minimum of delay

These requirements cannot all be met with fast frequency high-Q crystals or with RC-type low-Q oscillators. The compromise selected for the MSP430 uses a low-crystal frequency, which is multiplied to achieve the desired nominal operating range:

$$f_{(\text{system})} = (N+1) \times f_{(\text{crystal})}$$

The crystal frequency multiplication is achieved with a frequency locked loop (FLL) technique. The factor N is set to 31 after a power-up clear condition. The FLL technique, in combination with a digital controlled oscillator (DCO) provides immediate start-up capability together with long term crystal stability. The frequency variation of the DCO with the FLL inactive is typically 330 ppm, which means that with a cycle time of 1 μs the maximum possible variation is 0.33 ns. For more precise timing, the FLL can be used forcing longer cycle times, if the previous cycle time was shorter than the selected one. This switching of cycle times makes it possible to meet the chosen system frequency over a long period of time.

The start-up operation of the system clock depends on the previous machine state. During a power-up clear (PUC), the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after recognition of PUC. Connect operation of the FLL control logic requires the presence of a stable crystal oscillator.

digital I/O

One 8-Bit I/O port (Port0) is implemented. Six control registers give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of port P0.
- Provides read/write access to all registers with all instructions

The six registers are:

- Input register Contains information at the pins
- Output register Contains output information
- Direction register Controls direction
- Interrupt flags Indicates if interrupt(s) are pending
- Interrupt edge select Contains input signal change necessary for interrupt
- Interrupt enable Contains interrupt enable pins

All six registers contain eight bits except for the interrupt flag register and the interrupt enable register. The two LSBs of the interrupt flag and interrupt enable registers are located in the special functions register (SFR). Three interrupt vectors are implemented, one for Port0.0, one for Port0.1, and one commonly used for any interrupt event on Port0.2 to Port0.7. The Port0.1 and Port0.2 pin function is shared with the 8-Bit Timer/Counter.

LCD drive

Liquid crystal displays (LCDs) for static, 2-, 3- and 4-MUX operations can be driven directly. The controller LCD logic operation is defined by software using memory-bit manipulation. LCD memory is part of the LCD module, not part of data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily obtained using table programming techniques combined with the correct addressing mode. The segment information is stored in LCD memory using instructions for memory manipulation.

The drive capability is mainly defined by the external resistor divider that supports the analog levels for 2-, 3- and 4-MUX operation. Groups of the LCD segment lines can be selected for digital output signals. The MSP430x32x configuration has four common signal lines and 21 segment lines.

A/D converter

The analog-to-digital converter (ADC) is a cascaded converter type that converts analog signals from V_{CC} to GND. It is a 12+2 bit converter with a software or automatically-controlled range select. Five inputs can be selected for analog or digital function. A ratiometric current source can be used on four of the analog pins. The current is adjusted by an external resistor and is enabled/disabled by bits located in the control registers. The conversion is started by setting the start-of-conversion bit (SOC) in the control register and the end-of-conversions sets the interrupt flag. The analog input signal is sampled starting with SOC during the next twelve MCLK clock pulses. The power-down bit in the control register controls the operating mode of the ADC peripheral. The current consumption and operation is stopped when it is set. The system reset PUC sets the power-down bit.

Basic Timer1

The Basic Timer1 (BT1) divides the frequency of MCLK or ACLK, as selected with the SSEL bit, to provide low frequency control signals. This is done within the system by one central divider, the Basic Timer1, to support low current applications. The BTCTL control register contains the flags which control or select the different operational functions. When the supply voltage is applied or when a reset of the device (\overline{RST}/NMI pin), a watchdog overflow or a watchdog security key violation occurs, and all bits in the register hold undefined or unchanged status. The user software usually configures the operational conditions on the BT1 during initialization.

The Basic Timer1 has two 8-Bit timers which can be cascaded to a 16-bit timer. Both timers can be read and written by software. Two bits in the SFR address range handle the system control interaction according to the function implemented in the Basic Timer1. These two bits are the Basic Timer1 interrupt flag (BTIFG) and the Basic Timer1 interrupt enable (BTIE) bit.

Watchdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The Watchdog Timer counter (WDTCNT) is a 15/16-bit up-counter which is not directly accessible by software. The WDTCNT is controlled using the Watchdog Timer control register (WDTCTL), which is an 8-Bit read/write register. Writing to WDTCTL, in both operating modes (watchdog or timer) is only possible by using the correct password in the high-byte. The low-byte stores data written to the WDTCTL. The high-byte password is 05Ah. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. *When the password is read its value is 069h.* This minimizes accidental write operations to the WDTCTL register. In addition to the Watchdog Timer control bits, two bits included in the WDTCTL configure the NMI pin.

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8-Bit Timer/Counter

The 8-Bit interval timer supports three major functions for the application:

- Serial communication or data exchange
- Pulse counting or pulse accumulation
- Timer

The 8-Bit Timer/Counter peripheral includes the following major blocks: an 8-Bit up-counter with preload register, an 8-Bit control register, an input clock selector, an edge detection (e.g. Start bit detection for asynchronous protocols), and an input and output data latch, triggered by the carry-out-signal from the 8-Bit counter.

The 8-Bit counter counts up with an input clock which is selected by two control bits from the control register. The four possible clock sources are MCLK, ACLK, the external signal from terminal P0.1, and the signal from the logical AND of MCLK and terminal P0.1.

Two counter inputs (load, enable) control the counter operation. The load input controls load operations. A write-access to the counter results in loading the content of the preload register into the counter. The software writes or reads the preload register with all instructions. The preload register acts as a buffer and can be written immediately after the load of the counter is completed. The enable input enables the count operation. When the enable signal is set to high, the counter will count-up each time a positive clock edge is applied to the clock input of the counter.

Serial protocols, like UART protocol, need start-bit edge-detection to determine, at the receiver, the start of a data transmission. When this function is activated, the counter starts counting after the start-bit condition is detected. The first signal level is sampled into the RXD input data-latch after completing the first timing interval, which is programmed into the counter. Two latches are used for input and output data (RXD_FF and TXD_FF) are clocked by the counter after the programmed timing interval has elapsed.

UART

The serial communication uses software and the 8-Bit Timer/Counter hardware. The hardware supports the output of the serial data stream, bit-by-bit, with the timing determined by the counter. The software/hardware interface connects the mixed signal controller to external devices, systems, or networks.

Timer/Port

The Timer/Port module has two 8-Bit counters, an input that triggers one counter, and six 3-state digital outputs. Both counters have an independent clock-selector for selecting an external signal or one of the internal clocks (ACLK or MCLK). One of the counters has an extended control capability to halt, count continuously, or gate the counter by selecting one of two external signals. This gate signal sets the interrupt flag, if an external signal is selected, and the gate stops the counter.

Both timers can be read from and written to by software. The two 8-Bit counters can be cascaded to a 16-bit counter. A common interrupt vector is implemented. The interrupt flag can be set from three events in the 8-Bit counter mode (gate signal, overflow from the counters) or from two events in the 16-bit counter mode (gate signal, overflow from the MSB of the cascaded counter).

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absolute maximum ratings†

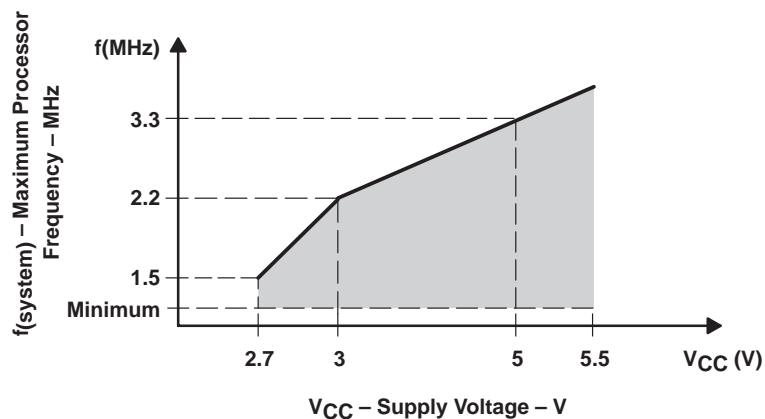
| | |
|--|----------------------------|
| Voltage applied at V_{CC} to V_{SS} (see Note 5) | –0.3 V to 6 V |
| Voltage applied to any pin (referenced to V_{SS}) | –0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal | ± 2 mA |
| Storage temperature, T_{stg} (unprogrammed device) | –55°C to 150°C |
| T_{stg} (programmed device) | –40°C to 85°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 5: All voltage values relative to V_{SS} .

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|------------------------|---------------------|---------------------|--------------|------|
| Supply voltage, V_{CC} (MSP430P/E325) | | 2.7 | | 5.5 | V |
| Supply voltage, during programming OTP/EPROM ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430P325, PMS430E325 | 2.7 | 5 | 5.5 | V |
| Supply voltage, V_{SS} | | | 0 | | V |
| Operating free-air temperature range, T_A | MSP430P325 | –40 | | 85 | °C |
| | PMS430E325 | | 25 | | |
| XTAL frequency, $f_{(XTAL)}$ | | | 32 768 | | Hz |
| Processor frequency (signal MCLK), $f_{(system)}$ | $V_{CC} = 3$ V | DC | | 2.2 | MHz |
| | $V_{CC} = 5$ V | DC | | 3.3 | |
| Low-level input voltage, V_{IL} (excluding X_{in} , X_{out}) | $V_{CC} = 3$ V/5 V | | V_{SS} | $V_{SS}+0.8$ | V |
| High-level input voltage, V_{IH} (excluding X_{in} , X_{out}) | | $0.7 V_{CC}$ | V_{CC} | | |
| Low-level input voltage, $V_{IL}(X_{in}, X_{out})$ | | V_{SS} | $0.2 \times V_{CC}$ | | V |
| High-level input voltage, $V_{IH}(X_{in}, X_{out})$ | | $0.8 \times V_{CC}$ | V_{CC} | | |



NOTE: Minimum processor frequency is defined by system clock.

Figure 1. Processor Frequency vs Supply Voltage

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

supply current into $V_{CC}+DV_{CC}$ excluding external current, $f_{system} = 1$ MHz

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|----------------|---|--|--|---------------------|-------|---------|---------|-----|
| $I_{(AM)}$ | Active mode, A/D conversion in power-down | P325 $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 3$ V | | 3000 | 5000 | μA | | |
| | | | $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 5$ V | 10000 | 12000 | | | |
| $I_{(CPUOff)}$ | Low power mode, (LPM0, LPM1) | P325 $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 3$ V | | 70 | 110 | μA | | |
| | | | $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 5$ V | 150 | 200 | | | |
| $I_{(LPM2)}$ | Low power mode, (LPM2) | $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 3$ V | | 6 | 12 | μA | | |
| | | | $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 5$ V | 15 | 25 | | | |
| $I_{(LPM3)}$ | Low power mode, (LPM3) | $T_A = -40^{\circ}C$ | $V_{CC} = 3$ V | | 1.5 | 2.4 | μA | |
| | | | | $T_A = 25^{\circ}C$ | | 1.3 | | 2 |
| | | | | $T_A = 85^{\circ}C$ | | 1.6 | | 2.8 |
| | | $T_A = -40^{\circ}C$ | $V_{CC} = 5$ V | | 5.2 | 7 | | |
| | | | | $T_A = 25^{\circ}C$ | | 4.2 | | 6.5 |
| | | | | $T_A = 85^{\circ}C$ | | 4 | | 7 |
| $I_{(LPM4)}$ | Low power mode, (LPM4) | $T_A = -40^{\circ}C$ | $V_{CC} = 3$ V/5 V | | 0.1 | 0.8 | μA | |
| | | | | $T_A = 25^{\circ}C$ | | 0.1 | | 0.8 |
| | | | | $T_A = 85^{\circ}C$ | | 0.4 | | 1.3 |

NOTE: All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current. The current consumption in LPM2, LPM3 and LPM4 are measured with active Basic Timer1 (ACLK selected) and LCD module ($f_{(LCD)}=1024$ Hz, 4 MUX).

current consumption of active mode versus system frequency

$$I_{AM} = I_{AM[1\text{ MHz}]} \times f_{system} [\text{MHz}]$$

current consumption of active mode versus supply voltage

$$I_{AM} = I_{AM[3\text{ V}]} + 200 \mu A/V \times (V_{CC}-3\text{ V})$$

Schmitt-trigger inputs Port 0, P0.x Timer/Port, CIN, TP 0.5

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------|--|----------------|----------------|-----|------|---|
| V_{IT+} | Positive-going input threshold voltage | $V_{CC} = 3$ V | | 1.2 | 2.1 | V |
| | | | $V_{CC} = 5$ V | 2.3 | 3.4 | |
| V_{IT-} | Negative-going input threshold voltage | $V_{CC} = 3$ V | | 0.5 | 1.35 | |
| | | | $V_{CC} = 5$ V | 1.4 | 2.3 | |
| V_{hys} | Hysteresis ($V_{IT+}-V_{IT-}$) | $V_{CC} = 3$ V | | 0.3 | 1 | |
| | | | $V_{CC} = 5$ V | 0.6 | 1.4 | |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

outputs – Port 0: P0.x; Timer/Port: TP0.0...5; LCD: Sxx/Oxx; XBUF, (see Note 6)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------|--|----------------------|-----|----------------------|------|
| V _{OH} | High-level output current | I _{OH} = -1.2 mA, V _{CC} = 3 V, See Note 6 | V _{CC} -0.4 | | V _{CC} | V |
| | | I _{OH} = -3.5 mA, V _{CC} = 3 V, See Note 7 | V _{CC} -1 | | V _{CC} | |
| | | I _{OH} = -1.5 mA, V _{CC} = 5 V, See Note 6 | V _{CC} -0.4 | | V _{CC} | |
| | | I _{OH} = -4.5 mA, V _{CC} = 5 V, See Note 7 | V _{CC} -1 | | V _{CC} | |
| V _{OL} | Low-level output voltage | I _{OL} = 1.2 mA, V _{CC} = 3 V, See Note 6 | V _{SS} | | V _{SS} +0.4 | V |
| | | I _{OL} = 3.5 mA, V _{CC} = 3 V, See Note 7 | V _{SS} | | V _{SS} +1 | |
| | | I _{OL} = 1.5 mA, V _{CC} = 5 V, See Note 6 | V _{SS} | | V _{SS} +0.4 | |
| | | I _{OL} = 4.5 mA, V _{CC} = 5 V, See Note 7 | V _{SS} | | V _{SS} +1 | |

- NOTES: 6. The maximum total current, I_{OH}max and I_{OL}max, for all outputs combined, should not exceed ±9.6 mA to satisfy the maximum voltage drop specified.
 7. The maximum total current, I_{OH}max and I_{OL}max, for all outputs combined, should not exceed ±20 mA to satisfy the maximum voltage drop specified.

leakage current (see Note 8)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|-----------------------------|---|-----|-----|-----|------|
| I _{lkg} (TP) | Leakage current, Timer/Port | Timer/Port: V _(TP0.x,CIN) (see Note 9) | | | ±50 | nA |
| I _{lkg} (P0x) | Leakage current, port 0 | Port 0: V _(P0.x) (see Note 10) | | | ±50 | nA |
| I _{lkg} (S20) | Leakage current, S20 | V _(S20) = V _{SS} to V _{CC} | | | ±50 | nA |
| I _{lkg} (Ax) | Leakage current, ADC | ADC: Ax, x= 0 to 5 (see Note 11) | | | ±30 | nA |
| I _{lkg} (RST/NMI) | Leakage current, RST/NMI | | | | ±50 | nA |

- NOTES: 8. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
 9. All Timer/Port pins TP0.0 to TP0.5 are Hi-Z. Pins CIN and TP.0 to TP0.5 are connected together during leakage current measurement. In the leakage measurement the input CIN is included. The input voltage is V_{SS} or V_{CC}.
 10. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.
 11. The input voltage is V_(IN) = V_{SS} to V_{CC}, the current source is off, AEN.x bit is normally reset to stop throughput current flowing from V_{CC} to V_{SS} terminal.

input frequency – Port 0: P0.1; Timer/Port: CIN, TP0.5

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|------------------------------|-----------------|-----|-----|-----------------------|------|
| f _(IN) | Input frequency | | DC | | f _(system) | MHz |
| t _(H) or t _(L) | High level or low level time | P0.x, CIN, TP.5 | 3 V | | | ns |
| | | | 5 V | | | ns |

output frequency

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------------|---|--|-----|-----------------------|------|
| f _{XBUF} | | XBUF, C _L = 20 pF | | | f _(system) | MHz |
| t _{Xdc} | Duty cycle of O/P frequency | XBUF, C _L = 20 pF, V _{CC} = 3 V/5 V | f _{MCLK} = 1.1 MHz | 40% | 60% | |
| | | | f _{XBUF} = f _{ACLK} | 35% | 65% | |
| | | | f _{XBUF} = f _{ACLK} /n | | 50% | |

MSP430P325

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

external interrupt timing

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---|-----|-----|-----|-------|
| $t_{(int)}$ | Port P0: External trigger signal for the interrupt flag (see Notes 12 and 13) | 1.5 | | | cycle |

NOTES: 12. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. Input frequency ($t_{(int)}$) is defined in MCLK cycles.
 13. The external signal needs additionally a timing resulting from the maximum input frequency constraint.

RAM

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|--------------------------|-----|-----|-----|------|
| V_{RAMh} | CPU halted (see Note 14) | 1.8 | | | V |

NOTE 14: This parameter defines the minimum supply voltage when the data in the program memory RAM remains unchanged. No program execution should take place during this supply voltage condition.

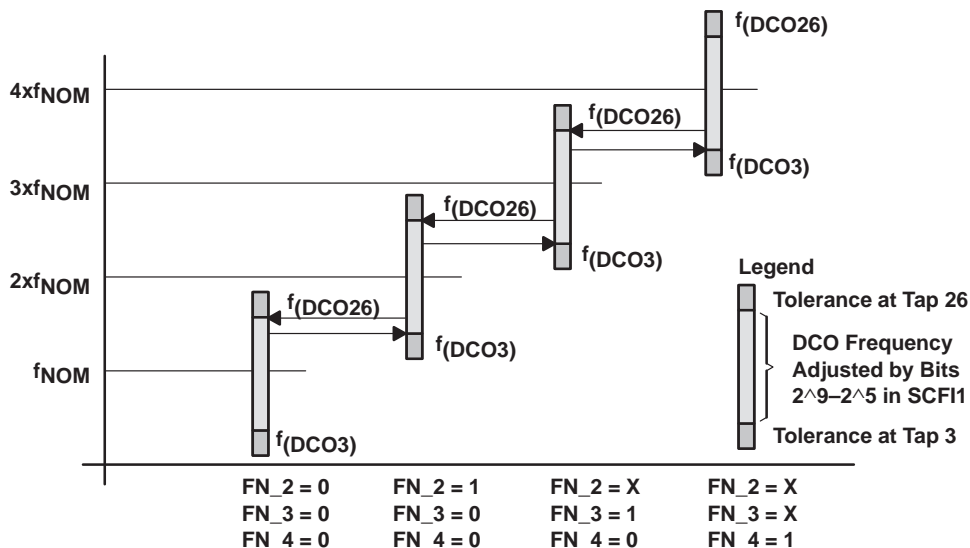
DCO

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------|---|---|-----------------------|------|------|-----|
| $f_{(NOM)}$ | DCO NDCO = 1A0h, FN_4=FN_3=FN_2=0 | $V_{CC} = 3\text{ V/5 V}$ | 1 | | MHz | |
| $f_{(NOM)}$ | f_{DCO3} | NDCO = 00 0110 0000, FN_4=FN_3=FN_2=0 | $V_{CC} = 3\text{ V}$ | 0.15 | 0.6 | MHz |
| | | $V_{CC} = 5\text{ V}$ | 0.18 | 0.62 | | |
| | f_{DCO26} | NDCO = 11 0100 0000 FN_4=FN_3=FN_2=0 | $V_{CC} = 3\text{ V}$ | 1.25 | 4.7 | |
| | | $V_{CC} = 5\text{ V}$ | 1.45 | 5.5 | | |
| $2xf_{(NOM)}$ | f_{DCO3} | NDCO = 00 0110 0000, FN_4=FN_3=0, FN_2=1 | $V_{CC} = 3\text{ V}$ | 0.36 | 1.05 | MHz |
| | | $V_{CC} = 5\text{ V}$ | 0.39 | 1.2 | | |
| | f_{DC26} | NDCO = 11 0100 0000, FN_4=FN_3=0, FN_2=1 | $V_{CC} = 3\text{ V}$ | 2.5 | 8.1 | |
| | | $V_{CC} = 5\text{ V}$ | 3 | 9.9 | | |
| $3xf_{(NOM)}$ | f_{DCO3} | NDCO = 00 0110 0000, FN_4=0, FN_3=1, FN_2=X | $V_{CC} = 3\text{ V}$ | 0.5 | 1.5 | MHz |
| | | $V_{CC} = 5\text{ V}$ | 0.6 | 1.8 | | |
| | f_{DCO26} | NDCO = 11 0100 0000, FN_4=0, FN_3=1, FN_2=X | $V_{CC} = 3\text{ V}$ | 3.7 | 11 | |
| | | $V_{CC} = 5\text{ V}$ | 4.5 | 13.8 | | |
| $4xf_{(NOM)}$ | f_{DCO3} | NDCO = 00 0110 0000 FN_4 =1, FN_3=FN_2=X | $V_{CC} = 3\text{ V}$ | 0.7 | 1.85 | MHz |
| | | $V_{CC} = 5\text{ V}$ | 0.8 | 2.4 | | |
| | f_{DCO26} | NDCO = 11 0100 0000, FN_4=1, FN_3=FN_2=X | $V_{CC} = 3\text{ V}$ | 4.8 | 13.3 | |
| | | $V_{CC} = 5\text{ V}$ | 6 | 17.7 | | |
| NDCO | $f_{MCLK} = f_{NOM}$, FN_4=FN_3=FN_2=0 | $V_{CC} = 3\text{ V/5 V}$ | A0h | 1A0h | 340h | |
| S | $f_{NDCO+1} = S \times f_{NDCO}$ | $V_{CC} = 3\text{ V/5 V}$ | 1.07 | | 1.13 | |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)



crystal oscillator

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|------------------------------------|-----|-----|-----|------|
| $C(X_{in})$ Integrated capacitance at input | $V_{CC} = 3 \text{ V}/5 \text{ V}$ | | 12 | | pF |
| $C(X_{out})$ Integrated capacitance at output | $V_{CC} = 3 \text{ V}/5 \text{ V}$ | | 12 | | pF |

PUC/POR

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|------------------------|-----------------|------------------------------------|---------------------------|-----|---------------|---|
| $t(\text{POR_delay})$ | | | 150 | 250 | μs | |
| $V(\text{POR})$ | POR | $V_{CC} = 3 \text{ V}/5 \text{ V}$ | $T_A = -40^\circ\text{C}$ | | 2.4 | V |
| | | | $T_A = 25^\circ\text{C}$ | | 2.1 | V |
| | | | $T_A = 85^\circ\text{C}$ | | 1.8 | V |
| $V(\text{min})$ | | | 0 | 0.4 | V | |
| $t(\text{reset})$ | PUC/POR | Reset is accepted internally | | 2 | μs | |

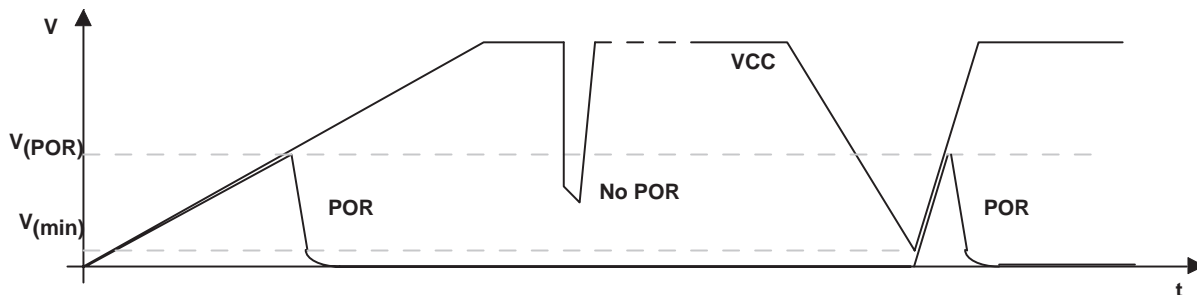


Figure 3. Power-On Reset (POR) vs Supply Voltage

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

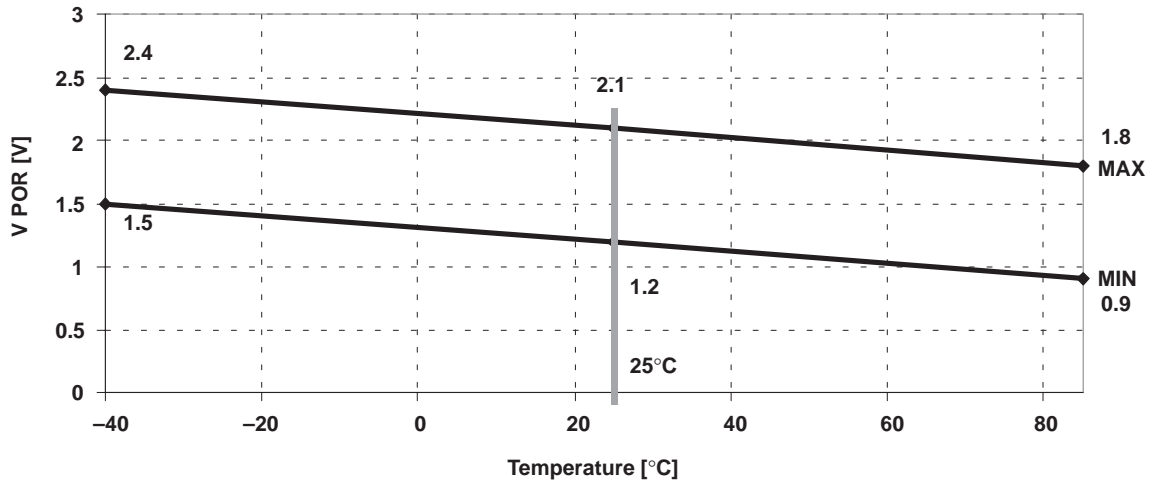


Figure 4. V_(POR) vs Temperature

LCD

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------|---|---------------------------|------------------------|-----|------------------------|------|
| V _O (HLCD) | Output 1 (HLCD) | I _I (HLCD) ≤ 10 nA | V _{CC} = 3 V/5 V | V _{CC} -0.125 | | V _{CC} | V |
| V _O (LLCD) | Output 0 (LLCD) | I _I (LLCD) ≤ 10 nA | | V _{SS} | | V _{SS} +0.125 | |
| I _I (R03) | Input leakage | R03 = V _{SS} , No load at all seg and com pins | V _{CC} = 3 V/5 V | | | ±20 | nA |
| I _I (R13) | | R13 = V _{CC} / 3, No load at all seg and com pins | | | | | |
| I _I (R23) | | R23 = 2 V _{CC} / 3, No load at all seg and com pins | | | | | |
| r _o (Rx3 to Sxx) | Resistance | I _I (SXX) = -3 μA, | V _{CC} = 3 V/5 V | | | 50 | kΩ |

comparator (Timer/Port)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------------|--|-----------------|---------------------------|----------------------|----------------------|----------------------|------|
| I _I (com) | Comparator (Timer/Port) | CPON = 1 | V _{CC} = 3 V | | 250 | 350 | μA |
| | | | V _{CC} = 5 V | | 450 | 600 | |
| V _{ref} (com) | Internal reference voltage at (-) terminal | CPON = 1 | V _{CC} = 3 V/5 V | 0.23×V _{CC} | 0.25×V _{CC} | 0.26×V _{CC} | V |
| V _{hys} (com) | Input hysteresis (comparator) | CPON = 1 | V _{CC} = 3 V | | 5 | 37 | mV |
| | | | V _{CC} = 5 V | | 10 | 42 | |

wake-up LPM3

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------|------------|-----------------|-----------------------|-----|-----|-----|------|
| t _(LPM3) | Delay time | f = 1 MHz | V _{CC} = 3 V | | | 6 | μs |
| | | | V _{CC} = 5 V | | | | |
| | | f = 2 MHz | V _{CC} = 3 V | | | 6 | |
| | | | V _{CC} = 5 V | | | | |
| | | f = 3 MHz | V _{CC} = 5 V | | | 6 | |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

ADC supply current ($f_{ADCLK} = 1 \text{ MHz}$)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|-------------|-------------|--|-----|-----|-----|---------------|
| $I_{(ADC)}$ | ADC current | SV_{CC} on, current source off, $V_{CC} = 3 \text{ V}$ | | 200 | 400 | μA |
| $I_{(ADC)}$ | | SV_{CC} on, current source off, $V_{CC} = 5 \text{ V}$ | | 300 | 740 | μA |

SV_{CC} (switched AV_{CC})

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--------------|-----------------|---|--------------------------|-----|-----------|------------------|
| $V_{(SVCC)}$ | | SV_{CC} on, $I_{(SVCC)} = -8 \text{ mA}$, $V_{CC} = 2.5 \text{ V}$ | $V_{CC} - 0.2 \text{ V}$ | | V_{CC} | V |
| $I_{(SVCC)}$ | | SV_{CC} off, $SV_{CC} = 0 \text{ V}$, $V_{CC} = 5 \text{ V}$ | | | ± 0.1 | μA |
| $Z_{(SVCC)}$ | Input impedance | SV_{CC} off, $V_{CC} = 3 \text{ V}/5 \text{ V}$ | 40 | | 100 | $\text{k}\Omega$ |

current source (ADC)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|-------------------|--|---------------------------|---------------------------|---------------------------|---------------|
| $V_{(Rext)}$ | Voltage, (Rext) | $V_{(Rext)} = V_{(SVCC)} - V_{(RI)}$, $I_{(RI)} = 6 \text{ mA}$, $V_{CC} = 3 \text{ V}/5 \text{ V}$, | $0.246 \times V_{(SVCC)}$ | $0.249 \times V_{(SVCC)}$ | $0.252 \times V_{(SVCC)}$ | V |
| $R_{(ext)}$ | External resistor | $V_{CC} = 3 \text{ V}/5 \text{ V}$ | 95 | | 1600 | Ω |
| ΔI_S | Load compliance | $VA0..A3 = 0 \dots 0.4 \times V_{(SVCC)}$, $I_S = V_{(Rext)}/R_{(ext)} = 1 \text{ mA}$, $V_{CC} = 3 \text{ V}$, | -1 | | 1 | μA |
| | | $VA0..A3 = 0 \dots 0.4 \times V_{(SVCC)}$, $I_S = V_{(Rext)}/R_{(ext)} = 6 \text{ mA}$, $V_{CC} = 3 \text{ V}$, | -3.2 | | 3.2 | μA |
| | | $VA0..A3 = 0 \dots 0.5 \times V_{(SVCC)}$, $I_S = V_{(Rext)}/R_{(ext)} = 1 \text{ mA}$, $V_{CC} = 5 \text{ V}$, | -1.5 | | 1.5 | μA |
| | | $VA0..A3 = 0 \dots 0.5 \times V_{(SVCC)}$, $I_S = V_{(Rext)}/R_{(ext)} = 6 \text{ mA}$, $V_{CC} = 5 \text{ V}$, | -3.2 | | 3.2 | μA |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

A/D converter ($f_{ADCLK} = 1 \text{ MHz}$)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|--|--|---|----------------------------|----------------------------|--------|-------|------------------------------------|---------------------------------------|
| Resolution | | | | 12 + 2 | | | bits | |
| $f_{(con)}$ | Conversion frequency | $f_{(con)} = f_{ADCLK}$ | 12-bit conversion | $V_{CC} = 3 \text{ V/5 V}$ | 0.1 | 1.5 | MHz | |
| | | | 12+2-bit conversion | | 0.14 | 1.5 | | |
| $f_{(con cyc)}$ | Conversion cycles | $f_{ADCLK} = f_{(MCLK)}/N$ | 12-bit conversion | $V_{CC} = 3 \text{ V/5 V}$ | 96 | | cycles of ADCLK | |
| | | | 12+2-bit conversion | | 132 | | | |
| LSB Voltage | | | | $0.000061 \times V_{SVCC}$ | | | V | |
| INL ₁ | Integral nonlinearity (see Note 15) | 0 ≤ DDV ≤ 127 | | $V_{CC} = 3 \text{ V/5 V}$ | -2 | 2 | LSB | |
| INL ₂ | | 128 ≤ DDV ≤ 255 | | $V_{CC} = 3 \text{ V/5 V}$ | -3 | 3 | LSB | |
| INL ₃ | | 256 ≤ DDV ≤ 2047 | | $V_{CC} = 3 \text{ V/5 V}$ | -7 | 7 | LSB | |
| INL ₄ | | 2048 ≤ DDV ≤ 4095 | | $V_{CC} = 3 \text{ V/5 V}$ | -10 | 10 | LSB | |
| DNL | Differential nonlinearity (see Note 16) | | | $V_{CC} = 3 \text{ V/5 V}$ | -1 | 1 | LSB | |
| dN/dT | Temperature stability | $V_{(Rext)}/R_{(ext)} = 6 \text{ mA}$, Range A | | $V_{CC} = 3 \text{ V/5 V}$ | 0.008 | | LSB/°C | |
| | | Range B | | | 0.015 | | | |
| dN/dV(SVCC) | $V_{(SVCC)}$ rejection ratio | Range A, B, $V_{(Rext)}/R_{(ext)} = 1 \text{ mA}$, $SV_{CC} \pm 10\%$ | | $V_{CC} = 3 \text{ V/5 V}$ | 1.25 | | LSB/V | |
| Conversion offset 12 bit analog input to digital value (see Note 17) | Range A | | $V_{CC} = 3 \text{ V/5 V}$ | -1.2 | -0.49 | 0.24 | %FSR _A (see Note 18) | |
| | Range B | | $V_{CC} = 3 \text{ V/5 V}$ | -1.7 | -0.6 | 0.49 | %FSR _B (see Note 18) | |
| | Range C | | $V_{CC} = 3 \text{ V/5 V}$ | -1.8 | -0.6 | 0.6 | %FSR _C (see Note 18) | |
| | Range D | | $V_{CC} = 3 \text{ V/5 V}$ | -1.7 | 0.6 | 0.49 | %FSR _D (see Note 18) | |
| Conversion offset 14 bit analog input to digital value (see Note 17) | | Range ABCD | | $V_{CC} = 3 \text{ V/5 V}$ | -0.27 | -0.06 | 0.13 | %FSR _{ABCD} (see Note 18) |
| Slope 12 bit | | | | $V_{CC} = 3 \text{ V/5 V}$ | 0.9925 | 1 | 1.0075 | |
| Slope 14 bit | | | | $V_{CC} = 3 \text{ V/5 V}$ | 0.9982 | 1 | 1.0018 | |
| C(IN) | Input capacitance | | | $V_{CC} = 3 \text{ V/5 V}$ | 40 | 45 | pF | |
| R(SIN) | Serial input resistance | | | $V_{CC} = 3 \text{ V/5 V}$ | 2 | | kΩ | |

NOTES: 15. DDV is short form of delta digital value. The DDV is a span of conversion results. It is assumed that the conversion is of 12 bit not 12+2 bit.

16. DNL is valid for all 12-bit ranges and the 14-bit (12+2) range.

17. Offset referred to full scale 12/14 bit

18. FSRx: full scale range, separate for the four 12-bit ranges and the 14-bit (12+2) range.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

JTAG

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|----------------|--------------------------------------|---|---|-----|------|------|--------|
| f(TCK) | JTAG/test | TCK frequency | V _{CC} = 3 V | DC | 5 | MHz | |
| | | | V _{CC} = 5 V | DC | 10 | | |
| R(TEST) | | Pullup resistors on TMS, TCK, TDI (see Note 19) | V _{CC} = 3 V/ 5 V | 25 | 60 | 90 | kΩ |
| V(FB) | JTAG/fuse (see Note 20) | Fuse blow voltage, E/P versions (see Note 21) | V _{CC} = 3 V/ 5 V | 11 | | 12 | V |
| I(FB) | | Supply current on TDI to blow fuse | | | | 100 | mA |
| t(FB) | | Time to blow the fuse | | | | 1 | ms |
| V(PP) | EPROM (E) and OTP(P) – versions only | Programming voltage, applied to TDI/VPP | | 11 | 11.5 | 13 | V |
| I(PP) | | Current from programming voltage source | | | | 70 | mA |
| t(pps) | | Programming time, single pulse | | 5 | | | ms |
| t(ppf) | | Programming time, fast algorithm | | | 100 | | μs |
| P _n | | Number of pulses for successful programming | | 4 | | 100 | Pulses |
| | | Data retention T _J < 55°C | | 10 | | | year |
| t(erase) | | EPROM (E) versions only | Erase time wave length 2537 Å at 15 Ws/cm ² (UV lamp of 12 mW/ cm ²) | | 30 | | |
| | Write/Erase cycles | | 1000 | | | | cycles |

NOTES: 19. The TMS and TCK pullup resistors are implemented in all C-, P-, and E-versions.

20. Once the JTAG fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block switches to by-pass mode.

21. The voltage supply to blow the JTAG fuse is applied to TDI/VPP pin when fuse blowing is desired.

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TYPICAL CHARACTERISTICS

DIGITAL CONTROLLED OSCILLATOR FREQUENCY
vs
OPERATING FREE-AIR TEMPERATURE

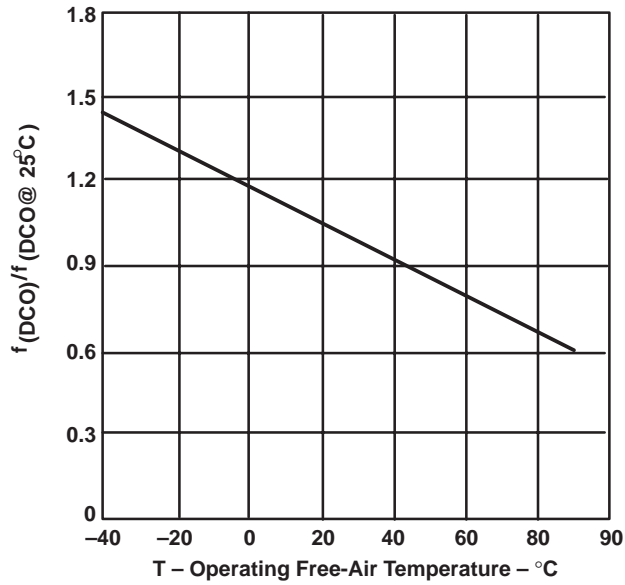


Figure 5

DIGITAL CONTROLLED OSCILLATOR FREQUENCY
vs
SUPPLY VOLTAGE

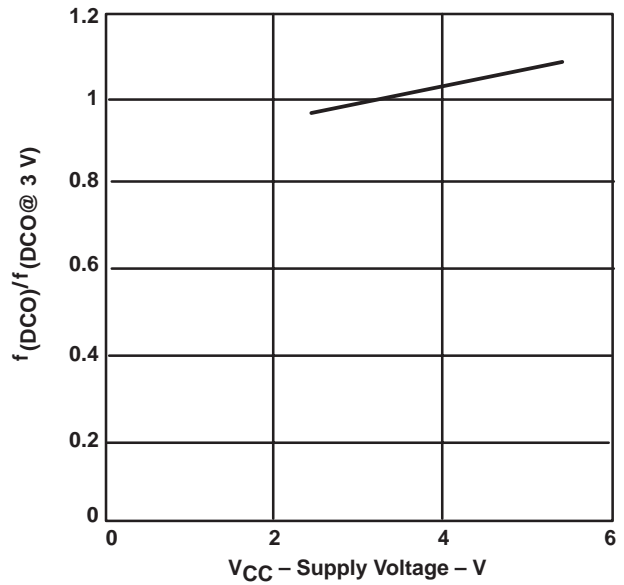
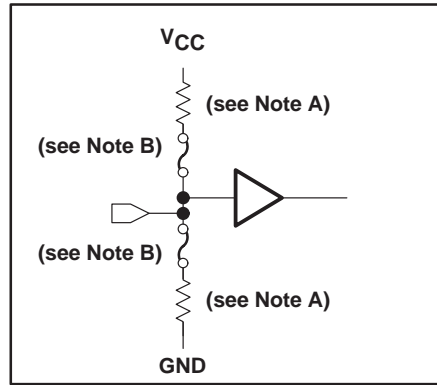


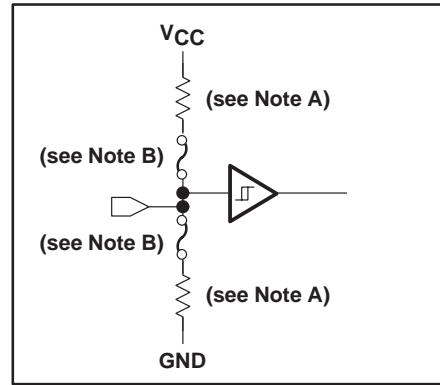
Figure 6

TYPICAL CHARACTERISTICS

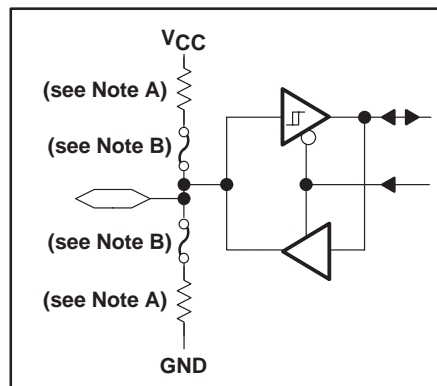
typical input/output schematics



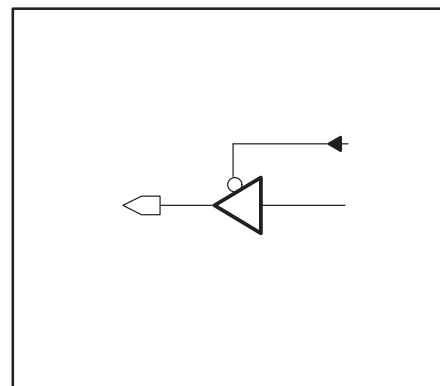
CMOS INPUT ($\overline{\text{RST/NMI}}$)



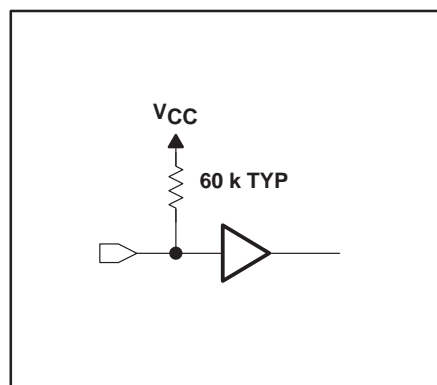
CMOS SCHMITT-TRIGGER INPUT (CIN)



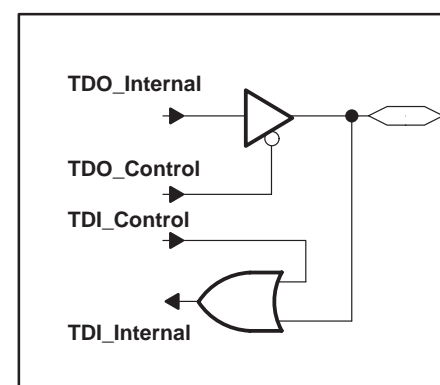
I/O WITH SCHMITT-TRIGGER INPUT (P0.x, TP5)



CMOS 3-STATE OUTPUT (TP0-4, XBUF)



MSP430P/E325: TMS, TCK



MSP430P/E325: TDO/TDI

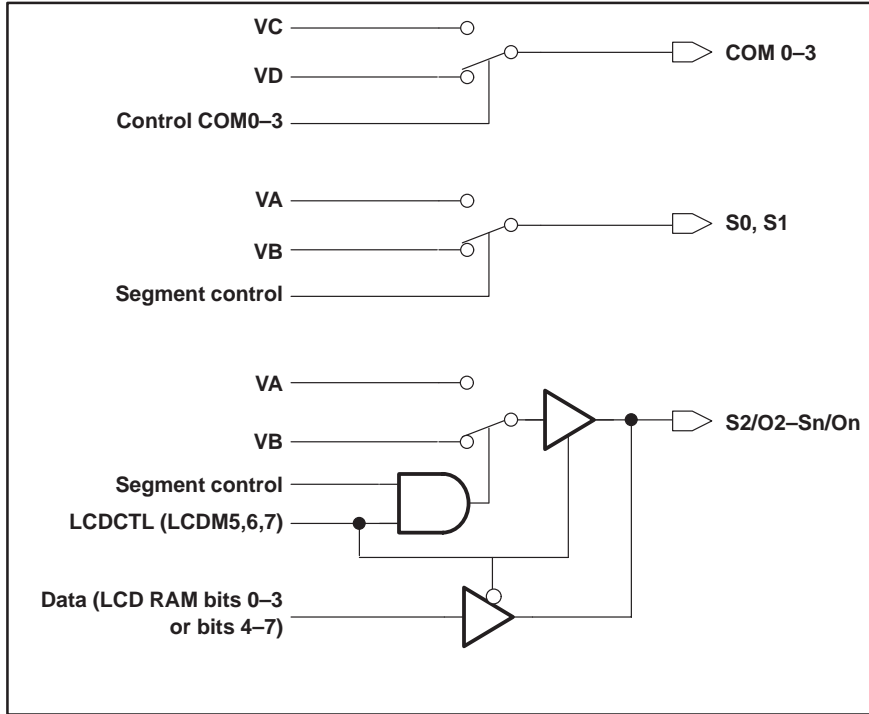
- NOTES: A. Optional selection of pullup or pulldown resistors with ROM (masked) versions. Anti-parallel diodes are connected between AV_{SS} and DV_{SS}.
B. Fuses for the optional pullup and pulldown resistors can only be programmed at the factory.

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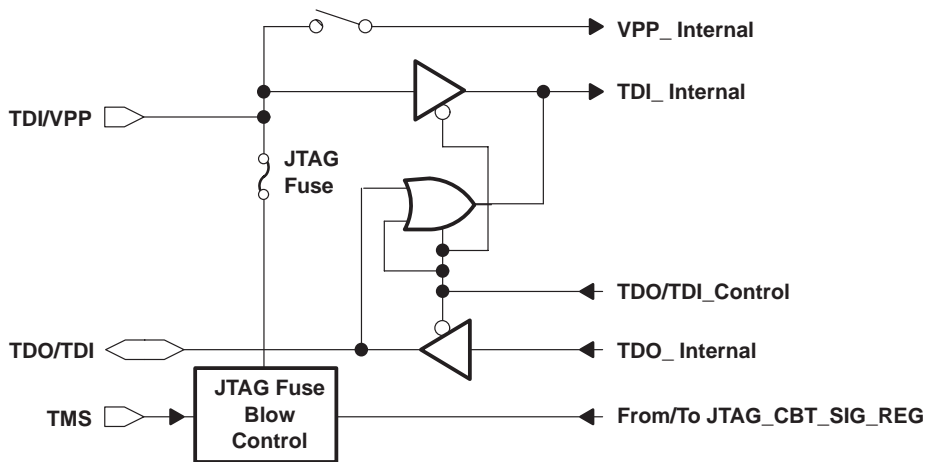
TYPICAL CHARACTERISTICS

typical input/output schematics



LCD OUTPUT (COM0-4, Sn, Sn/On)

NOTE: The signals VA, VB, VC, and VD come from the LCD module analog voltage generator.



- NOTES:
- A. During programming activity and when blowing the JTAG enable fuse, the TDI/VPP terminal is used to apply the correct voltage source. The TDO/TDI terminal is used to apply the test input data for JTAG circuitry.
 - B. The TDI/VPP terminal of the 'P325 and 'E325 does not have an internal pullup resistor. An external pulldown resistor is recommended to avoid a floating node which could increase the current consumption of the device.
 - C. The TDO/TDI terminal is in a high-impedance state after POR. The 'P325 and 'E325 needs a pullup or a pulldown resistor to avoid floating a node which could increase the current consumption of the device.

Figure 7. MSP430P325/E325: TDI/VPP, TDO/TDI

TYPICAL CHARACTERISTICS

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/VPP terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/VPP pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power-up or if TMS is being held low during power-up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.



Figure 8. Fuse Check Mode Current, MSP430P/E325

Care must be taken to avoid accidentally activating the fuse check mode, including guarding against EMI/ESD spikes that could cause signal edges on the TMS pin.

Configuration of TMS, TCK, TDI/VPP and TDO/TDI pins in applications.

| | P/E3xx |
|-----|---------------|
| TDI | 68k, pulldown |
| TDO | 68k, pulldown |
| TMS | Open |
| TCK | Open |

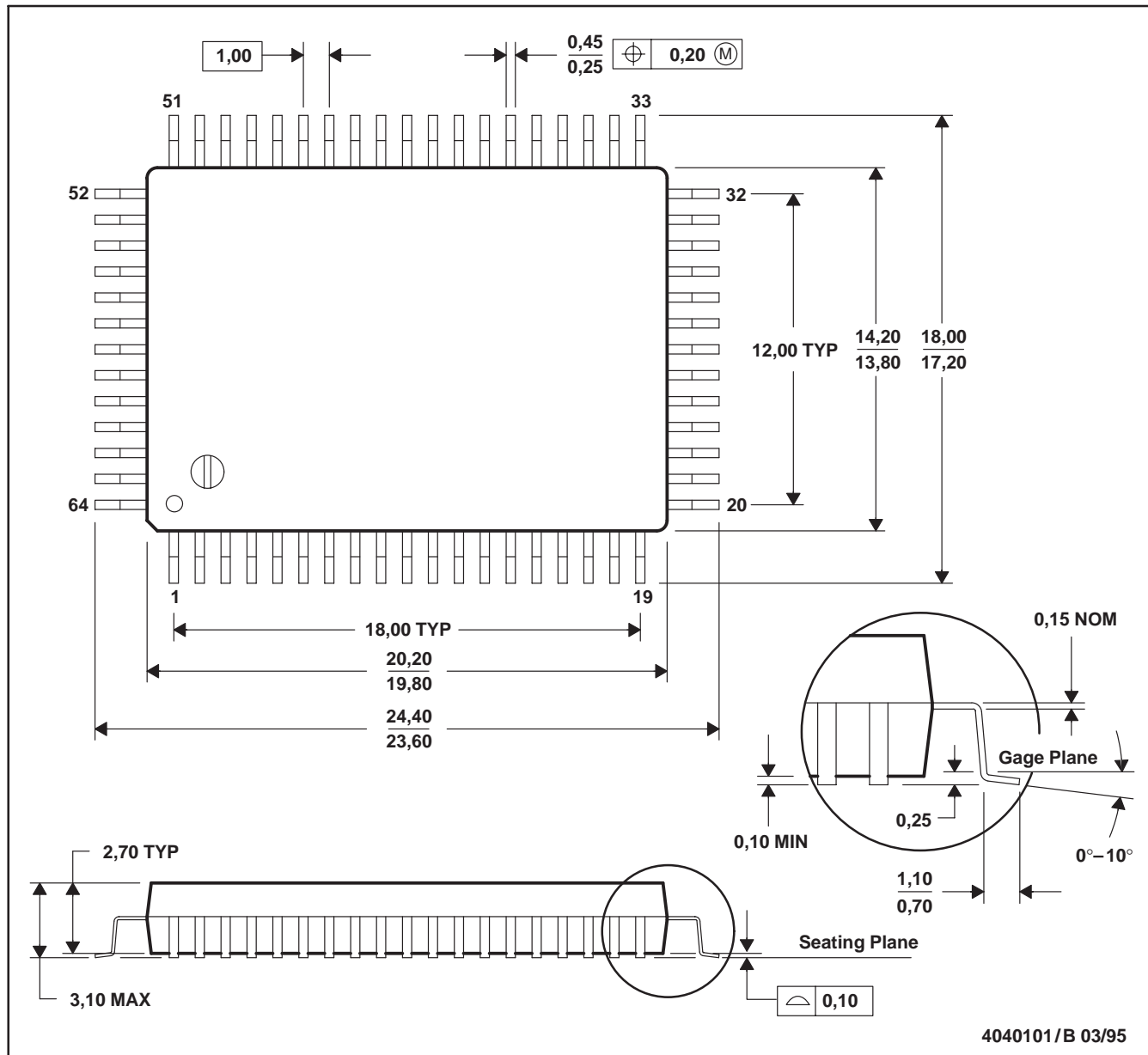
MSP430P325 MIXED SIGNAL MICROCONTROLLER

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MECHANICAL DATA

PG (R-PQFP-G64)

PLASTIC QUAD FLATPACK



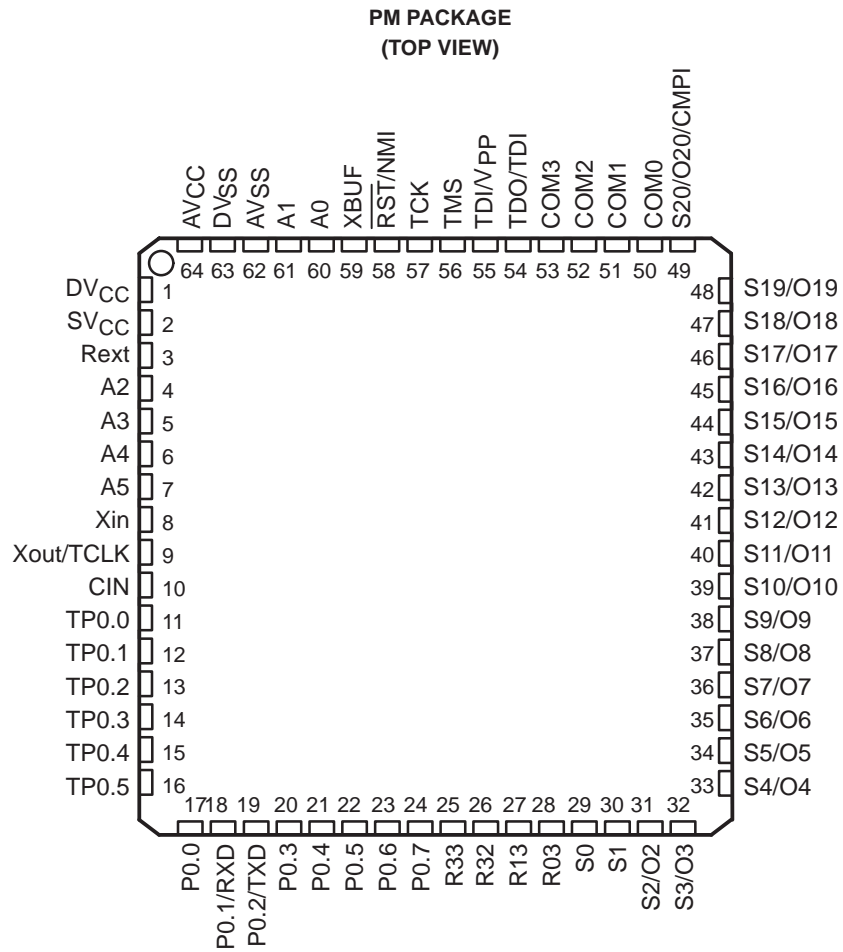
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

MSP430P325 MIXED SIGNAL MICROCONTROLLER

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MECHANICAL DATA

MSP430P325 (PM package)



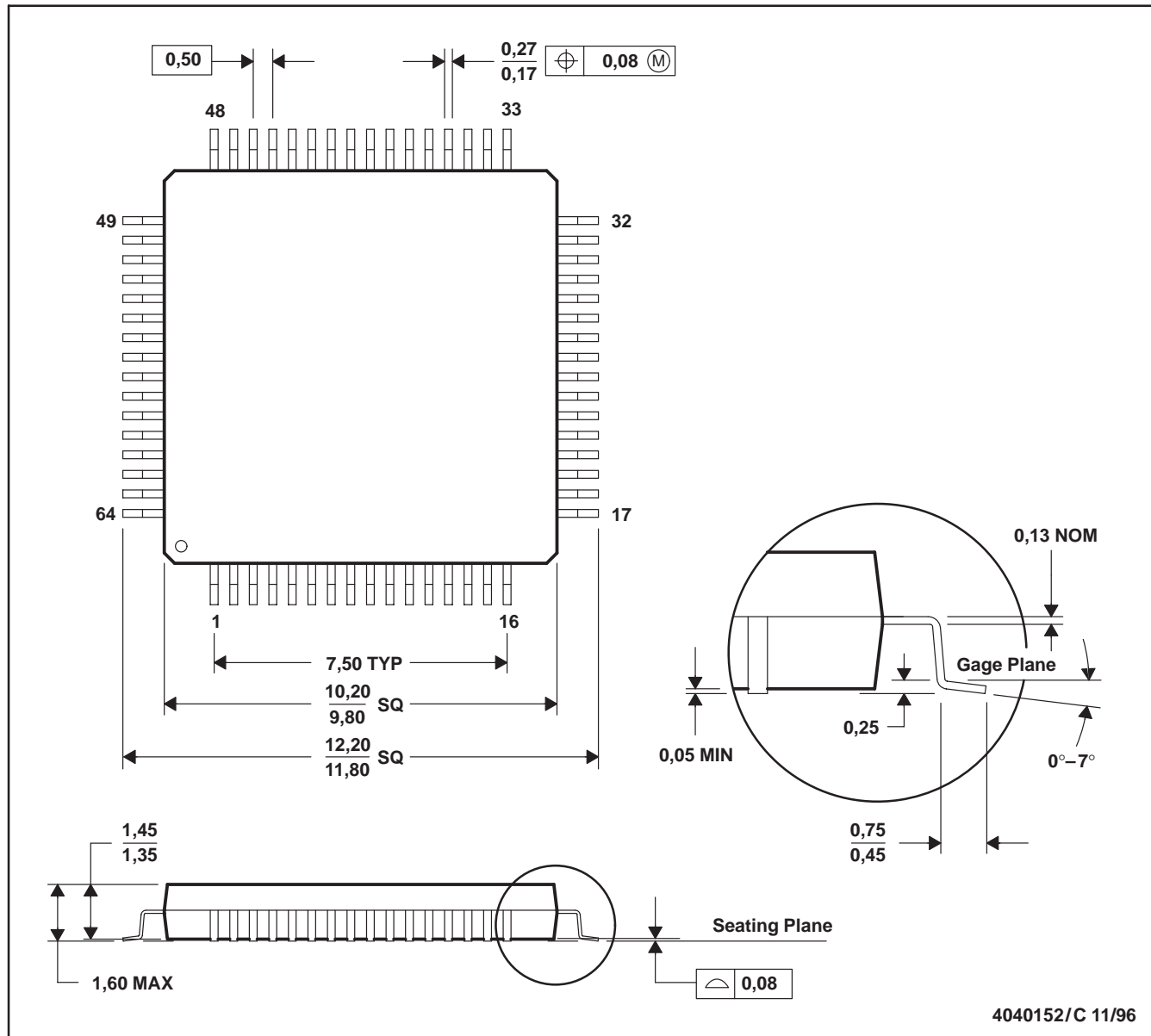
MSP430P325 MIXED SIGNAL MICROCONTROLLER

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MECHANICAL DATA

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



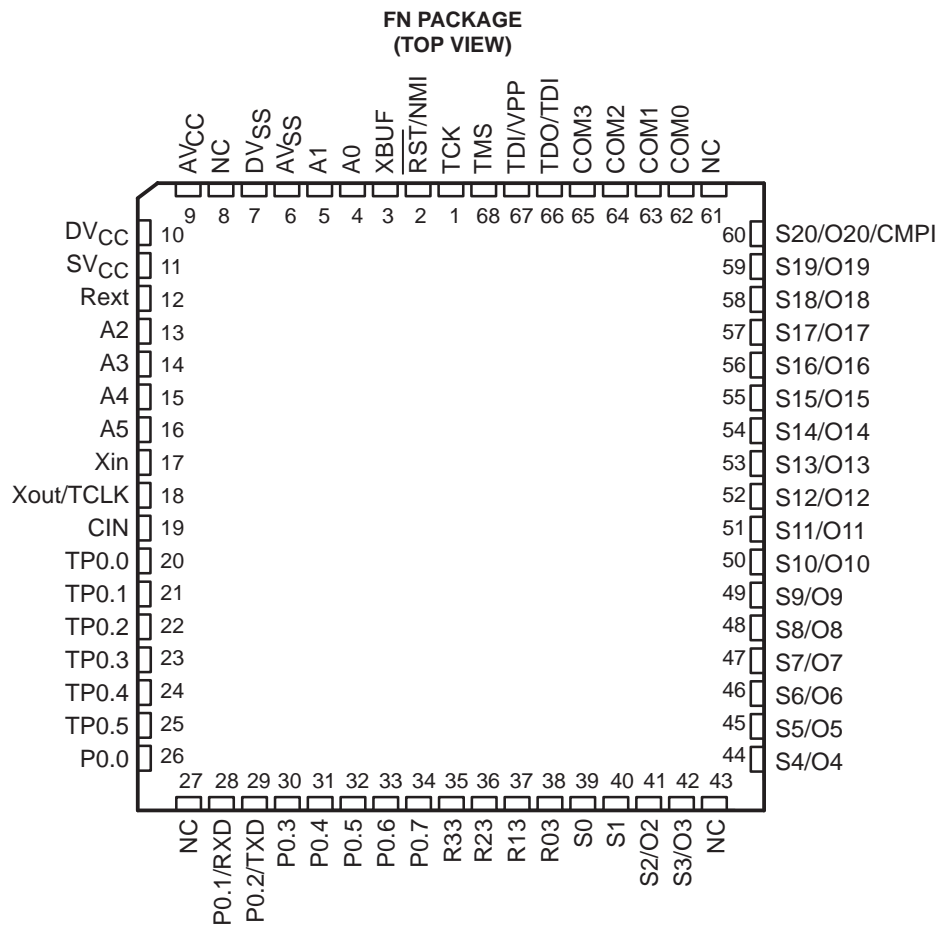
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026
 - D. May also be thermally enhanced plastic with leads connected to the die pads.

MSP430P325 MIXED SIGNAL MICROCONTROLLER

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MECHANICAL DATA

MSP430P325 (FN package)



NC – No internal connection

MSP430P325 MIXED SIGNAL MICROCONTROLLER

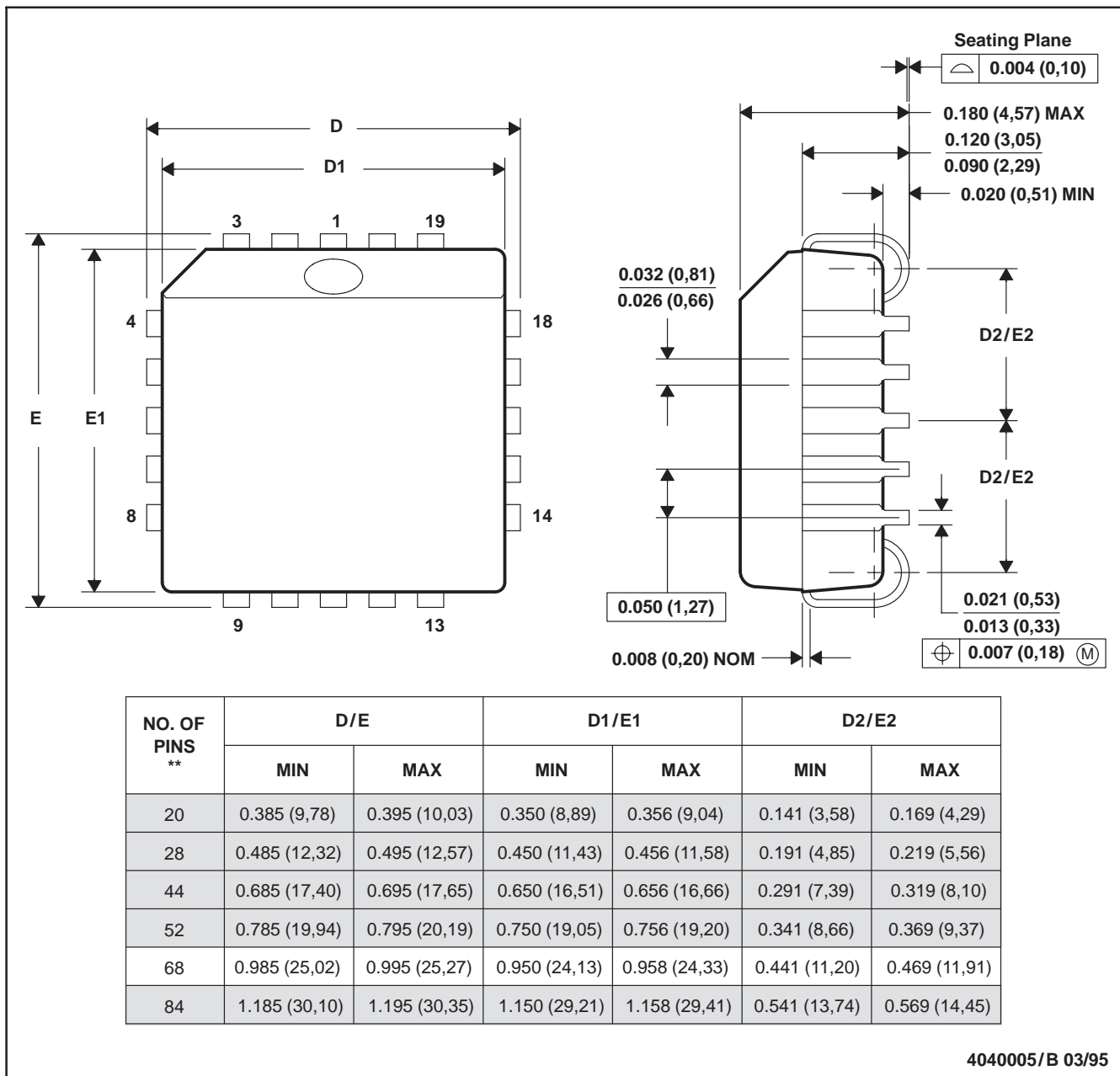
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MECHANICAL DATA

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



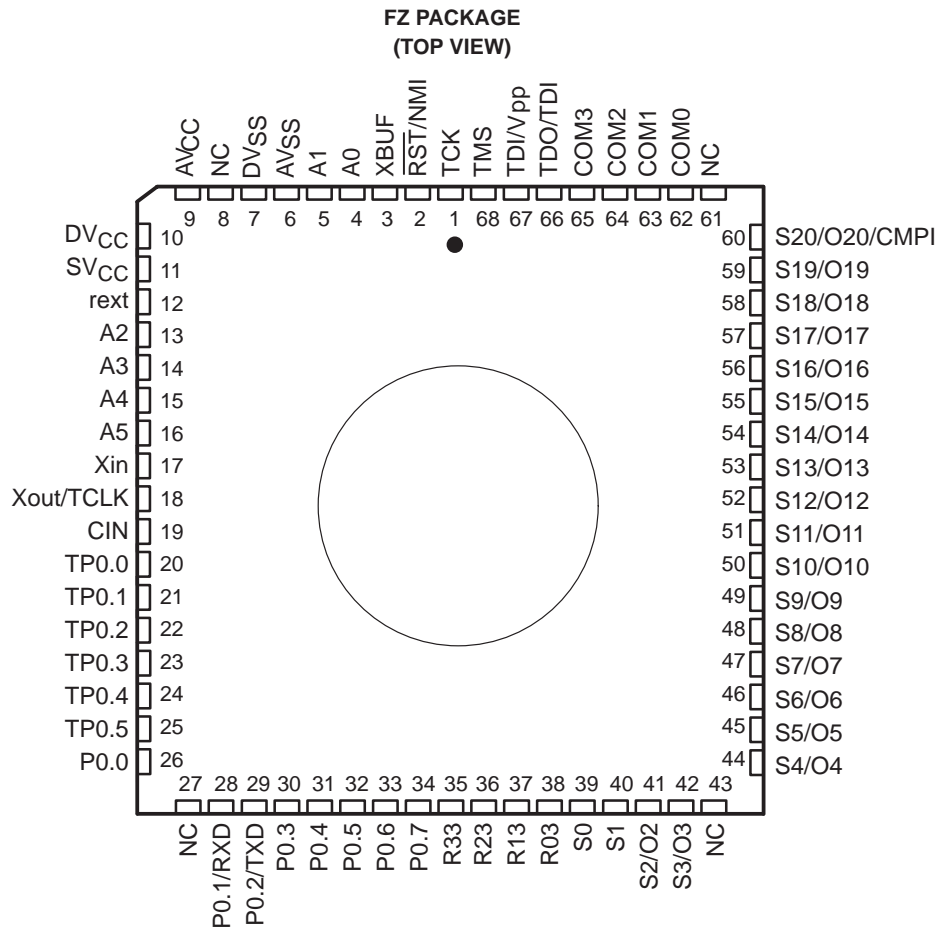
4040005/B 03/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

MSP430P325 MIXED SIGNAL MICROCONTROLLER

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PMS430E325 (FZ package)



NC – No internal connection

MSP430P325 MIXED SIGNAL MICROCONTROLLER

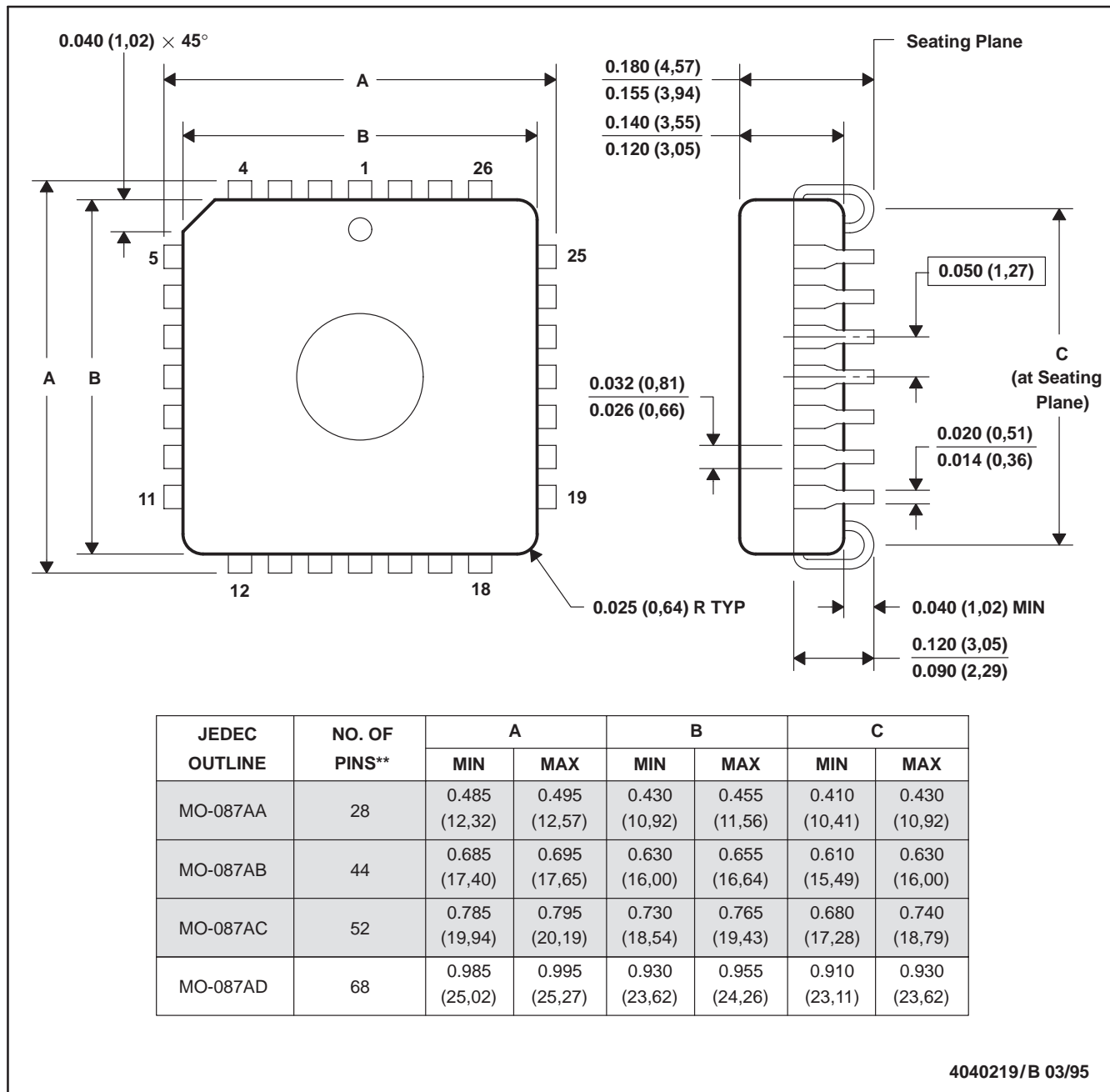
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MECHANICAL DATA

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.

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