NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT
ISL6232 (Available Feb. 2004)

August 2004 FN9032.1

Advanced Triple PWM and Dual Linear Power Controller for Portable Applications

The IPM6220A provides a highly integrated power control and protection solution for five output voltages required in high-performance notebook PC applications. The IC integrates three fixed frequency pulse-width-modulation (PWM) controllers and two linear regulators along with monitoring and protection circuitry into a single 24 lead SSOP package.

The two PWM controllers that regulate the system main 5V and 3.3V voltages are implemented with synchronous-rectified buck converters. Synchronous rectification and hysteretic operation at light loads contribute to high efficiency over a wide range of input voltage and load variation. Efficiency is further enhanced by using the lower MOSFET's $r_{DS(ON)}$ as the current sense element. Input voltage feed-forward ramp modulation, current-mode control, and internal feed-back compensation provide fast and stable handling of input voltage load transients encountered in advanced portable computer chip sets.

The third PWM controller is a boost converter that regulates a resistor selectable output voltage of nominally 12V.

Two internal linear regulators provide +5V ALWAYS and +3.3V ALWAYS low current outputs required by the notebook system controller.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
IPM6220ACA	-10 to 85	24 Ld SSOP	M24.15
IPM6220ACAZ (Note)	-10 to 85	24 Ld SSOP (Pb-free)	M24.15
IPM6220ACAZ-T (Note)	-10 to 85	24 Ld SSOP Tape & Reel (Pb-free)	M24.15
IPM6220ACAZA-T (Note)	-10 to 85	24 Ld SSOP Tape & Reel (Pb-free)	M24.15
IPM6220EVAL1	Evaluation Board		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

- Provides Five Regulated Voltages
  - +5V ALWAYS
  - +3.3V ALWAYS
  - +5V Main
  - +3.3V Main
  - +12V
- High Efficiency Over Wide Line and Load Range
  - Synchronous Buck Converters on Main Outputs
  - Hysteretic Operation at Light Load
- No Current-Sense Resistor Required
  - Uses MOSFET's $r_{DS(ON)}$
  - Optional Current-Sense Resistor for More Precision
- Operates Directly From Battery 5.6 to 22V Input
- Input Undervoltage Lock-Out (UVLO)
- Excellent Dynamic Response
  - Voltage Feed-Forward and Current-Mode Control
- Monitors Output Voltages
- Synchronous Converters Operate Out of Phase
- Separate Shut-Down Pins for Advanced Configuration and Power Interface (ACPI) Compatibility
- 300kHz Fixed Switching Frequency on Main Outputs
- Thermal Shut-Down Protection
- Pb-free Available

Applications

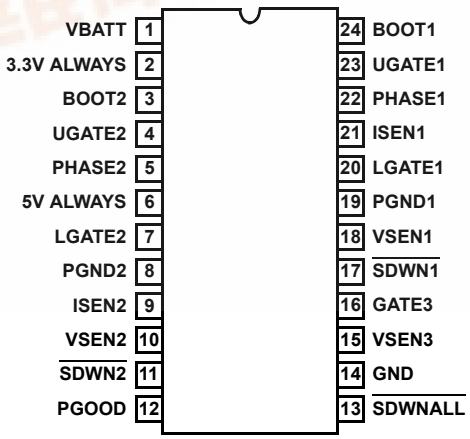
- Mobile PCs
- Hand-Held Portable Instruments

Related Literature

- Application Note AN9915

Pinout

IPM6220A (SSOP)
TOP VIEW



Block Diagram

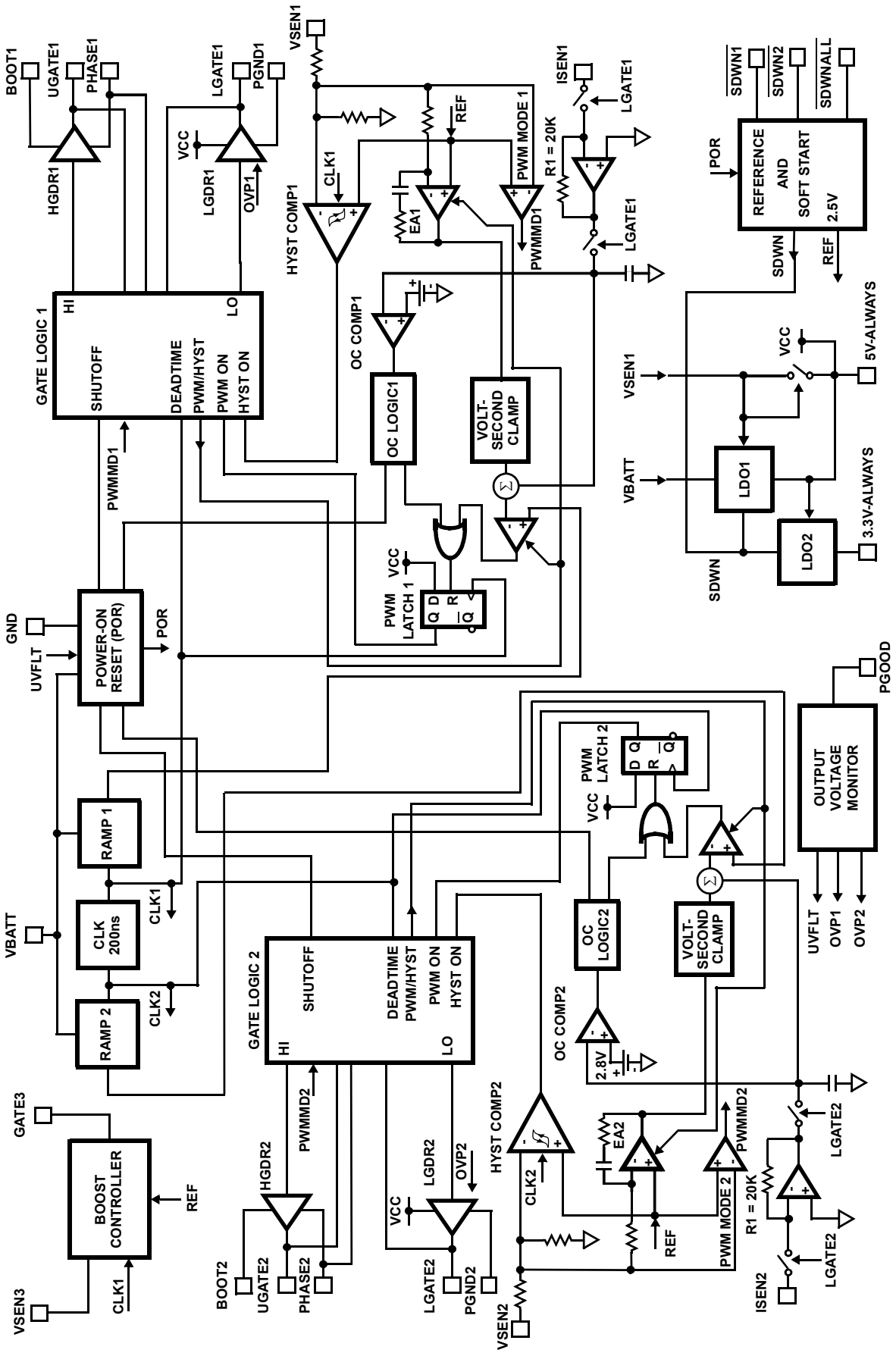


FIGURE 1.

Simplified Power System Diagram

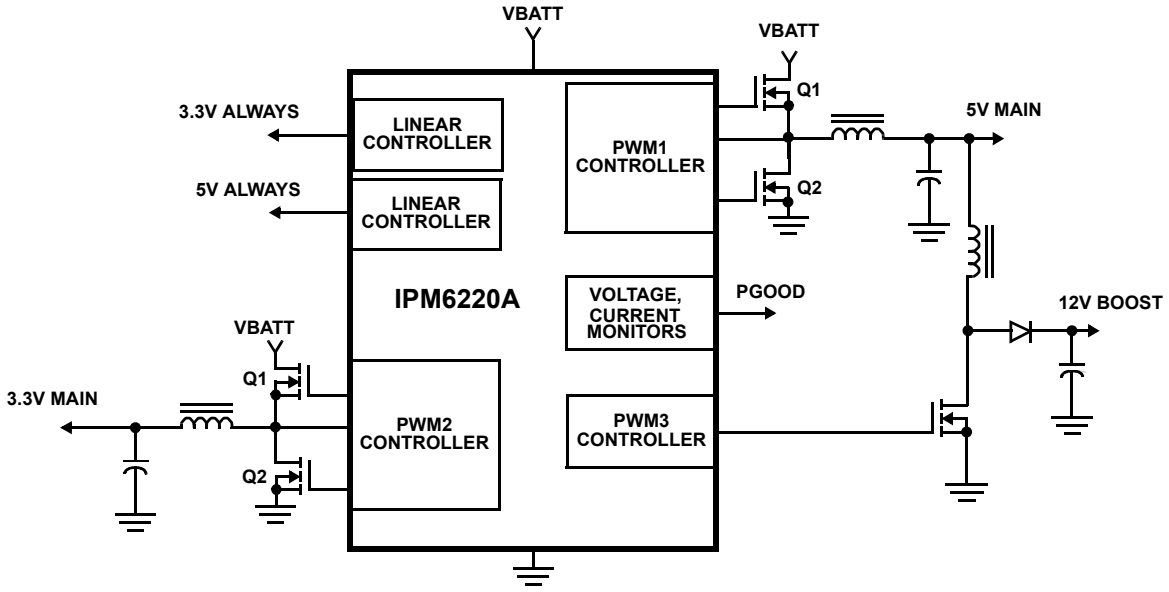


FIGURE 2.

Typical Application

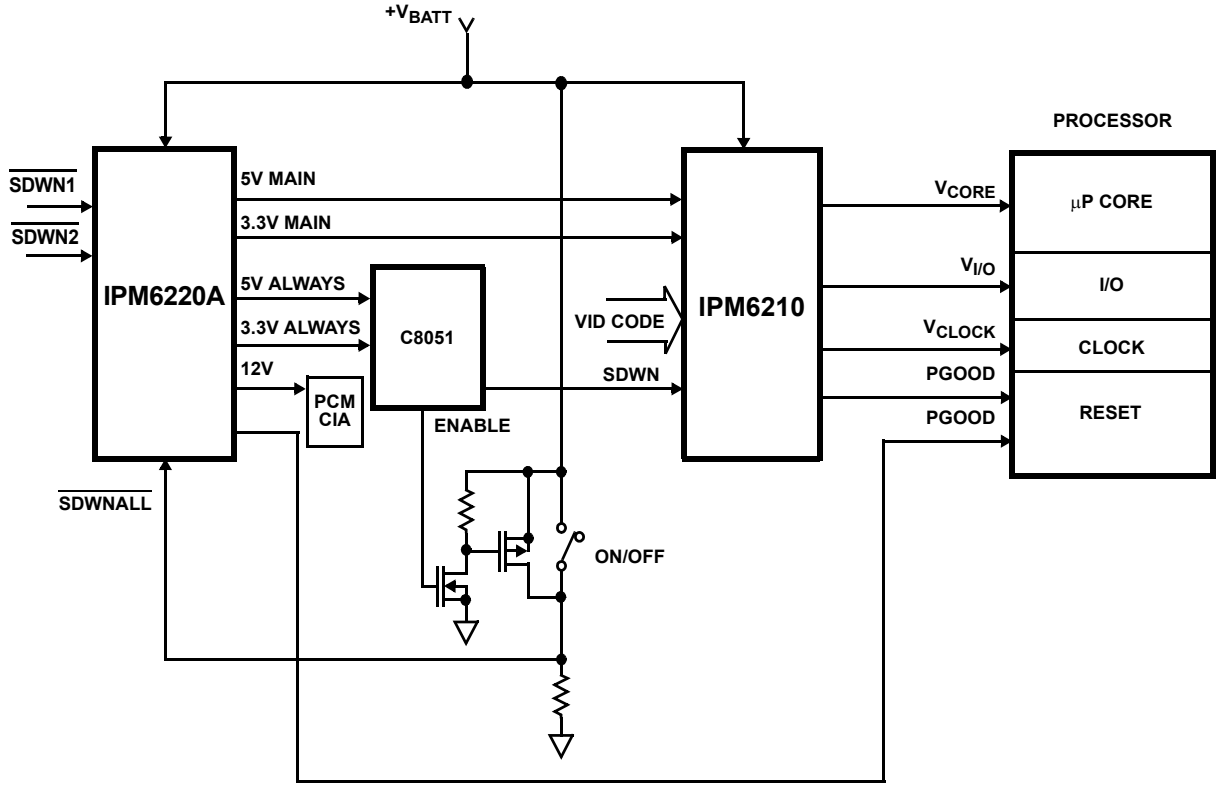


FIGURE 3.

Absolute Maximum Ratings

Input Voltage, VBATT . . . . . +27.0V
Phase, ISEN and $\overline{\text{SDWNALL}}$ Pins . . . . . GND -0.3V to +27.0V
Boot and UGATE Pins. . . . . +33.0V
BOOT1, 2 with Respect to PHASE1, 2 . . . . . +6.5V
All Other Pins. . . . . +6.5V

Operating Conditions

Input Voltage, VBATT . . . . . +5.6V to +24.0V
Ambient Temperature Range . . . . . -10°C to 85°C
Junction Temperature Range. . . . . 0°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SSOP Package 110
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Quiescent Current	I_{CC}	$\overline{\text{SDWN1}}$ = $\overline{\text{SDWN2}}$ = 5V, $\overline{\text{SDWNALL}}$ = VIN, Outputs open circuited	-	1.4	2.0	mA
Stand-by Current	I_{CCSB}	$\overline{\text{SDWN1}}$ = $\overline{\text{SDWN2}}$ = 0V, $\overline{\text{SDWNALL}}$ = VIN, Outputs open circuited	-	300		µA
Shut-down Current	I_{CCSN}	$\overline{\text{SDWNALL}}$ = 0V	-	<1.0		µA
Input Under-voltage Lock Out	UVLO	Rising VBATT	4.3	4.7	5.1	V
Input Under-voltage Lock Out	UVLO	VBATT, Hysteresis		300		mV
OSCILLATOR						
PWM1,2 Oscillator Frequency	$F_{c1,2}$		255	300	345	kHz
REFERENCE AND SOFT START						
Internal Reference Voltage	V_{REF}		-	2.472	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
SDWN1, SDWN2 Output Current During Start-up	I_{SS}		-	5	-	µA
PWM1 CONVERTER, 5V Main						
Output Voltage	V_{OUT1}			5.0		V
Line and Load Regulation		0.0 < IVOUT1 < 5.0A; 5.6V < VBATT < 22.0V	-2	0.5	+2	%
Under-Voltage Shut-Down Level	V_{UV1}	2µs delay, % Feedback Voltage at VSNS1 pin	70	75	80	%
Current Limit Threshold	I_{OC2}	Current from ISNS1 Pin Through RSNS1	90	135	180	µA
Over-Voltage Threshold	V_{OVP1}	2µs delay, % Feedback Voltage at VSNS1 pin	110	115	120	%
Maximum Duty Cycle	DC_{MAX}	SDWN1 > 4.0V		94		%
PWM2 CONVERTER, 3.3V Main						
Output Voltage	VOUT2			3.3		V
Line and Load Regulation		0.0 < IVOUT2 < 5.0A; 5.6V < VBATT < 24.0V	-2	0.5	+2	%
Under-Voltage Shut-Down Level	V_{UV2}	2µs delay, % Feedback Voltage at VSNS2 pin	70	75	80	%
Current Limit Threshold	I_{OC2}	Current from ISNS2 Pin Through RSNS2	90	135	180	µA
Over-Voltage Threshold	V_{OVP2}	2µs delay, % Feedback Voltage at VSNS2 pin	110	115	120	%
Maximum Duty Cycle	DC_{MAX}	SDWN2 > 4.0V		94		%
Internal Resistance to GND on VSNS2 Pin	R_{VSNS2}			66K		Ω

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM1 and PWM2 CONTROLLER GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}		-	5	12	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}		-	4	10	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}		-	6	9	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}		-	5	8	Ω
PWM 3 CONVERTER						
12V Feedback Regulation Voltage	VSEN3			2.472		V
12V Feedback Regulation Voltage Input Current	I_{VSEN3}			0.1	1.0	µA
Line and Load Regulation		0.0 < IV_{OUT3} < 120mA, 4.9V< $5V_{Main}$ <5.1V	-2		+2	%
Under-Voltage Shut-Down Level	V_{UV3}	2µs delay, % Feedback Voltage at VSNS3 pin	70	75	80	%
Over-Voltage Threshold	V_{OVP3}	2µs delay, % Feedback Voltage at VSNS3 pin		115	120	%
PWM3 Oscillator Frequency	F_{c3}		85	100	115	kHz
Maximum Duty Cycle				33		%
PWM 3 CONTROLLER GATE DRIVERS						
Pull-Up Resistance	R3GPUP			6	12	Ω
Pull-Down Resistance	R3GPDN			6	12	Ω
5V and 3.3V ALWAYS						
Linear Regulator Accuracy		PWM1, 5V Output OFF ($\overline{SDWN1}$ = 0V); 5.6V < VBATT < 22V; 0 < I_{LOAD} < 50mA	-2.0	0.5	+2.0	%
5V ALWAYS Output Voltage Regulation		PWM1, 5V Output ON ($\overline{SDWN1}$ = 5V); 0 < I_{LOAD} < 50mA	-3.3	1.0	+2.0	%
Maximum Output Current		Combined 5V ALWAYS and 3.3V ALWAYS	50			mA
Current Limit		Combined 5V ALWAYS and 3.3V ALWAYS	100	180		mA
5V ALWAYS Under-Voltage Shut-Down				75		%
Bypass Switch $r_{DS(ON)}$		PWM1, 5V Output ON ($\overline{SDWN1}$ = 5V)		1.3		Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power Good Threshold for PWM1 and PWM2 Output Voltages			-14	-12	-10	%
PGOOD Leakage Current	I_{PGLKG}	VPULLUP = 5.0V	-	-	1.0	µA
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA		0.2	0.5	V
PGOOD Minimum Pulse Width	T_{PGmin}			10		µs
$\overline{SDWN1, 2}$, - Low (Off)				0.8		V
$\overline{SDWN1, 2}$, - High (On)				4.3		V
$\overline{SDWNALL}$ - High (On)				2.4		V
$\overline{SDWNALL}$ - Low (Off)		SDWNALL, Hysteresis		40		mV
Over-Temperature Shutdown				150		°C
Over-Temperature Hysteresis				25		°C

Functional Pin Descriptions

VBATT (Pin 1)

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds 4.7V and stops operating when the voltage on this pin drops below approximately 4.5V. Also provides battery voltage to the oscillator for feed-forward rejection to input voltage variations.

3.3V ALWAYS (Pin 2)

Output of 3.3V ALWAYS linear regulator.

5V ALWAYS (Pin 6)

Output of 5V ALWAYS linear regulator or the +5V Main output. If the +5V Main output is enabled, it is switched internally from the VSEN1 pin to the 5V ALWAYS output. This improves efficiency and reduces the power dissipation in the controller.

BOOT1, BOOT2 (Pins 24 and 3)

Power is supplied to the upper MOSFET drivers of PWM1 and PWM2 converters via the BOOT pins. Connect these pins to the respective junctions of bootstrap capacitors with the cathodes of the bootstrap diodes. Anodes of the bootstrap diodes are connected to pin 6, 5V ALWAYS.

UGATE1, UGATE2 (Pins 23 and 4)

These pins provide the gate drive for the upper MOSFETs. Connect UGATE pins to the respective PWM converter's upper MOSFET gate.

PHASE1, PHASE2 (Pins 22 and 5)

The phase nodes are the junctions of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect the PHASE pins directly to the respective PWM converter's lower MOSFET drain.

ISEN1, ISEN2 (Pins 21 and 9)

These pins are used to monitor the voltage drop across the lower MOSFETs for current feedback and current-limit protection. For more precise current detection, these inputs can be connected to optional current sense resistors placed in series with the sources of the lower MOSFETs.

LGATE1, LGATE 2 (Pins 20 and 7)

These pins provide the gate drive for the lower MOSFETs. Connect the lower MOSFET gate of each converter to the corresponding pin.

PGND1, PGND2 (Pins 19 and 8)

These are the lower MOSFET gate drive return connection for PWM1 and PWM2 converters, respectively. Tie each lower MOSFET source directly to the corresponding pin.

VSEN1, VSEN2 (Pins 18, 10)

These pins are connected to the main outputs and provide the voltage feedback signal for the respective PWM controllers. The PGOOD, overvoltage protection (OVP) and undervoltage shutdown circuits use these signals to determine output-voltage status and/or to initiate undervoltage shut down. The VSEN1 input is also switched internally to the 5V ALWAYS output if the +5V Main output is enabled.

$\overline{\text{SDWNALL}}$ (Pin 13)

This pin provides enable/disable function for all outputs. The chip is completely disabled when this pin is pulled to ground. When this pin is pulled high, the 5V ALWAYS and 3.3 ALWAYS outputs are on and the other outputs are enabled. The state of 5V Main and 3.3V Main outputs depend on the voltage on $\overline{\text{SDWN1}}$ and $\overline{\text{SDWN2}}$ respectively. See Table 1.

$\overline{\text{SDWN1}}$ (Pin 17)

This pin provides enable/disable function and soft-start for the PWM1, 5V Main, output. The output is enabled when this pin is high and $\overline{\text{SDWNALL}}$ is also high. The 5V output is held off when the pin is pulled to the ground.

$\overline{\text{SDWN2}}$ (Pin 11)

This pin provides enable/disable function and soft-start for PWM2, 3.3V Main, output. The output is enabled when this pin is high and $\overline{\text{SDWNALL}}$ is also high. The 3.3V output is held off when the pin is pulled to the ground.

VSEN3 (Pin 15)

This input pin is the voltage feedback signal for PWM3, the boost controller. The boost controller regulates this point to a voltage divided level of 2.472 VDC. The PGOOD, overvoltage protection (OVP) and undervoltage shutdown circuits use this signal to determine output-voltage status and/or to initiate undervoltage shut down.

This pin can also be used to independently disable the PWM3 controller. Connect this pin to 5V ALWAYS if the boost converter is not populated in your design.

GATE3 (Pin 16)

This pin drives the gate of the boost MOSFET.

PGOOD (Pin 12)

PGOOD is an open drain output used to indicate the status of the PWM converters' output voltages. This pin is pulled low when any of the outputs except PWM3 (12V) is not within -10% of respective nominal voltages, or when PWM3 (12V) is not within its undervoltage and overvoltage thresholds.

GND (Pin 14)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

General Description

The IPM6220A addresses the system electronics power needs of modern notebook and sub-notebook PCs. The IC integrates control circuits for two synchronous buck

converters for 5V Main and 3.3V Main buses, two linear regulators for 3.3V ALWAYS and 5V ALWAYS, and a 12V boost converter.

The two synchronous converters operate out of phase to substantially reduce the input-current ripple, minimizing input filter requirements, minimizing battery heating and prolonging battery life.

The 12V boost controller uses a 100kHz clock derived from the main clock. This controller uses leading edge modulation with the maximum duty cycle limited to 33%.

The chip has three input control lines $\overline{\text{SDWN1}}$, $\overline{\text{SDWN2}}$ and $\overline{\text{SDWNALL}}$. These are provided for Advanced Configuration and Power Interface (ACPI) compatibility. They turn on and off all outputs, as well as provide independent control of the 3.3V Main and +5V Main outputs.

To maximize efficiency for the 5V Main and 3.3V Main outputs, the current-sense technique is based on the lower MOSFET $r_{DS(ON)}$. Light-load efficiency is further enhanced by a hysteretic mode of operation which is automatically engaged at light loads when the inductor current becomes discontinuous.

3.3V Main and 5V Main Architecture

These main outputs are generated from the unregulated battery input by two independent synchronous buck converters. The IC integrates all the components required for output voltage setpoint and feedback compensation, significantly reducing the number of external components, saving board space and parts cost.

The buck PWM controllers employ a 300kHz fixed frequency current-mode control scheme with input voltage feed-forward ramp programming for better rejection of input voltage variations.

Figure 4 shows the out-of-phase operation for the 3.3V Main and 5V Main outputs. The phase node is the junction of the upper MOSFET, lower MOSFET and the output inductor. The phase node is high when the upper MOSFET is conducting and the inductor current rises accordingly. When the phase node is low, the lower MOSFET is conducting and the inductor current is ramping down as shown.

Current Sensing and Current Limit Protection

Both PWM converters use the lower MOSFET on-state resistance, $r_{DS(ON)}$, as the current-sensing element. This technique eliminates the need for a current sense resistor and the associated power losses. If more accurate current protection is desired, current sense resistors may be used in series with the lower MOSFETs' source.

To set the current limit, place a resistor, RSNS, between the ISEN inputs and the drain of the lower MOSFET (or optional current sense resistor). The required value of the RSNS resistor is determined from the following equation:

$$RSNS = \frac{Rcs}{135\mu A}\left(Iocdc + \frac{Vo}{L \times 2 \times 300kHz}\right) - 100$$

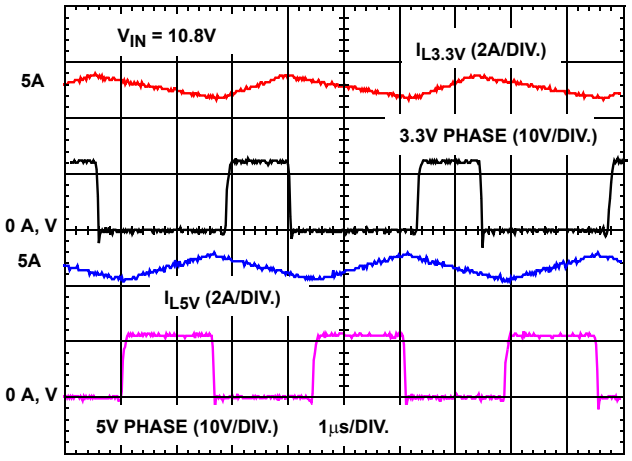


FIGURE 4. OUT OF PHASE OPERATION

where IOCDC is the desired DC overcurrent limit; RCS is either the $r_{DS(ON)}$ of the lower MOSFET, or the value of the optional current-sense resistor, Vo is the output voltage and L is the output inductor. Also, the value of RCS should be specified for the expected maximum operating temperature.

The sensed voltage, and the resulting current out of the ISEN pin through RSNS, is used for current feedback and current limit protection. This is compared with an internal current limit threshold. When a sampled value of the output current is determined to be above the current limit threshold, the PWM drive is terminated and a counter is initiated. This limits the inductor current build-up and essentially switches the converter into current-limit mode. If an overcurrent is detected between 26µs to 53µs later, an overcurrent shutdown is initiated. If during the 26µs to 53µs period, an overcurrent is not detected, the counter is reset and sampling continues as normal.

This current limit scheme has proven to be very robust in applications like portable computers where fast inductor current build-up is common due to a large difference between input and output voltages and a low value of the inductor.

Light-Load (Hysteretic) Operation

In the light-load (hysteretic) mode the output voltage is regulated by the hysteretic comparator which regulates the output voltage by maintaining the output voltage ripple as shown in Figure 5. In Hysteretic mode, the inductor current flows only when the output voltage reaches the lower limit of the hysteretic comparator and turns off at the upper limit. Hysteretic mode saves converter energy at light loads by supplying energy only at the time when the output voltage requires it. This mode conserves energy by reducing the power dissipation associated with continuous switching.

During the time between inductor current pulses, both the upper and lower MOSFETs are turned off. This is referred to as ‘diode emulation mode’ because the lower MOSFET performs the function of a diode. This diode emulation mode prevents the output capacitor from discharging through the lower MOSFET when the upper MOSFET is not conducting.

The gate drive is synchronized to the main clock, so the out-of-phase timing is maintained in hysteretic mode. Such a scheme insures a seamless transition between the operational modes.

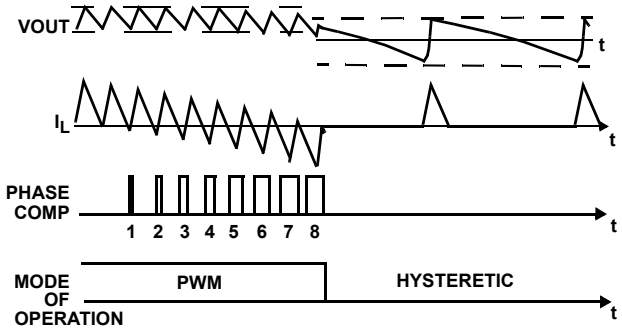


FIGURE 5. REGULATION IN HYSTERETIC MODE

Operation-Mode Control

The mode-control circuit changes the converter’s mode of operation based on the voltage polarity of the phase node when the lower MOSFET is conducting and just before the upper MOSFET turns on. For continuous inductor current, the phase node is negative when the lower MOSFET is conducting and the converters operate in fixed-frequency PWM mode as shown in Figure 6. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the ‘reverse’ direction, the phase node becomes positive, and the mode is changed to hysteretic.

A phase comparator handles the timing of the phase node voltage sensing. A low level on the phase comparator output indicates a negative phase voltage during the conduction time of the lower MOSFET. A high level on the phase comparator output indicates a positive phase voltage.

When the phase node is positive (phase comparator high), at the end of the lower MOSFET conduction time, for eight consecutive clock cycles, the mode is changed to hysteretic as shown in Figure 6. The dashed lines indicate when the phase node goes positive and the phase comparator output goes high. The solid vertical lines at 1,2,...8 indicate the sampling time, of the phase comparator, to determine the polarity (sign) of the phase node. At the transition between PWM and hysteretic mode, both the upper and lower MOSFETs are turned off. The phase node will ‘ring’ based on the output inductor and the parasitic capacitance on the phase node and settle out at the value of the output voltage.

The mode change from hysteretic to PWM can be caused by one of two events. One event is the same mechanism that causes a PWM to hysteretic transition. But instead of looking for eight consecutive positive occurrences on the phase node, it is looking for eight consecutive negative occurrences on the phase node. The operation mode will be changed from hysteretic to PWM when these eight consecutive pulses occur. This transition technique prevents jitter of the operation mode at load levels close to boundary.

The other mechanism for changing from hysteretic to PWM is due to a sudden increase in the output current. This step load causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the decrease causes the output voltage to drop below the hysteretic regulation level, the mode is changed to PWM on the next clock cycle. This insures the full power required by the increase in output current.

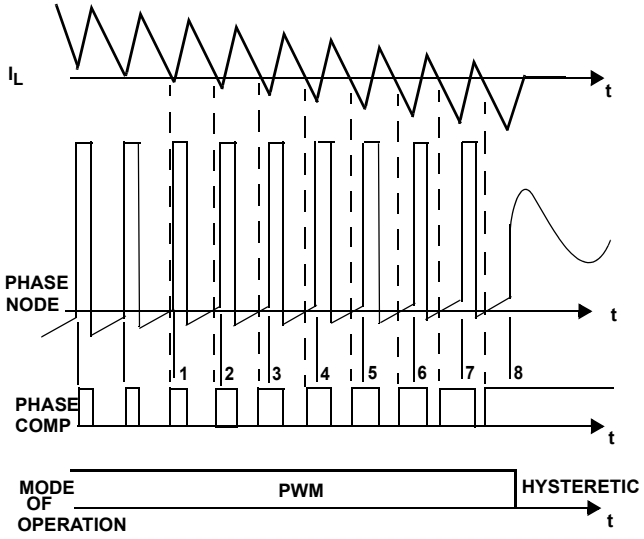


FIGURE 6. MODE CONTROL WAVEFORMS

Gate Control Logic

The gate control logic translates generated PWM control signals into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operational conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1 volt. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1 volt. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

3.3V Main and 5V Main Soft Start, Sequencing and Stand-by

See Table 1 for the output voltage control algorithm. The 5V Main and 3.3V Main converters are enabled if $\overline{SDWN1}$ and $\overline{SDWN2}$ are high and $\overline{SDWNALL}$ is also high. The stand-by mode is defined as a condition when $\overline{SDWN1}$ and $\overline{SDWN2}$ are low and the PWM converters are disabled but $\overline{SDWNALL}$ is high (3.3V ALWAYS and 5V ALWAYS outputs are enabled). In this power saving mode, only the low power micro-controller and keyboard may be powered.

TABLE 1. OUTPUT VOLTAGE CONTROL

$\overline{SDWNALL}$	$\overline{SDWN1}$	$\overline{SDWN2}$	3V AND 5V ALWAYS	5V MAIN	3V MAIN
0	X	X	OFF	OFF	OFF
1	0	0	ON	OFF	OFF
1	1	0	ON	ON	OFF
1	0	1	ON	OFF	ON
1	1	1	ON	ON	ON

Soft start of the 3.3V Main and 5V Main converters is accomplished by means of capacitors connected from pins $\overline{SDWN1}$ and $\overline{SDWN2}$ to ground. In conjunction with 5µA internal current sources, they provide a controlled rise of the 3.3V Main and 5V Main output voltages. The value of the soft-start capacitors can be calculated from the following expression.

$$Css = \frac{5\mu A \times Tss}{3.5V}$$

Where Tss is the desired soft-start time.

By varying the values of the soft-start capacitors, it is possible to provide sequencing of the main outputs at startup.

Figure 7 shows the soft-start initiated by the $\overline{SDWNALL}$ pin being pulled high with the Vbatt input at 10.8V and the resulting 3.3V Main and 5V Main outputs.

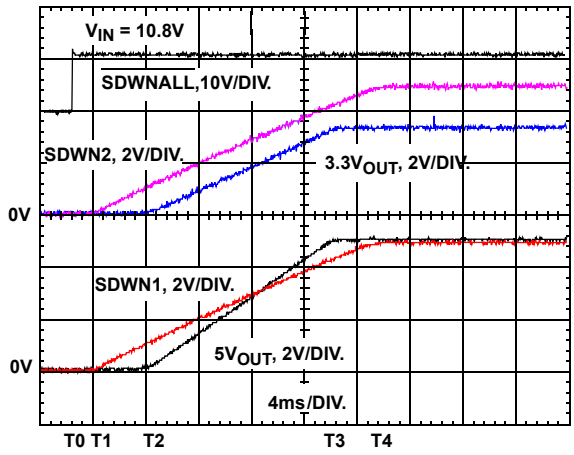


FIGURE 7. SOFT-START ON 3.3V AND 5V OUTPUTS

While the $\overline{SDWNALL}$ pin is held low, prior to T0, all outputs are off. Pulling $\overline{SDWNALL}$ high enables the 3.3V ALWAYS and 5V ALWAYS outputs. With the 3.3V Main and 5V Main outputs enabled, at T1, the internal 5µA current sources start charging the soft start capacitors on the $\overline{SDWN1}$ and $\overline{SDWN2}$ pins. At T2 the outputs begin to rise and because they both have the same value of soft-start capacitors, 0.022µF, they both reach regulation at the same time, T3. The soft-start capacitors continue to charge and are completely charged at T4.

12V Converter Architecture

The 12V boost converter generates its output voltage from the 5V Main output. An external MOSFET, inductor, diode and capacitor are required to complete the circuit. The output signal is fed back to the controller via an external resistive divider. The boost controller can be disabled by connecting the VSEN3 pin to 5V ALWAYS.

The control circuit for the 12V converter consists of a 3:1 frequency divider which drives a ramp generator and resets a PWM latch as shown in Figure 8. The width of the CLK/3 pulses is equal to the period of the main clock, limiting the duty cycle to 33%. The output of a non-inverting error amplifier is compared with the rising ramp voltage. When the ramp voltage becomes higher than the error signal, the PWM comparator sets the latch and the output of the gate driver is pulled high providing leading edge, voltage mode PWM. The falling edge of the CLK/3 pulses resets the latch and pulls the output of the gate driver low.

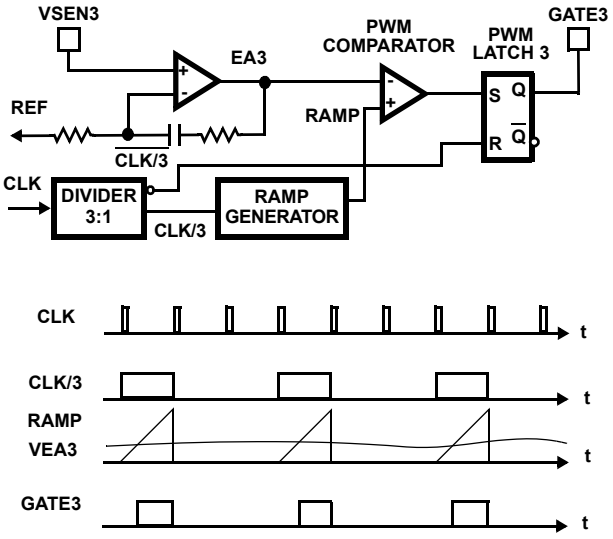


FIGURE 8. 12V BOOST OPERATION

The 33% maximum duty cycle of the converter guarantees discontinuous inductor current and unconditional stability over all operating conditions.

The boost converter with the limited duty cycle and discontinuous inductor current can deliver to the load a limited amount of power before the output voltage starts to drop. When the duty cycle has reached DMAX, the control loop is operating open circuit and the output voltage varies with the output load resistance, Ro, as given by:

$$Vo = Vin \times Dmax\left(\sqrt{\frac{Ro}{2(LxF)}}\right)$$

Where Vin is the 5V Main voltage, Dmax = 0.33, L is the value of the boost inductor, L3, and F = 100kHz. This provides automatic output current limiting. When the maximum duty cycle has been reached and for a given inductor, a further reduction in Ro by one-half will pull the output voltage down to 0.707 of nominal and cause an undervoltage condition.

The 12V converter starts to operate at the same time as the 5V Main converter. The rising voltage on the 5V Main output and the 33% duty cycle limit provides a similar soft-start, as the 5V Main, for the 12V output.

3V ALWAYS, 5V ALWAYS Linear Regulators

The 3.3V ALWAYS and 5V ALWAYS outputs are derived from the battery voltage and are the first voltages available in the notebook when power on is initiated. The 5V ALWAYS output is generated directly from the battery voltage by a linear regulator. It is used to power the system micro-controller and to internally power the chip and the gate drivers. The 3.3V ALWAYS output is generated from the 5V ALWAYS output and may be used to power the keyboard controller or other peripherals. The combined current capability of these outputs is 50mA. When the 5V Main output is greater than it's undervoltage level, it is switched to the 5V ALWAYS output via an internal 1.3Ω MOSFET switch. Simultaneously, the 5V ALWAYS linear regulator is disabled to prevent excessive power dissipation.

The rise time of the 5V ALWAYS is determined by the value of the output capacitance on the 5V and 3.3V ALWAYS outputs. The internal regulator is current limited to about 180mA, so the startup time is approximately:

$$t = C_{OUT} \times \frac{5V}{180mA}$$

Where C_{OUT} is the sum of the capacitances on the 5V and 3.3V ALWAYS outputs.

Power Good Status

The IPM6220A monitors all the output voltages except for the 3.3V ALWAYS. A single power-good signal, PGOOD, is issued when soft-start is completed and all monitored outputs are within 10% of their respective set points. After the soft-start sequence is completed, undervoltage protection latches the chip off when any of the monitored outputs drop below 75% of its set point.

A 'soft-crowbar' function is implemented for an overvoltage on the 3.3V Main or 5V Main outputs. If the output voltage goes above 115% of their nominal output level, the upper MOSFET is turned off and the lower MOSFET is turned on. This 'soft-crowbar' condition will be maintained until the output voltage returns to the regulation window and then normal operation will continue.

This 'soft-crowbar' and monitoring of the output, prevents the output voltage from ringing negative as the inductor current flows in the 'reverse' direction through the lower MOSFET and output capacitors.

Over-Temperature Protection

The IC incorporates an over-temperature protection circuit that shuts all the outputs down when the die temperature exceeds 150°C. Normal operation is automatically restored when the die temperature cools to 125°C.

Component Selection Guidelines

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients.

3.3V Main and 5V Main PWM Output Capacitors

Selection of the output capacitors is also dependent on the output inductor so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. Given a sufficiently fast control loop design, the IPM6220A will provide either 0% or 94% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, this reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is:

$$C_{OUT} = \frac{L_O \times I_{TRAN}}{(V_{IN} - V_{OUT}) \times 2} \times \frac{I_{TRAN}}{DV_{OUT}}$$

Where: C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_{OUT} is output voltage, and ΔV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Equivalent Series Resistance) and voltage rating requirements as well as actual capacitance requirements. The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by:

$$V_{RIPPLE} = \Delta I_L \times ESR$$

where, ΔI_L is calculated in the Inductor Selection section.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications, at 300kHz, for the bulk capacitors. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

The stability requirement on the selection of the output capacitor is that the 'ESR zero', f_Z, be between 1.2kHz and 30kHz. This range is set by an internal, single compensation zero at 6kHz. The ESR zero can be a factor of five on either side of the internal zero and still contribute to increased phase margin of the control loop. Therefore:

$$C_{OUT} = \frac{1}{2 \times \pi \times ESR \times f_Z}$$

In conclusion, the output capacitors must meet three criteria: By varying the values of the soft-start capacitors, it is possible to provide sequencing of the main outputs at start-up.

1. They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient
2. The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current, and
3. The ESR zero should be placed, in a rather large range, to provide additional phase margin.

3.3V ALWAYS and 5V ALWAYS Output Capacitors

The output capacitors for the linear regulators insure stability and provide dynamic load current. The 3.3V ALWAYS and the 5V ALWAYS linear regulators should have, as a minimum, 10μF capacitors on their outputs.

3.3V Main and 5V Main PWM Output Inductor Selection

The PWM converters require output inductors. The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Input Capacitor Selection

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline.

The AC RMS input current varies with load as shown in Figure 9. Depending on the specifics of the input power and its impedance, most (or all) of this current is supplied by the input capacitor(s). Figure 9 also shows the advantage of having the PWM converters operating out of phase. If the converters were operating in-phase, the combined RMS current would be the algebraic sum, which is a much larger value as shown. The combined out-of-phase current is the square root of the sum of the square of the individual reflected currents and is significantly less than the combined in-phase current.

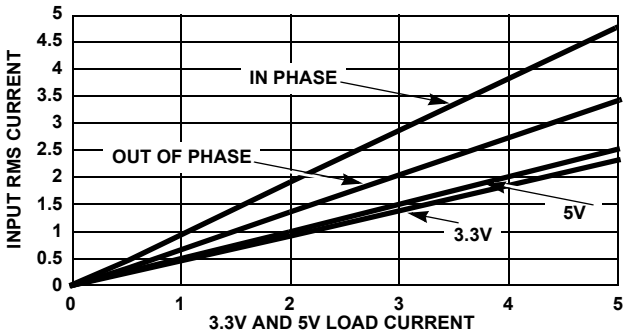


FIGURE 9. INPUT RMS CURRENT vs LOAD

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For board designs that allow through-hole components, the Sanyo OS-CON® series offer low ESR and good temperature performance.

For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX is surge current tested.

+12V Boost Converter Inductor Selection

The inductor value is chosen to provide the required output power to the load.

$$Lmax = \frac{Vinmin^2 \times Dmax^2 \times Ro}{2 \times Vo^2 \times F}$$

where, Vinmin is the minimum input voltage, 4.9V; Dmax = 1/3, the maximum duty cycle; Ro is the minimum load resistance; Vo is the nominal output voltage and F is the switching frequency, 100kHz.

+12V Boost Converter Output Capacitor Selection

The total capacitance on the 12V output should be chosen appropriately, so that the output voltage will be higher than the undervoltage limit (9V) when the 5V Main soft-start time has elapsed. This will avoid triggering of the 12V undervoltage protection.

The maximum value of the boost capacitor, Comax that will charge to 9V in the soft-start time, Tss, is shown below, where L is the value of the boost inductor.

$$Comax = \frac{Tss}{L} \times 0.115\mu F$$

The output capacitor ESR and the boost inductor ripple current determines the output voltage ripple. The ripple voltage is given by:

$$V_{RIPPLE} = \Delta I_L \times ESR$$

and the maximum ripple current, ΔI_L, is given by:

$$\Delta I_L = \frac{5V}{L} \times 3.3\mu$$

where L is the boost inductor calculated above, 5V is the boost input voltage and 3.3µ is the maximum on time for the boost MOSFET.

MOSFET Considerations

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements. Two N-channel MOSFETs are used in each of the synchronous-rectified buck converters for the PWM1 and PWM2 outputs. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see the following equations). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the IPM6220A and do not heat the MOSFETs. However, a large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of one of the upper PWM MOSFETs. Prior to turn-off, the upper MOSFET is carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the

magnitude of voltage spikes. See the Application Note AN9915 for the evaluation board component placement and the printed circuit board layout details.

There are two sets of critical components in a DC-DC converter using an IPM6220A controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents.

Power Components Layout Considerations

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power MOSFETs. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

Insure the current paths from the input capacitors to the MOSFETs, to the output inductors and output capacitors are as short as possible with maximum allowable trace widths.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes, but do not unnecessarily oversize these particular islands. Since the phase nodes are subjected to very high dV/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.

Small Components Signal Layout Considerations

4. The VSNS1 and VSNS2 inputs should be bypassed with a 1.0µF capacitor close to their respective IC pins.
5. A ‘T’ filter consisting of a ‘split’ RSNS and a small, 100pF, capacitor as shown in Figure 10, may be helpful in reducing noise coupling into the ISEN input. For example, if the calculated value of RSNS1 is 2.2kΩ, dividing it as shown with a 100pF capacitor provides filtering without changing the current limit set point. For any calculated value of RSNS, keep the value of the R9 portion to approximately 200Ω, and the remainder of the resistance in the R19 position. The 200Ω resistor and 100pF capacitor provide effective filtering for noise above 8MHz. This filter configuration may be helpful on both the 3.3V and 5V Main outputs.

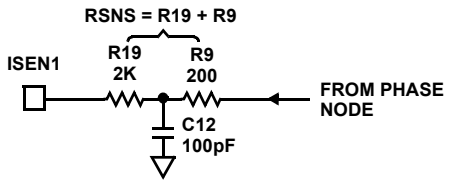


FIGURE 10. NOISE FILTER FOR ISEN1 INPUT

6. The bypass capacitors for VBATT and the soft-start capacitors, C_{SS1} and C_{SS2} should be located close to their connecting pins on the control IC. Minimize any leakage current paths from SDWN1 and SDWN2 nodes, since the internal current source is only 5µA.
7. Refer to the Application Note AN9915 for a recommended component placement and interconnections.

Figure 11 shows an application circuit of a power supply for a notebook PC microprocessor system. The power supply provides +5V ALWAYS, +3.3V ALWAYS, +5.0V, +3.3V, and 12V from +5.6-22V_{DC} battery voltage. For detailed information on the circuit, including a Bill of Materials and circuit board description, see Application Note AN9915. Also see Intersil’s web site (www.intersil.com) for the latest information.

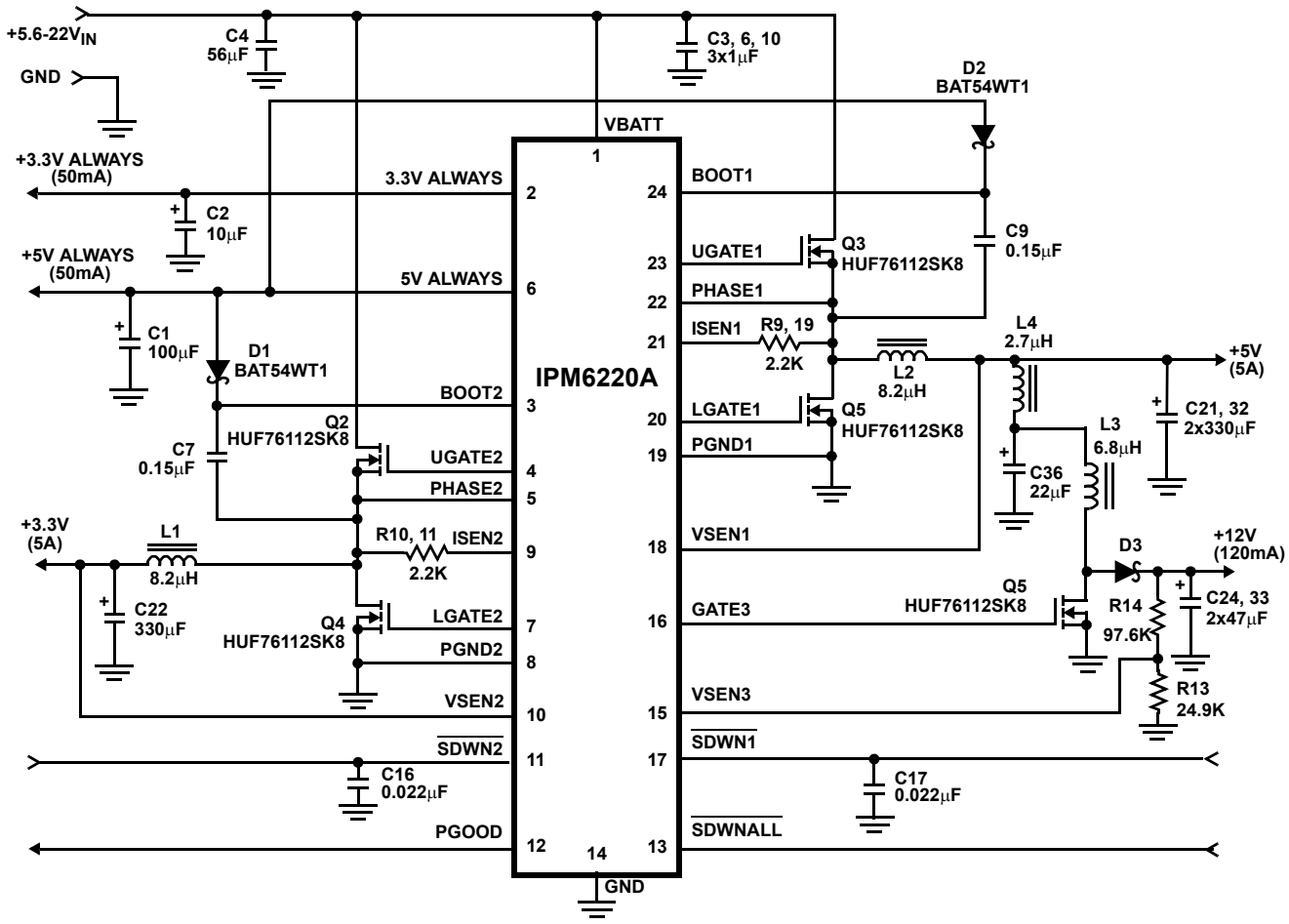
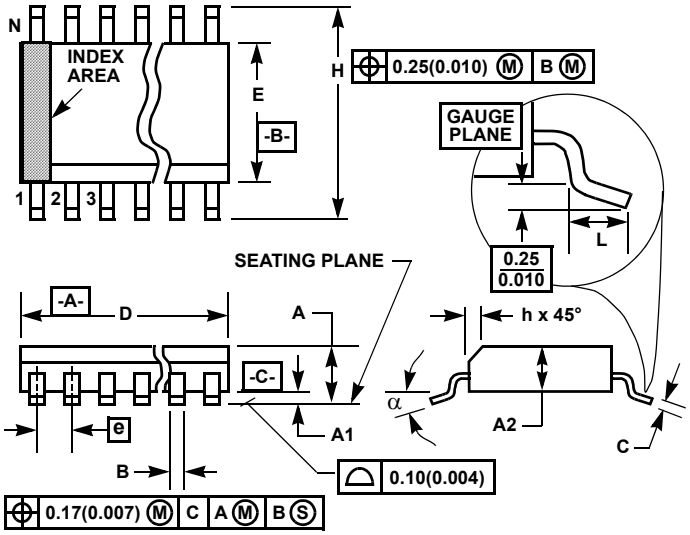


FIGURE 11. APPLICATIONS CIRCUIT

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M24.15

24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.55	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 2 6/04