Ultra Low ON-Resistance, Low Voltage, Single Supply, DPDT Analog Switch

The Intersil ISL43L410 device is a low ON-resistance, low voltage, bidirectional, double-pole/double-throw (DPDT) analog switch designed to operate from a single +1.65V to +3.6V supply. It is equipped with an inhibit pin to simultaneously open all signal paths.

Targeted applications include battery powered equipment that benefit from low R_{ON} (0.25Ω) and fast switching speeds (t_{ON} = 12ns, t_{OFF} = 5ns). The digital logic input is 1.8V logic-compatible when using a single +3V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to “mux-in” additional functionality while reducing ASIC design risk. The ISL43L410 is offered in small form factor packages, alleviating board space limitations.

The ISL43L410 is a committed double-pole/double-throw (DPDT) that consists of two normally open (NO) and two normally closed (NC) switches. This configuration is perfect for use in differential 2-to-1 multiplexer applications.

TABLE 1. FEATURES AT A GLANCE

	ISL43L410
Number of Switches	2
SW	DPDT
3V R_{ON}	0.25Ω
3V t_{ON}/t_{OFF}	12ns/5ns
1.8V R_{ON}	0.4Ω
1.8V t_{ON}/t_{OFF}	20ns/8ns
Packages	10Ld 3x3 thin DFN, 10Ld MSOP

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Features

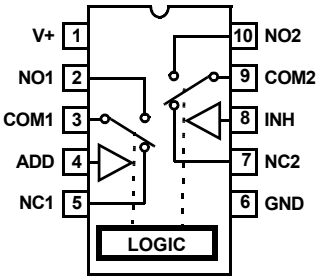
- Pb-Free Available (RoHS Compliant) (see Ordering Info)
- ON Resistance (R_{ON})
  - V+ = +3.0V 0.25Ω
  - V+ = +1.8V 0.4Ω
- R_{ON} Matching Between Channels 0.03Ω
- R_{ON} Flatness Across Signal Range 0.03Ω
- Single Supply Operation. . . . . +1.65V to +3.6V
- Low Power Consumption (P_D). . . . . <0.2µW
- Fast Switching Action (V+ = +2.7V)
  - t_{ON} 12ns
  - t_{OFF} 5ns
- ESD HBM Rating . . . . . >9kV
- Guaranteed Break-before-Make
- 1.8V Logic Compatible (+3V supply)
- Available in 10 Ld 3x3 thin DFN and 10 Ld MSOP Packages

Applications

- Battery powered, Handheld, and Portable Equipment
  - Cellular/mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

Pinout (Note 1)

ISL43L410 (TDFN, MSOP)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

INH	ADD	SWITCH ON
1	X	NONE
0	0	NC_X
0	1	NO_X

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.65V to +3.6V)
GND	Ground Connection
INH	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
ADD	Address Input Pin
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL43L410IR (L40)	-40 to 85	10 Ld 3x3 thin DFN	L10.3x3A
ISL43L410IR-T (L40)	-40 to 85	10 Ld 3x3 thin DFN Tape and Reel	L10.3x3A
ISL43L410IU (L410)	-40 to 85	10 Ld MSOP	M10.118
ISL43L410IU-T (L410)	-40 to 85	10 Ld MSOP Tape and Reel	M10.118
ISL43L410IRZ (L40) (See Note)	-40 to 85	10 Ld 3x3 thin DFN (Pb-free)	L10.3x3A
ISL43L410IRZ-T (L40) (See Note)	-40 to 85	10 Ld 3x3 thin DFN Tape and Reel (Pb-free)	L10.3x3A
ISL43L410IUZ (L410) (See Note)	-40 to 85	10 Ld MSOP (Pb-free)	M10.118
ISL43L410IUZ-T (L410) (See Note)	-40 to 85	10 Ld MSOP Tape and Reel (Pb-free)	M10.118

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
NO, NC, ADD, INH (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current NO, NC, or COM . . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating:
HBM . . . . . >9kV
MM . . . . . >500V
CDM . . . . . >1kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
10 Ld 3x3 DFN Package	110
10 Ld MSOP Package	190

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Operating Conditions

Temperature Range
ISL43L410IX . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NC, NO, ADD, INH, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, See Figure 5	25	-	0.29	0.4	Ω
		Full	-	-	0.4	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC}= Voltage at max R_{ON}, Note 9	25	-	0.03	0.06	Ω
		Full	-	-	0.06	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, Note 7	25	-	0.03	0.1	Ω
		Full	-	-	0.1	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-2	-	2	nA
		Full	-40	-	40	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V	25	-3	-	3	nA
		Full	-60	-	60	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 1, Note 8	25	-	14	20	ns
		Full	-	-	25	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 1, Note 8	25	-	6	12	ns
		Full	-	-	17	ns
Break-Before-Make Time Delay, t_D	V+ = 3.3V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 3, Note 8	Full	2	7	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	95	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, See Figure 4	25	-	68	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, See Figure 6	25	-	-95	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.003	-	%
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	115	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	224	-	pF

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4, 6), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.65		3.6	V
Positive Supply Current, I+	V+ = +1.65 to 3.6V, V_{IN} = 0V or V+	25	-	-	40	nA
		Full	-	-	750	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.3V, V_{IN} = 0V or V+ (Note 8)	Full	-0.5	-	0.5	µA

NOTES:

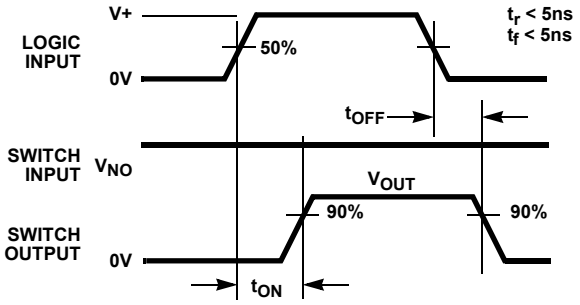
4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parts are 100% tested at +25°C**.** Limits across the full temperature range are guaranteed by design and correlation.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Guaranteed but not tested.
9. R_{ON} matching between channels is calculated by subtracting the channel with the highest max Ron value from the channel with lowest max Ron value.

Electrical Specifications - 1.8V Supply

Test Conditions: V+ = +1.65V to +2V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.4V (Note 4, 6), Unless Otherwise Specified

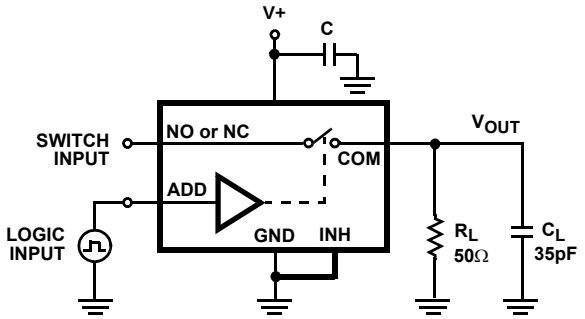
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, See Figure 5, Note 8	25	-	0.4	0.6	Ω
		Full	-	-	0.6	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 2.0V, V_{COM} = 0.3V, 1.8V, V_{NO} or V_{NC} = 1.8V, 0.3V	25	-2	-	2	nA
		Full	-40	-	40	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 2.0V, V_{COM} = 0.3V, 1.8V, or V_{NO} or V_{NC} = 0.3V, 1.8V	25	-3	-	3	nA
		Full	-60	-	60	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.65V, V_{NO} or V_{NC} = 1.0V, R_L =50Ω, C_L = 35pF, See Figure 1, Note 8	25	-	22	28	ns
		Full	-	-	33	ns
Turn-OFF Time, t_{OFF}	V+ = 1.65V, V_{NO} or V_{NC} = 1.0V, R_L =50Ω, C_L = 35pF, See Figure 1, Note 8	25	-	9	15	ns
		Full	-	-	20	ns
Break-Before-Make Time Delay, t_D	V+ = 2.0V, V_{NO} or V_{NC} = 1.0V, R_L =50Ω, C_L = 35pF, See Figure 3, Note 8	Full	2	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	49	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, See Figure 4	25	-	68	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, See Figure 6	25	-	-95	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	115	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	224	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.4	V
Input Voltage High, V_{INH}		Full	1.0	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+ (Note 8)	Full	-0.5	-	0.5	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

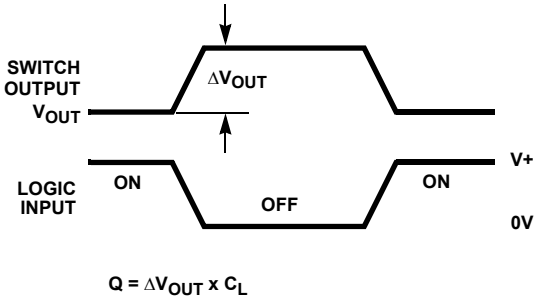
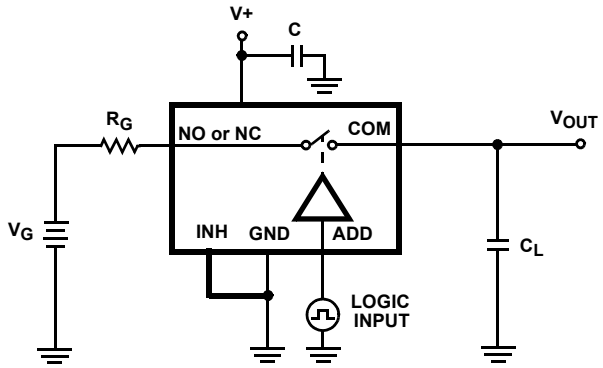


FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

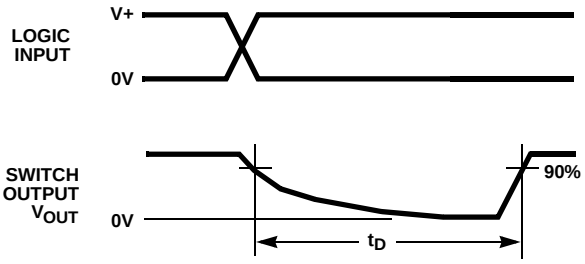
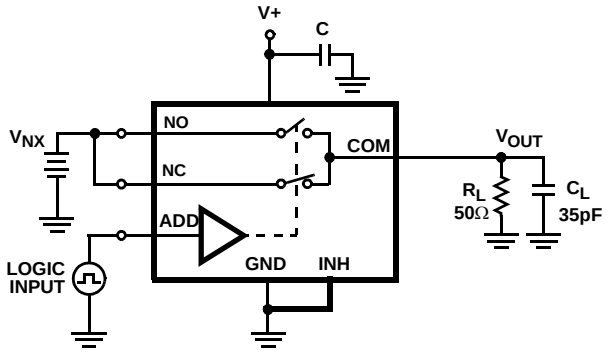


FIGURE 3A. MEASUREMENT POINTS

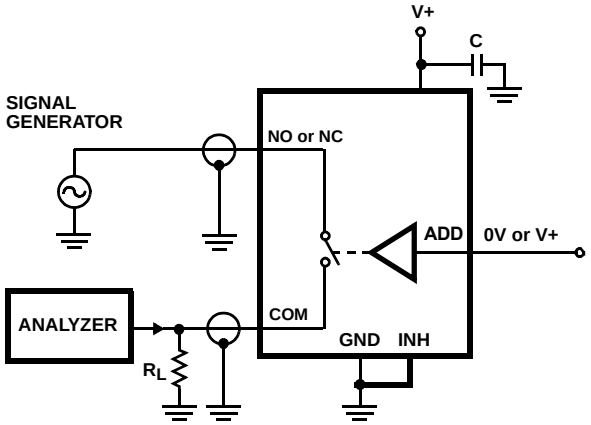


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

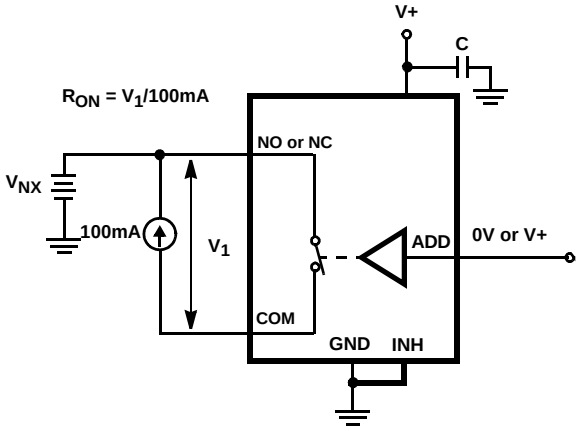
FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)



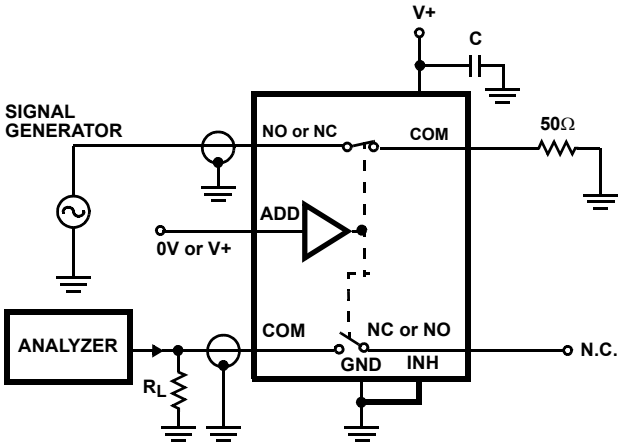
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 4. OFF ISOLATION TEST CIRCUIT



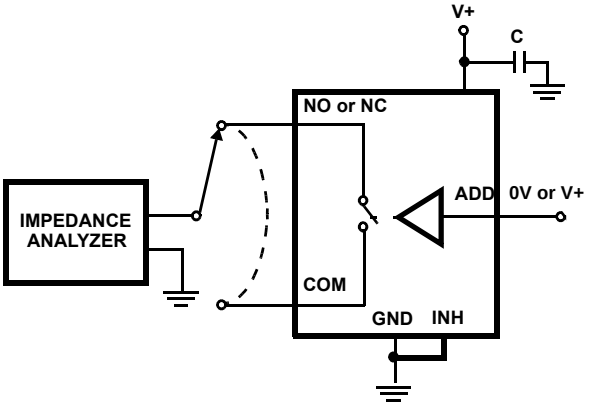
Repeat test for all switches.

FIGURE 5. R_{ON} TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43L410 is a bidirectional, double pole/double throw (DPDT) analog switch that offers precise switching capability from a single 1.65V to 3.6V supply with low on-resistance (0.25Ω) and high speed operation (t_{ON} = 12ns, t_{OFF} = 5ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.65V), low power consumption (2.7μW max), low leakage currents (60nA max), and the tiny DFN and MSOP packages. The ultra low on-resistance and Ron flatness provide very low insertion loss and distortion to applications that require signal reproduction.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces

permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch signal range is reduced and the resistance may increase, especially at low supply voltages.

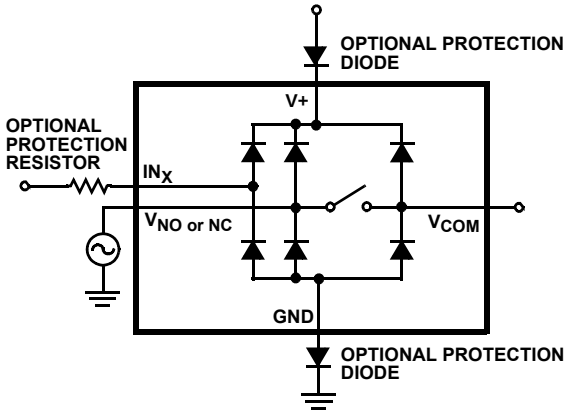


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43L410 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL43L410 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 3.6V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.65V but the part will operate with a supply below 1.5V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.0V to 3.6V (See Figure 15). At 3.6V the V_{IH} level is about 1.27V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, the signal response is reasonably flat even past 30MHz with a -3dB bandwidth of 120MHz (See Figure 16). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 17 details the high Off Isolation and Crosstalk rejection provided by this part. At 100kHz, Off Isolation is about 68dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

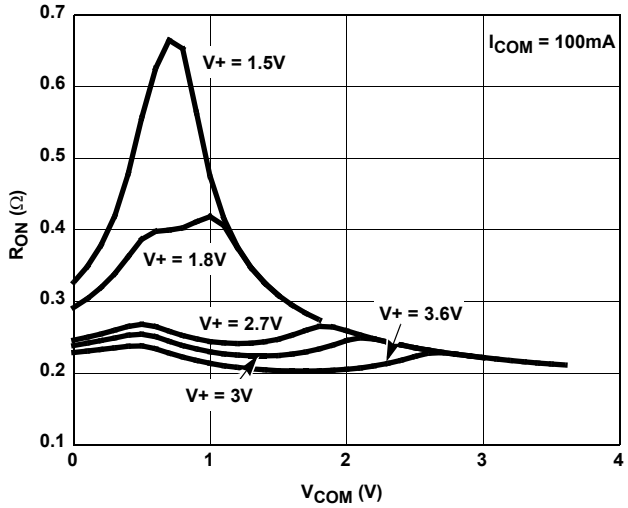


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

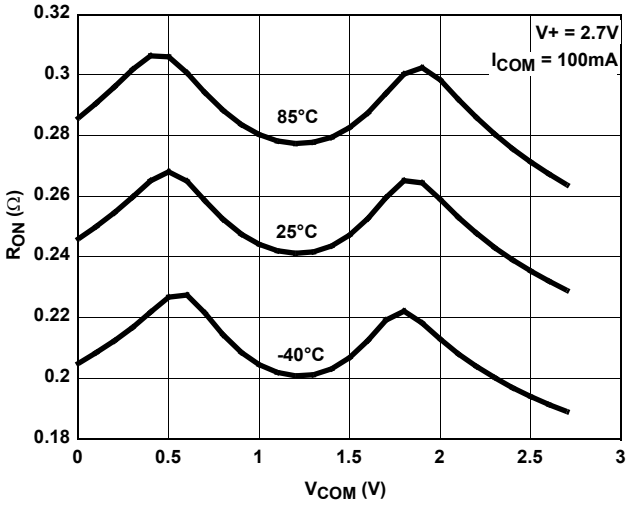


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

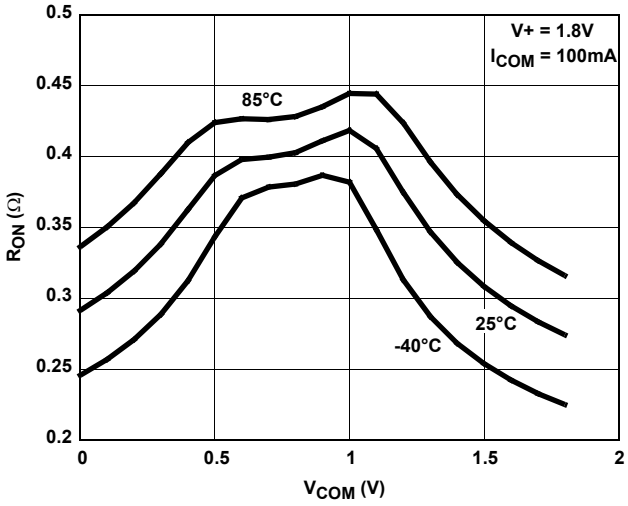


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

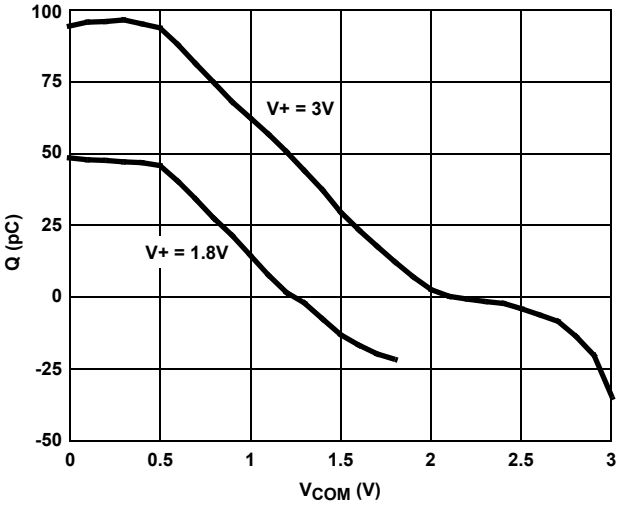


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

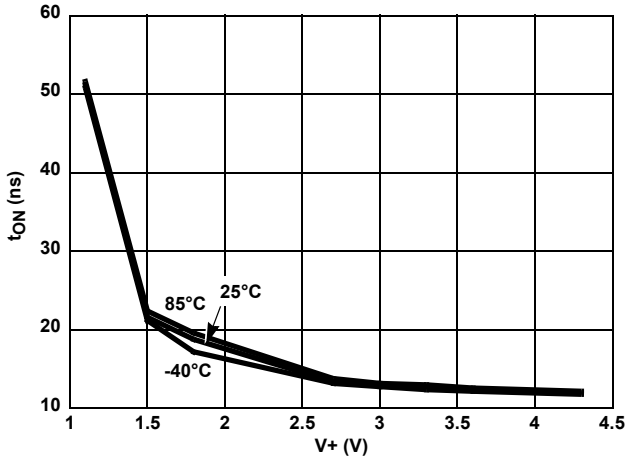


FIGURE 13. TURN - ON TIME vs SUPPLY VOLTAGE

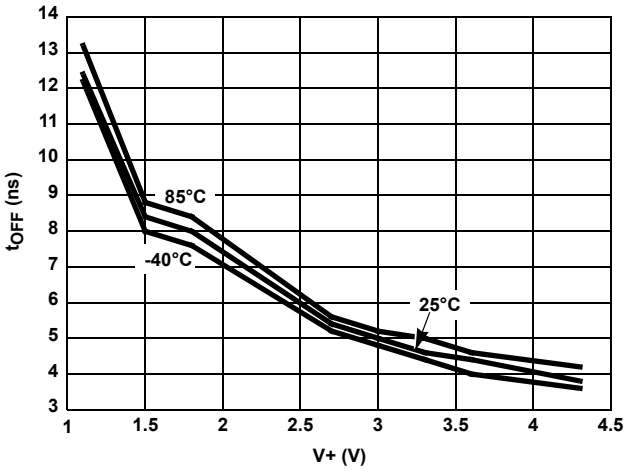


FIGURE 14. TURN - OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

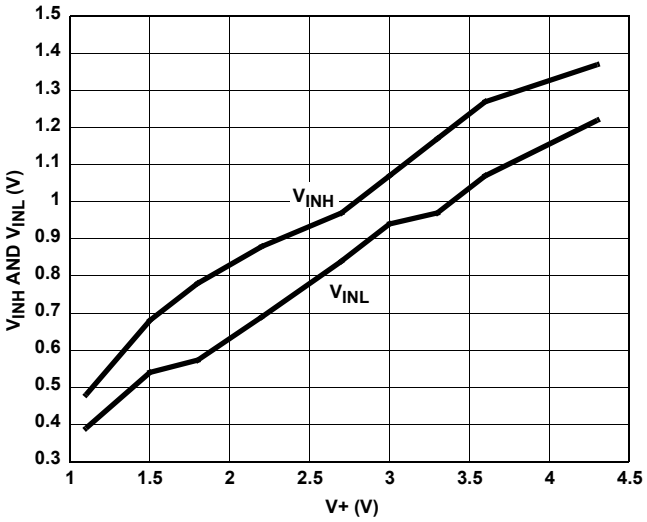


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

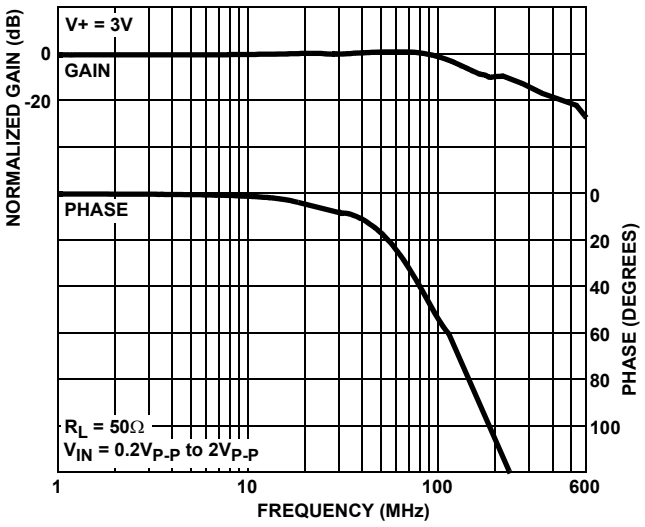


FIGURE 16. FREQUENCY RESPONSE

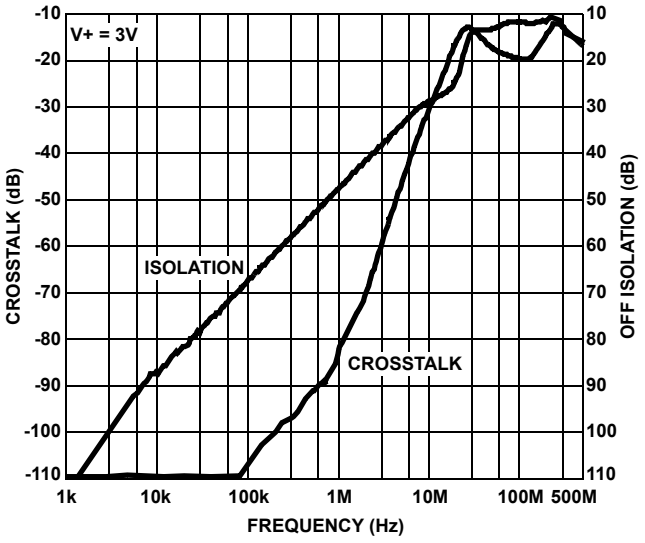


FIGURE 17. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

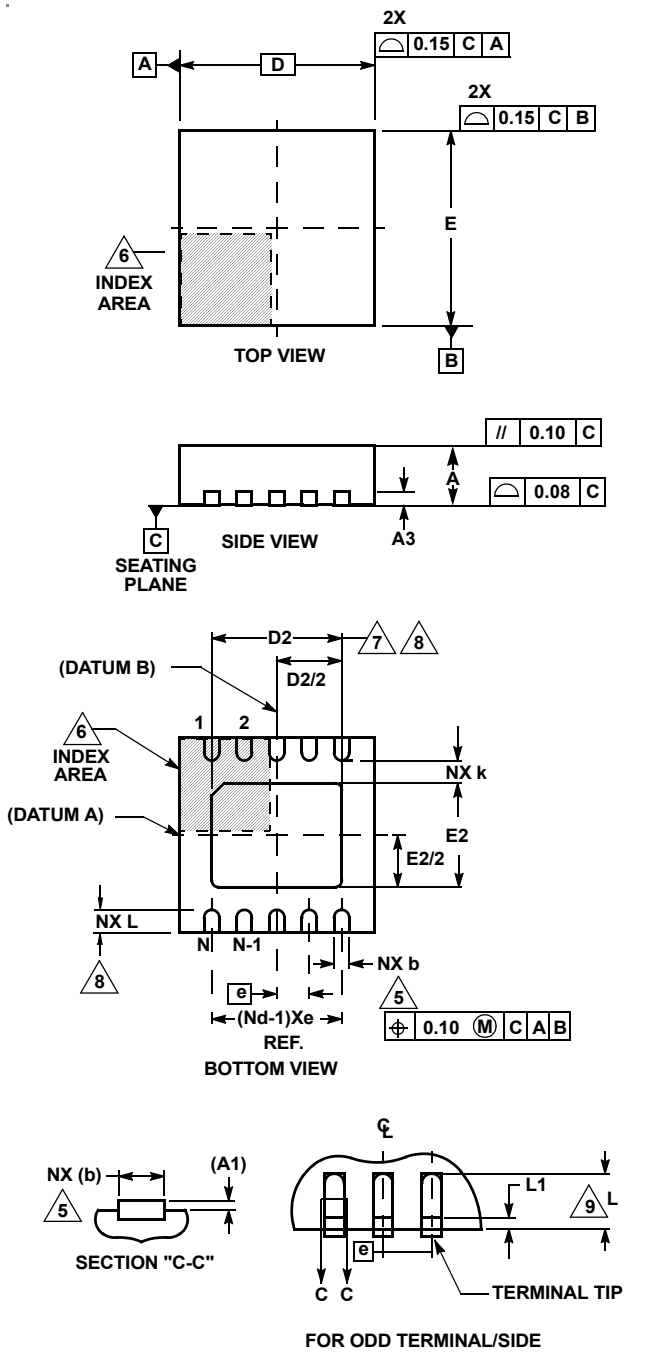
TRANSISTOR COUNT:

114

PROCESS:

Submicron CMOS

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5,8
D		3.00 BSC		-
D2	2.20	2.30	2.40	7,8
E		3.00 BSC		-
E2	1.40	1.50	1.60	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
L1	-	-	0.15	1
N		10		2
Nd		5		3

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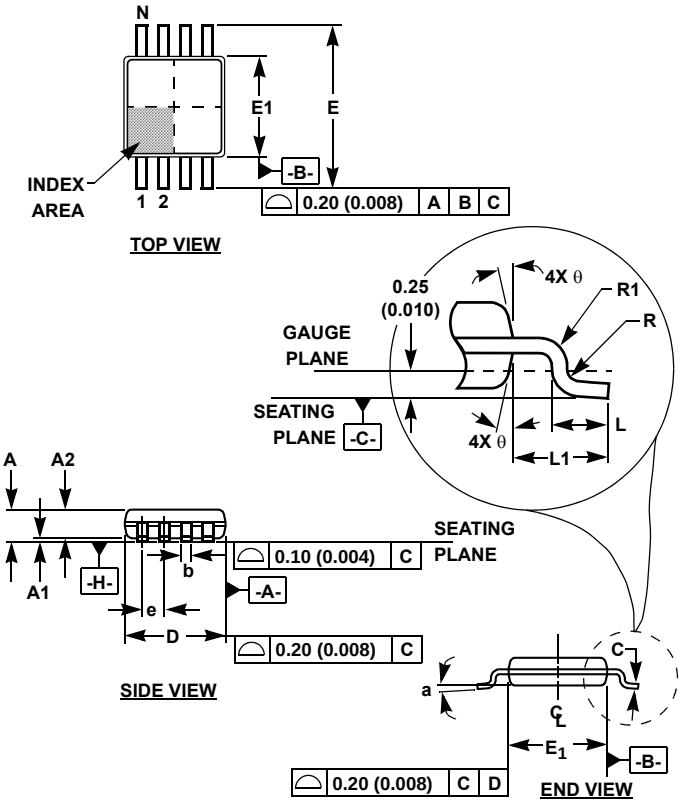
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.
10. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only