LCD Module Calibrator

The VCOM voltage of an LCD panel needs to be adjusted to remove flicker. This part provides a digital interface to control the sink-current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external VCOM buffer amplifier. Once the desired VCOM setting is obtained, the settings can be stored in the non-volatile memory, which would then be automatically recalled during every power-up.

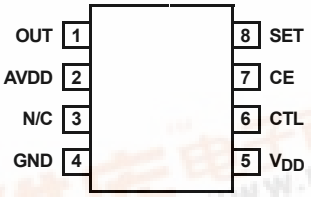
The VCOM adjustment and non-volatile memory programming is through a single interface pin. An additional pin is used to prevent programming.

An external resistor attaches to the SET pin, and sets the full-scale sink current that determines the lowest voltage of the external voltage divider.

The ISL45042 is available in an 8-pin 3mm x 3mm Thin DFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

Pinout

ISL45042 (THIN DFN)
TOP VIEW



Features

- 128-Step Adjustable Sink Current Output
- 2.6V to 3.6V Logic Supply Voltage Operating Range
- 4.5V to 20V Analog Supply Voltage Range
- Rewritable EEPROM for storing the optimum VCOM value
- Output Adjustment Enable/Disable Control
- Output Guaranteed Monotonic Over Temperature
- Two Pin Adjustment, Programming and Enable
- Ultra Thin 8-Pin 3mm x 3mm DFN (0.8mm max)
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- LCD Panels

Ordering Information

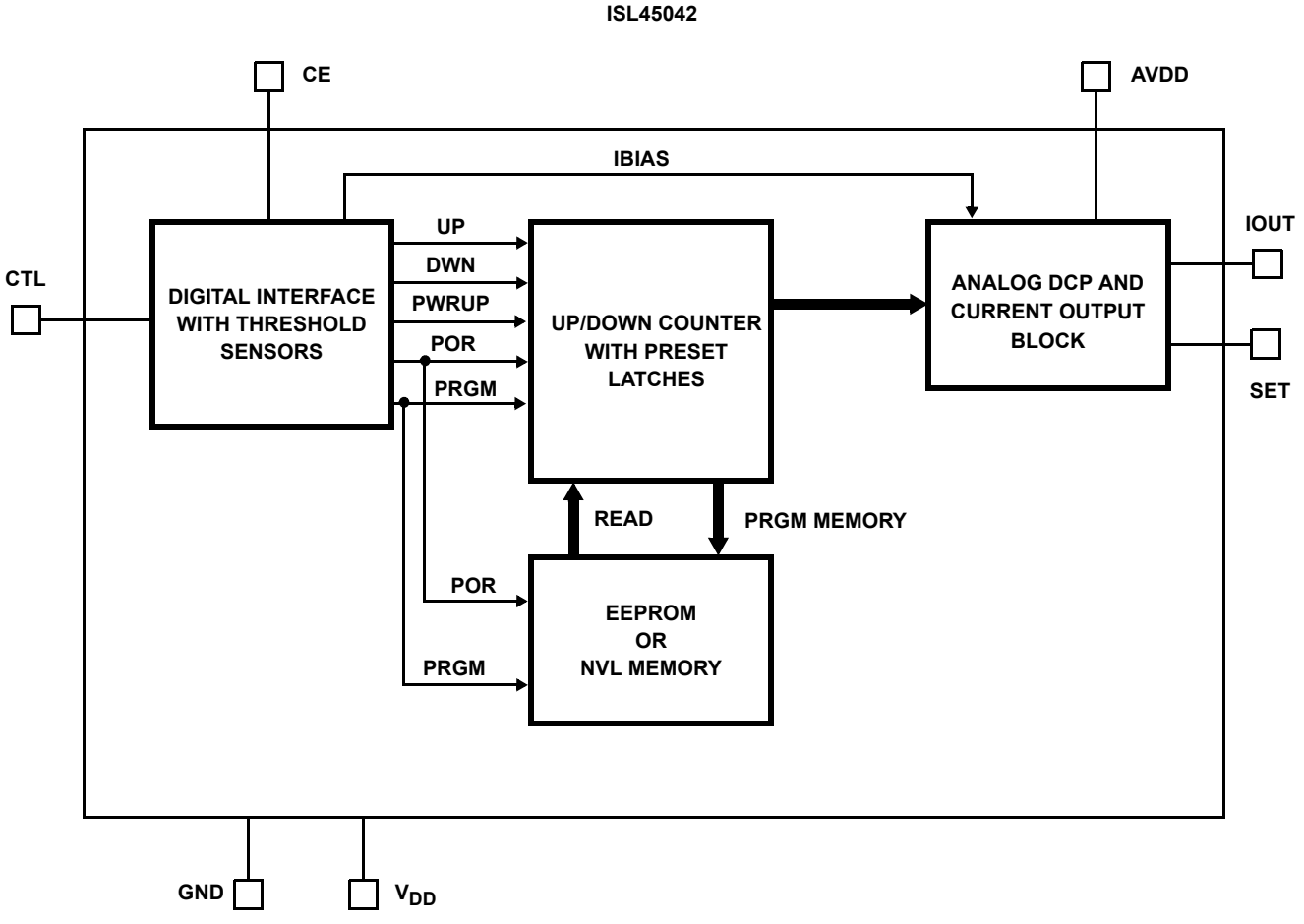
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL45042IR	-40 to 85	8 Ld 3x3 Thin DFN	L8.3x3A
ISL45042IR-T	-40 to 85	8 Ld 3x3 Thin DFN Tape and Reel	L8.3x3A
ISL45042IRZ (Note)	-40 to 85	8 Ld 3x3 Thin DFN (Pb-free)	L8.3x3A
ISL45042IRZ-T (Note)	-40 to 85	8 Ld 3x3 Thin DFN Tape and Reel (Pb-free)	L8.3x3A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN	FUNCTION
OUT	Adjustable Sink Current Output Pin. The current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maxim adjustable sink current setting.
AVDD	High-Voltage Analog Supply. Bypass to GND with 0.1µF capacitor.
N/C	No Connect. Not internally connected.
GND	Ground connection.
V_{DD}	System power supply input. Bypass to GND with 0.1µF capacitor.
CTL	Internal Counter Up/Down Control and Internal EEPROM Programming Control Input. If CE is high, a mid-to-low transition increments the 7-bit counter, raising the DAC setting, increasing the OUT sink current, and lowering the divider voltage at OUT. A mid-to-high transition decrements the 7-bit counter, lowering the DAC setting, decreasing the OUT sink current, and increasing the divider voltage at OUT. Applying 4.9V and above with appropriately arranged timing will overwrite EEPROM with the contents in the 7-bit counter. See EEPROM Programming section for details.
CE	Counter Enable Pin. Connect CE to V_{DD} to enable counting of the internal counter. Connect CE to GND to inhibit counting.
SET	Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AVDD/20) divided by RSET.

Block Diagram



Absolute Maximum Ratings

V_{DD} to Ground . . . . . +4V
Input Voltages to GND
SET, CE . . . . . -0.3V to +4V
AVDD . . . . . -0.3V to +20V
CTL. . . . . -0.3V to +17V
Output Voltages to GND
OUT . . . . . -0.3V to +20V
ESD Rating
HBM for Device 2.75kV
HBM for CTL to GND (no EEPROM Content Disruption). 8kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}
8 Ld Thin DFN Package	90(°C/W)

Moisture Sensitivity (see Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)
Erase/Write Cycles 10,000
Data Retention. . . . . 10 years @ 85°C

Operating Conditions

Temperature Range
ISL45042IR . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications

Test Conditions: VDD = 3V, AVDD = 10V, OUT = 5V, R_{SET} = 24.9kΩ; Unless Otherwise Specified. Typicals are at T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
V_{DD} Supply Range	V_{DD}	For Programming	0 to 85	3	-	3.6	V
		For Operation	Full	2.6	-	3.6	V
V_{DD} Supply Current	I_{DD}	CE = V_{DD}	Full	-	-	50	µA
		CE = GND	Full	-	-	20	µA
		Program (Charge Pump Current) (Note 5)	0 to 85	-	-	23	mA
		Read (Note 5)	Full	-	-	3	mA
AVDD Supply Range	AVDD		Full	4.5	-	20	V
AVDD Supply Current	IAVDD	(Note 3)	Full	-	-	20	µA
CTL High Voltage	CTL_{IH}	2.6V < V_{DD} < 3.6V	Full	0.7*V_{DD}	-	0.8*V_{DD}	V
CTL Low Voltage	CTL_{IL}	2.6V < V_{DD} < 3.6V	Full	0.2*V_{DD}	-	0.3*V_{DD}	V
CTL High Rejected Pulse Width	CTL_{IHRPW}		Full	20	-	-	µs
CTL Low Rejected Pulse Width	CTL_{ILRPW}		Full	20	-	-	µs
CTL High Minimum Pulse Width	CTL_{IHMPW}		Full	-	-	200	µs
CTL Low Minimum Pulse Width	CTL_{ILMPW}		Full	-	-	200	µs
CTL Minimum Time Between Counts	CTL_{MTC}		Full	-	-	10	µs
CTL Input Current	ICTL	CTL = GND	Full	-	-	10	µA
		CTL = V_{DD}	Full	-	-	10	µA
CTL Input Capacitance	CTL_{CAP}	(Note 5)	Full	-	10	-	pF
CE Input Low Voltage	CE_{IL}	2.6V < V_{DD} < 3.6V	Full	-	-	0.4	V
CE Input High Voltage	CE_{IH}	2.6V < V_{DD} < 3.6V	Full	1.6	-	-	V
CE Minimum Start Up Time	CE_{ST}	(Note 5)	Full	1	-	-	ms
CTL EEPROM Program Voltage	CTL_{PROM}	2.6V < V_{DD} < 3.6V, (Note 2)	Full	4.9	-	15.75	V

Electrical Specifications Test Conditions: VDD = 3V, AVDD = 10V, OUT = 5V, R_{SET} = 24.9kΩ; Unless Otherwise Specified. Typicals are at T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
CTL EEPROM Programming Signal Time	CTL_{PT}	>4.9V	Full	200	-	-	µs
Programming Time	P_T		Full			100	ms
EE Write Cycles	EE_{WC}	Guaranteed by Design	25	1000	-	-	Cycles
SET Voltage Resolution	SET_{VR}	(Note 4)	Full	7	-	-	Bits
SET Differential Nonlinearity	SET_{DN}	Monotonic Over Temperature	Full	-	-	±1	LSB
SET Zero-Scale Error	SET_{ZSE}		Full	-	-	±2	LSB
SET Full-Scale Error	SET_{FSE}		Full	-	-	±8	LSB
SET Current	ISET	Through R_{SET} (Note 5)	Full	-	-	120	µA
SET External Resistance	SET_{ER}	To GND, AVDD = 20V (Note 5)	Full	10	-	200	kΩ
		To GND, AVDD = 4.5V (Note 5)	Full	2.25	-	45	kΩ
AVDD to SET Voltage Attenuation	AVDD to SET		Full	-	1:20	-	V/V
OUT Settling Time	OUT_{ST}	to ±0.5 LSB Error Band (Note 5)	Full	-	20	-	µs
OUT Voltage Range	V_{OUT}	(Note 5)	Full	VSET + 0.5V	-	13	V
OUT Voltage Drift	OUT_{VD}	(Note 5)	25 to 55	-	-	10	mV

NOTES:

2. CTL signal only needs to be greater than 4.9V to program EEPROM.
3. Tested at AVDD = 20V.
4. The Counter value is set to mid-scale ±4 LSB's in the Production.
5. Simulated and Determined via Design and NOT Directly Tested.

Application Information

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the VCOM voltage during production test and alignment. A 128-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current.

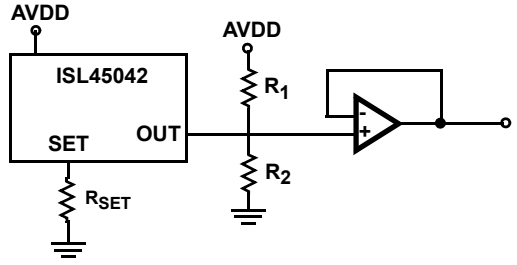


FIGURE 1. OUTPUT CONNECTION CIRCUIT EXAMPLE

The adjustment of the output and the programming of the non-volatile memory are provided on one pin, while the counter enable (CE) is provided on a separate pin. The output is adjusted via the CTL pin either by counting up with a mid to low transition, or by counting down with a mid to high transition. Once the minimum or maximum value is reached on the 128-steps, the device will not overflow or underflow beyond that minimum or maximum value. An increment of the counter will increase the output sink current, which will lower the voltage on the external voltage divider. A decrement of the counter will decrease the output sink current, which will raise the voltage on the external voltage divider.

Once the desired output level is obtained, the part can store its setting using the non-volatile memory in the device. (See the Non-volatile programming section for detailed information.)

The output adjustment can also be prevented from changing by pulling down the counter enable pin.

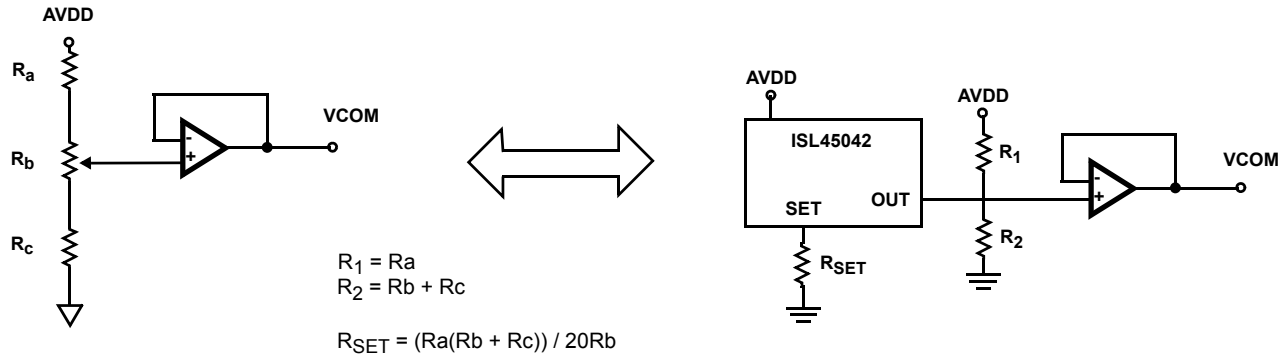


FIGURE 2. EXAMPLE OF THE REPLACEMENT FOR THE MECHANICAL POTENTIOMETER CIRCUIT USING THE ISL45042

Adjustable Sink Current Output

The device provides an output sink current which lowers the voltage on the external voltage divider. The equations that control the output are given below. See Figure 1.

$$IOUT = \frac{Setting}{128} X \frac{AVDD}{20(RSET)}$$

$$VOUT = \left(\frac{R2}{R1 + R2}\right) VAVDD\left(1 - \frac{Setting}{128} X \frac{R1}{20(RSET)}\right)$$

NOTE: Where setting is an integer between 1 and 128.

Replacing Existing Mechanical Potentiometer Circuits

Figure 2 shows the common adjustment mechanical circuits and equivalent replacement with the ISL45042.

7-Bit UP/DOWN Counter

The counter sets the level to the digital potentiometer and is connected to the non-volatile memory. When the part is programmed, the counter setting is loaded into the non-volatile memory. This value will be loaded from the non-volatile memory into the counter during power-on. The counter will not exceed its maximum level and will hold that value during subsequent increment requests on the CTL pin. The counter will not exceed its minimum level and will hold that value during subsequent decrement requests on the CTL pin.

CTL Pin

CTL should have a noise filter to reduce bouncing or noise on the input that could cause unwanted counting when the CE pin is high. The board should have an additional ESD protection circuit, with a series 1kΩ resistor and a shunt 0.01µF capacitor connected on the CTL pin. (See Figure 3)

In order to increment the setting, pulse CTL low for more than 200µs. The output sink current increases and lowers the VCOM lever by one least-significant bit (LSB). On the other hand, to decrement the setting, pulse CTL high for more than 200µs. The output sink current will decrease, and the VCOM level will increase by one LSB.

To avoid unintentional adjustment, the ISL45042 guarantees to reject CTL pulses shorter than 20µs.

To avoid the possibility of a false pulse (since the internal comparators come up in an unknown state) the very first CTL pulse is ignored. See Figure 4 for the timing information.

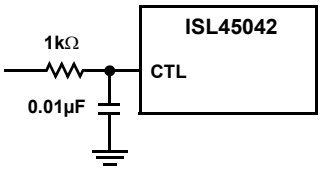


FIGURE 3. EXTERNAL ESD PROTECTION ON CTL PIN

TABLE 1. TRUTH TABLE

INPUT			OUTPUT		
CTL	CE	VDD	SET	ICC	MEMORY
Mid to Hi	Hi	VDD	Decrement	Normal	X
Mid to Lo	Hi	VDD	Increment	Normal	X
X	Lo	VDD	No Change	Lower	X
>4.9V	X	VDD	No Change	Increased	Program
X	X	0 to VDD	Read	Increased	Read

NOTE: ‘CE’ should be disabled (pulled low) before powering the device down to assure that the glitches and transients will not cause unwanted EEPROM overwriting.

NOTE: In case where CE is tied to VDD, CTL pin should be tied to ground (pulled low) when the programming is finished (should not move the counter as the first pulse after programming is ignored), and before the power-down. This will assure that no glitches or transients on CTL input would cause unwanted counter movements.

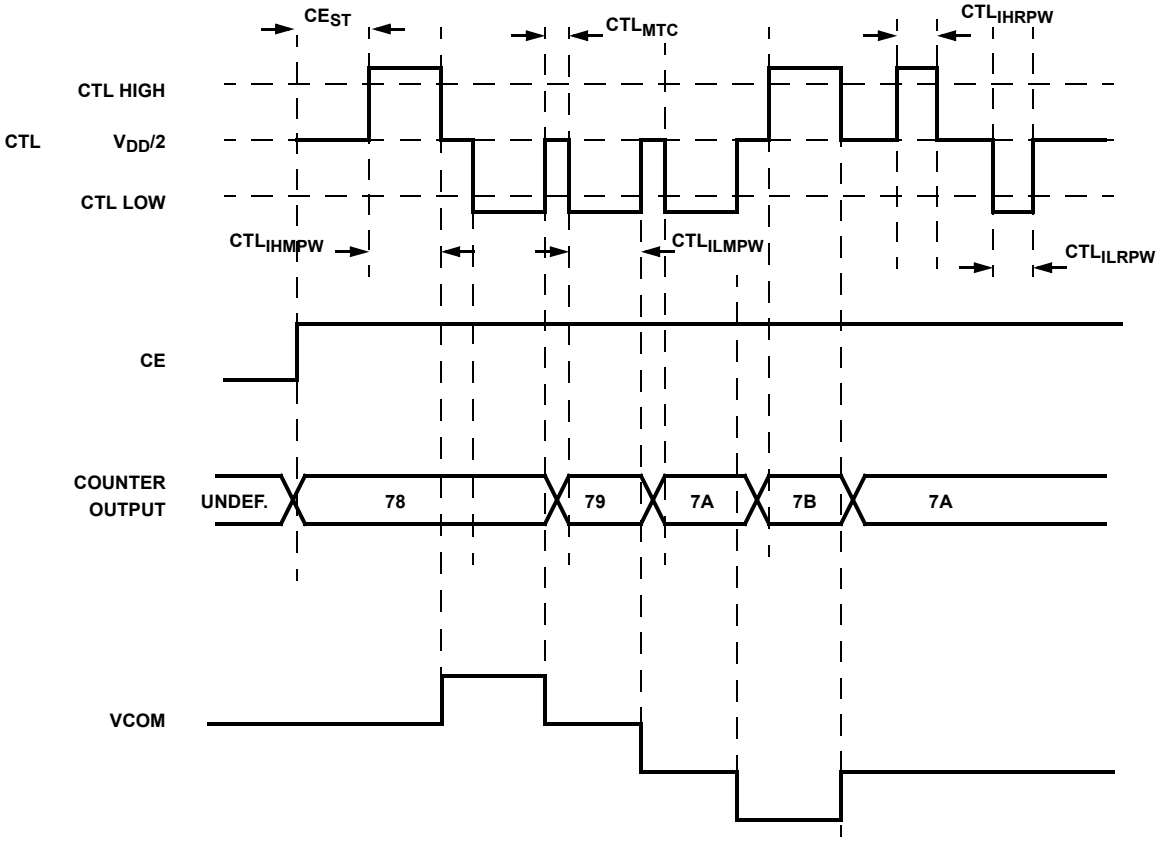


FIGURE 4. VCOM ADJUSTMENT

Non-Volatile Memory (EEPROM) Programming

When the CTL pin exceeds 4.9V, the non-volatile programming cycle will be activated. The CTL signal needs to remain above 4.9V for more than 200µs. The level and timing needed to program the non-volatile memory is given below. It then takes a maximum of 100ms for the programming to be completed inside the device (see P_T specification in Electrical Specification Table).

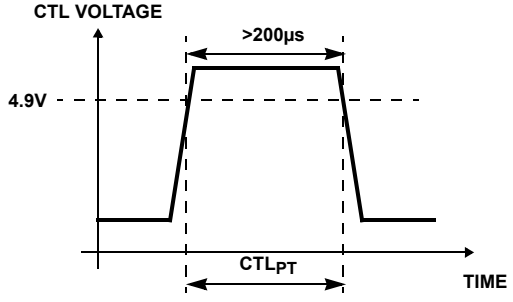
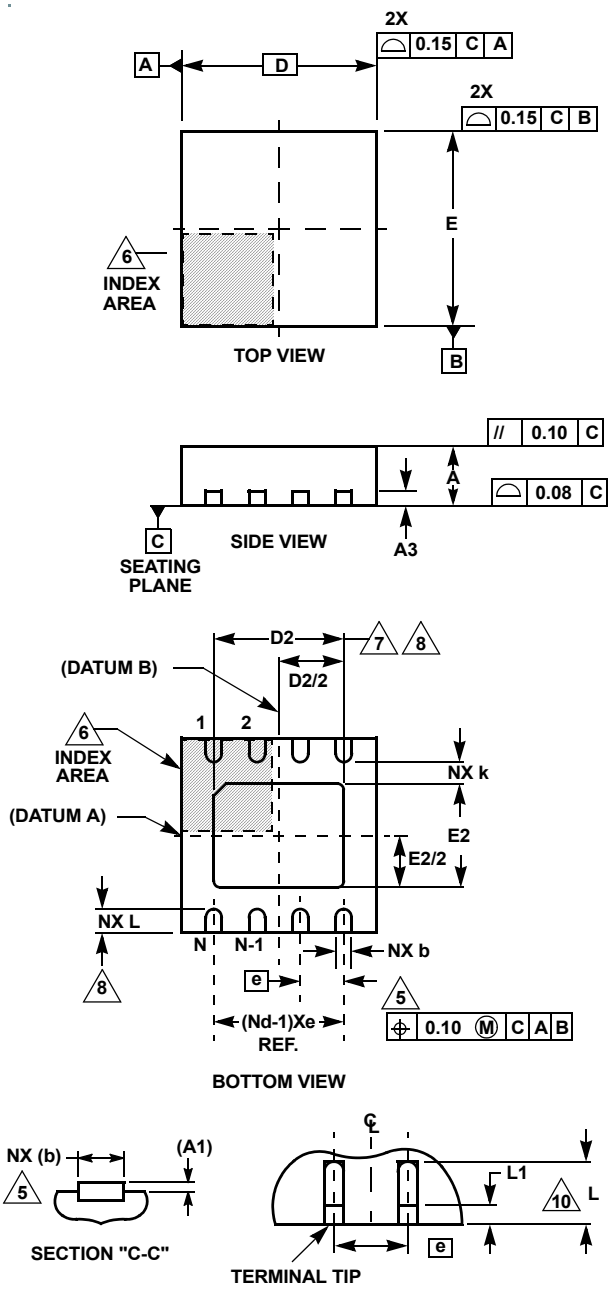


FIGURE 5. EEPROM PROGRAMMING

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3		0.20 REF		-
b	0.25	0.30	0.35	5, 8
D		3.00 BSC		-
D2	2.20	2.30	2.40	7, 8, 9
E		3.00 BSC		-
E2	1.40	1.50	1.60	7, 8, 9
e		0.65 BSC		-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N		8		2
Nd		4		3

Rev. 3 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the “L” min dimension.