International
IOR Rectifier

Data Sheet No. PD-6.042D

IR2128

CURRENT SENSING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- $\overline{\text{FAULT}}$ lead indicates shutdown has occured
- Output out of phase with input

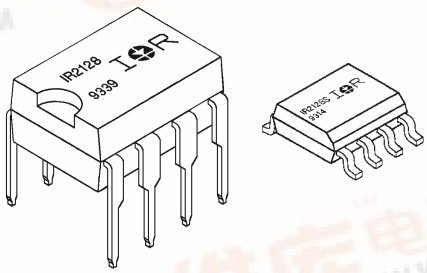
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
V_{CSth}	250 mV
$t_{on/off}$ (typ.)	150 & 100 ns

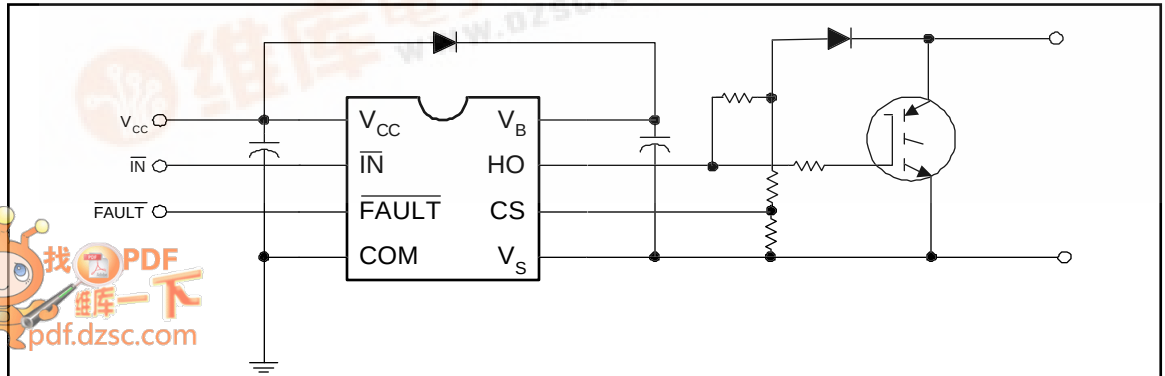
Description

The IR2128 is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 600 volts.

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage	-0.3	25	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_B + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Logic Supply Voltage	11.8	20	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_S + 5	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

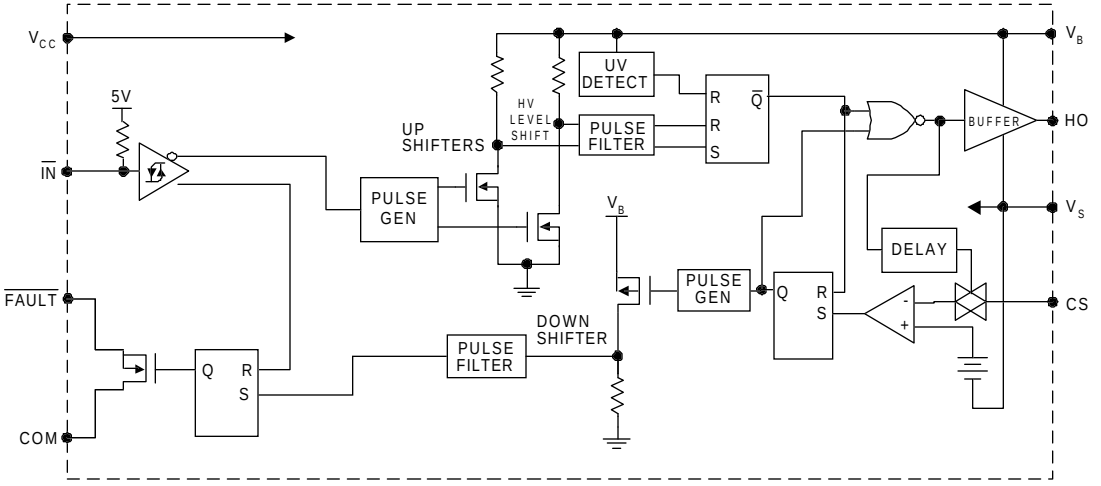
Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	150	200	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	100	150		V_S = 600V
t_r	Turn-On Rise Time	—	80	120		C_L = 1000 pF
t_f	Turn-Off Fall Time	—	40	60		C_L = 1000 pF
t_{bl}	Start-Up Blanking Time	500	750	900		
t_{cs}	CS Shutdown Propagation Delay	—	240	360		
t_{flt}	CS to $\overline{FAULT}$ Pull-Up Propagation Delay	—	340	510		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		V_{CC} = 10V to 20V
V_{CSTH+}	CS Input Positive Going Threshold	180	250	320	mV	V_{CC} = 10V to 20V
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	150	300		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	60	120		V_{IN} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current	—	7.0	15		V_{IN} = 0V
I_{IN-}	Logic "0" Input Bias Current	—	—	1.0		V_{IN} = 5V
I_{CS+}	"High" CS Bias Current	—	—	1.0		V_{CS} = 3V
I_{CS-}	"High" CS Bias Current	—	—	1.0		V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.8	10.3	11.8	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.5	9.0	10.6		
I_{O+}	Output High Short Circuit Pulsed Current	200	250	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	420	500	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

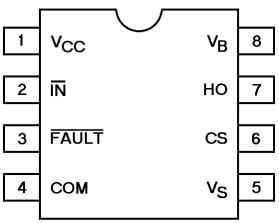
Functional Block Diagram



Lead Definitions

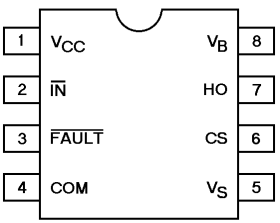
Lead Symbol	Description
V_{CC}	Logic and gate drive supply
$\overline{IN}$	Logic input for gate driver output (HO), out of phase with HO
$\overline{FAULT}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



8 Lead DIP

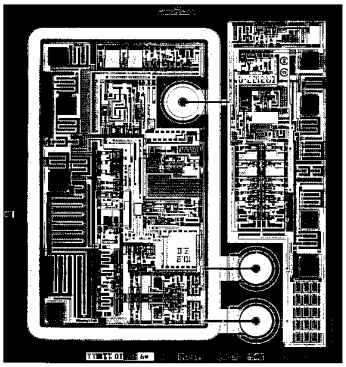
IR2128



SO-8

IR2128S

Device Information

Process & Design Rule		HVDCMOS 4.0 µm
Transistor Count		206
Die Size		77 X 85 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800Å
Connections	Material	Poly Silicon
First Layer	Width	4 µm
	Spacing	6 µm
	Thickness	5000Å
Second Layer	Material	Al - Si (Si: 1.0% ±0.1%)
	Width	6 µm
	Spacing	7 µm
	Thickness	20,000Å
Contact Hole Dimension		8 µm X 8 µm
Insulation Layer	Material	PSG (SiO_2)
	Thickness	1.5 µm
Passivation	Material	PSG (SiO_2)
	Thickness	1.5 µm
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	8 Lead PDIP / SO-8
	Materials	EME6300 / MP150 / MP190
Remarks:		

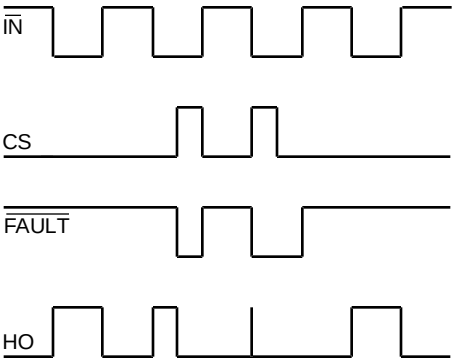


Figure 1. Input/Output Timing Diagram

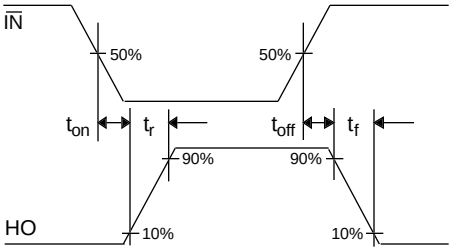


Figure 2. Switching Time Waveform Definition

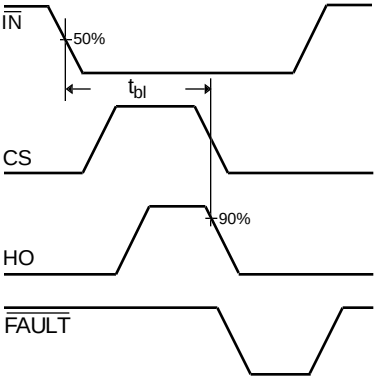


Figure3. Start-up Blanking Time Waveform Definitions

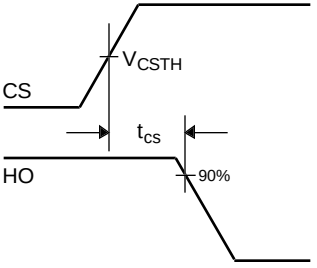


Figure 4. CS Shutdown Waveform Definitions

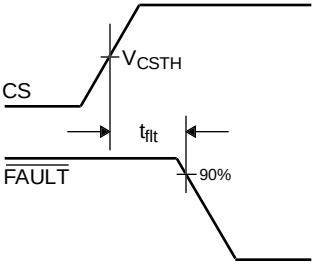


Figure 5. CS to FAULT Waveform Definitions