International
IOR Rectifier

Data Sheet No. PD60207 Rev.A

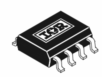
IR2302(S) & (PbF)

HALF-BRIDGE DRIVER

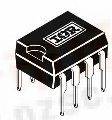
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 5 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels
- 8-Lead SOIC also available LEAD-FREE (PbF).

Packages



8-Lead SOIC
IR2302(S)
(Also available LEAD-FREE (PbF))



8-Lead PDIP
IR2302

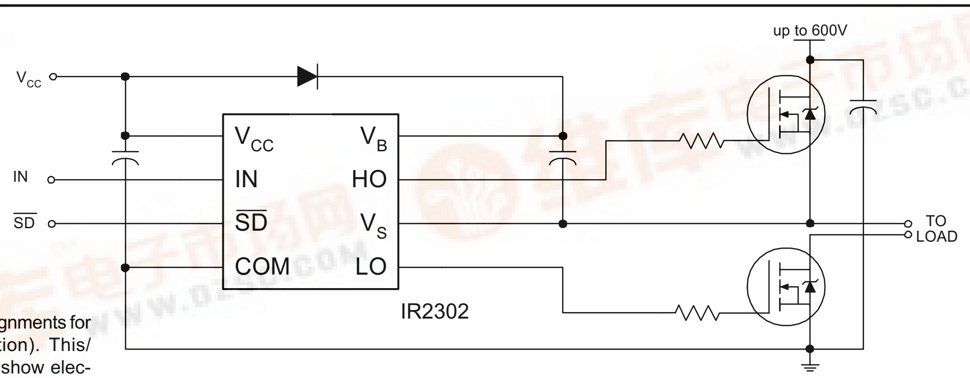
2106/2301//2108//2109/2302/2304 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106/2301	HIN/LIN	no	none	COM
21064				VSS/COM
2108	HIN/$\overline{LIN}$	yes	Internal 540ns	COM
21084			Programmable 0.54~5μs	VSS/COM
2109/2302	IN/$\overline{SD}$	yes	Internal 540ns	COM
21094			Programmable 0.54~5μs	VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM

Description

The IR2302(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/ These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		COM - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 5	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	5	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	COM	V_{CC}	
T_A	Ambient temperature	-40	150	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF, and T_A = 25°C unless otherwise specified.

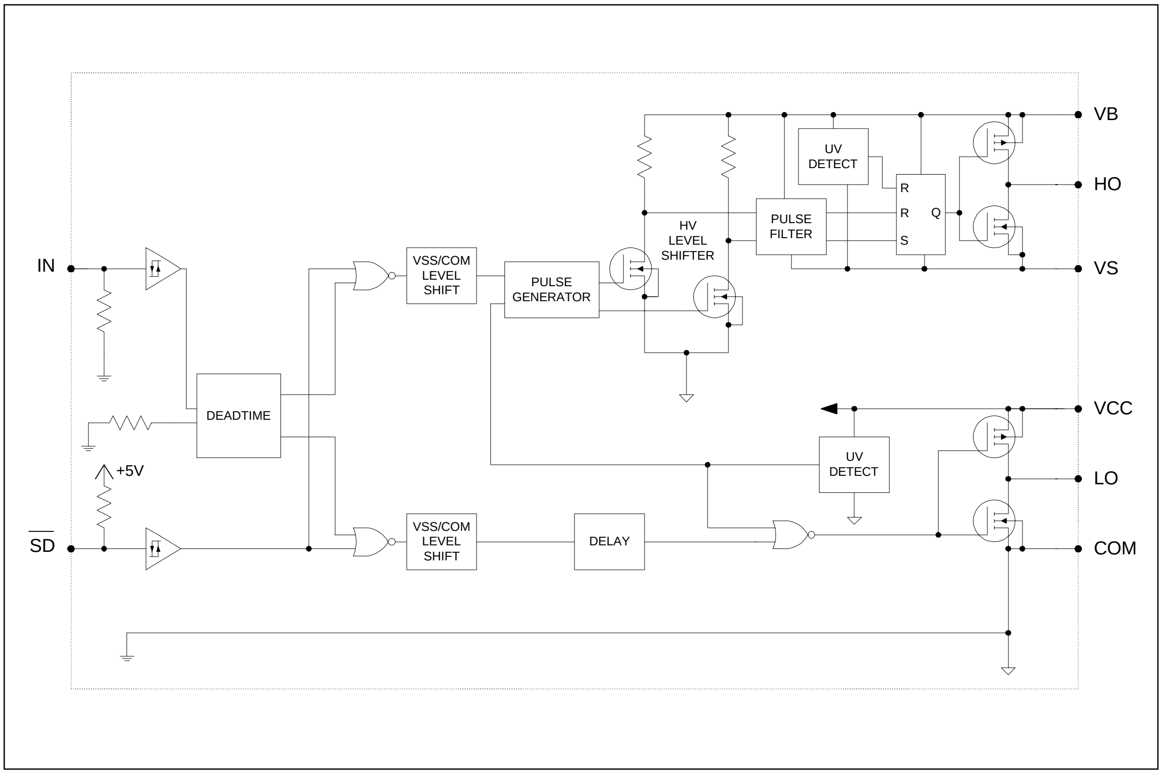
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	550	750	950	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	200	280		
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	130	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	400	540	680		
MDT	Deadtime matching = DT_{LO-HO} - DT_{HO-LO}	—	0	60		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.9	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.9	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	100		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current	—	5	20	µA	IN = 5V, SD = 0V
I_{IN-}	Logic "0" input bias current	—	—	2		IN = 0V, $\overline{SD}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	3.3	4.1	5	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	3	3.8	4.7		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.1	0.3	—		
I_{O+}	Output high short circuit pulsed vurrent	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V,PW ≤ 10 µs

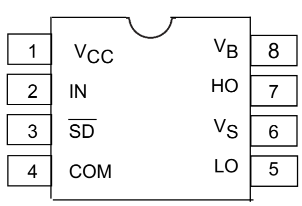
Functional Block Diagrams



Lead Definitions

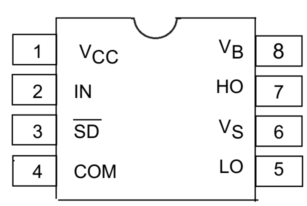
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
$\overline{SD}$	Logic input for shutdown
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8 Lead PDIP

IR2302



8 Lead SOIC
(Also available LEAD-FREE (PbF)

IR2302S

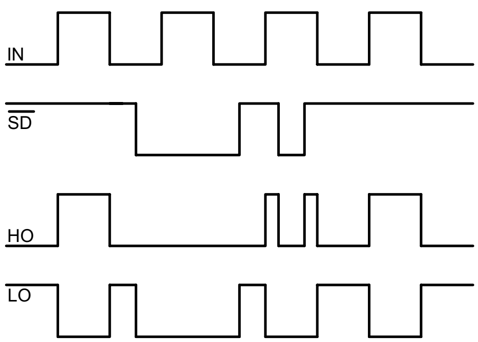


Figure 1. Input/Output Timing Diagram

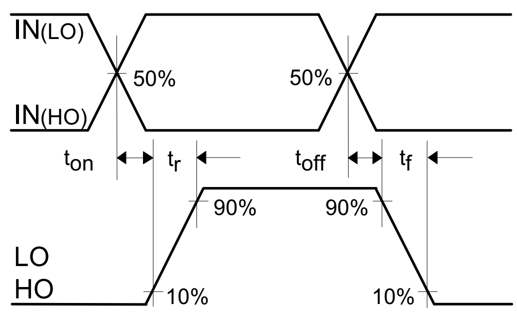


Figure 2. Switching Time Waveform Definitions

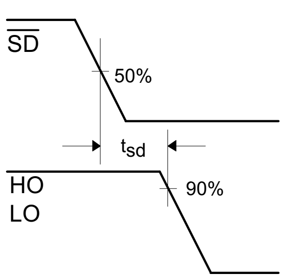


Figure 3. Shutdown Waveform Definitions

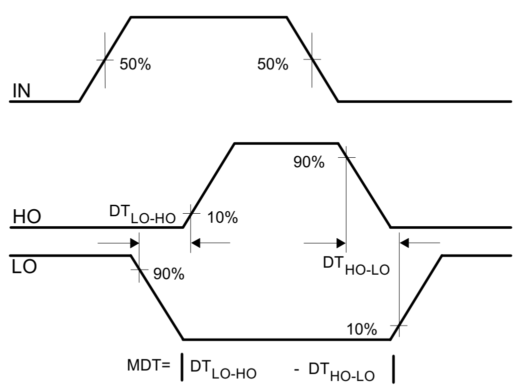


Figure 4. Deadtime Waveform Definitions

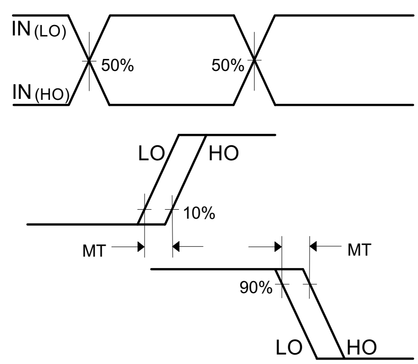


Figure 5. Delay Matching Waveform Definitions

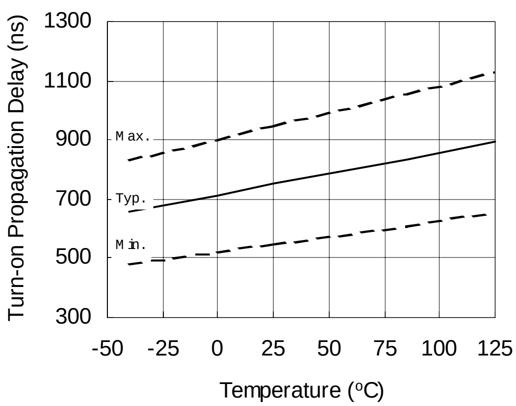


Figure 6A. Turn-on Propagation Delay vs. Temperature

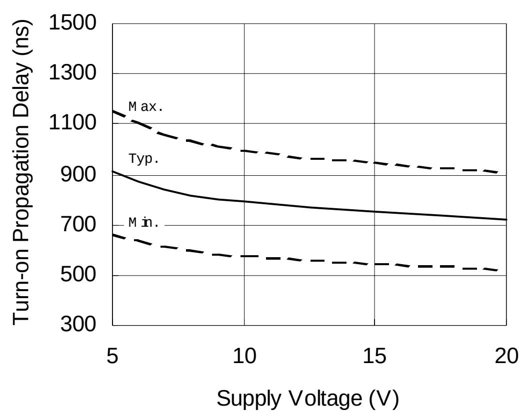


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

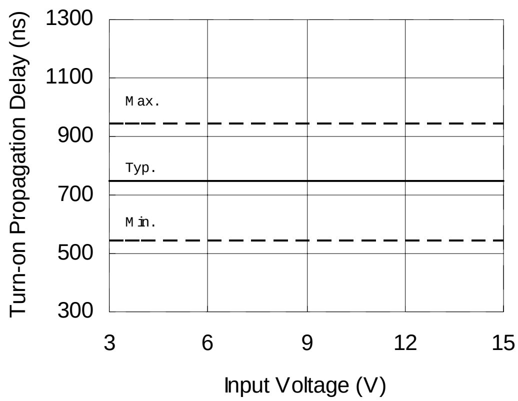


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

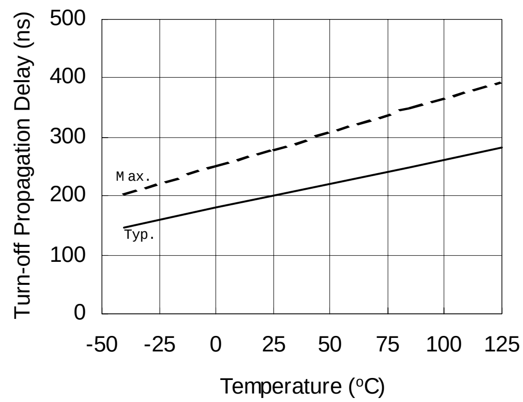


Figure 7A. Turn-off Propagation Delay vs. Temperature

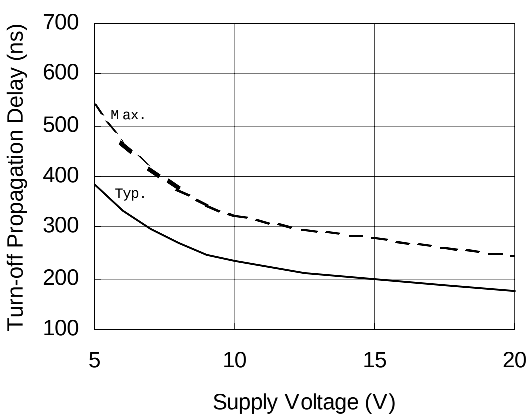


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

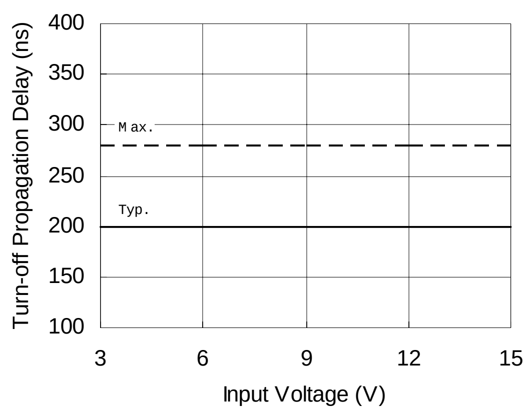


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

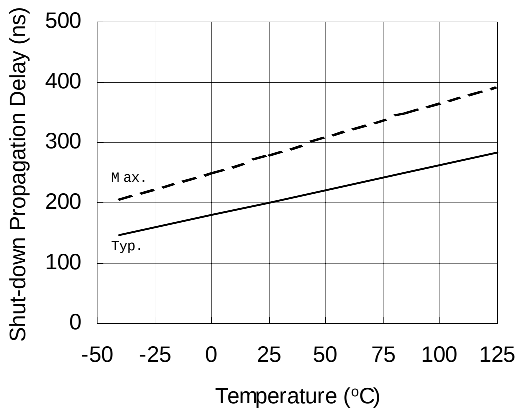


Figure 8A. Shut-down Propagation Delay vs. Temperature

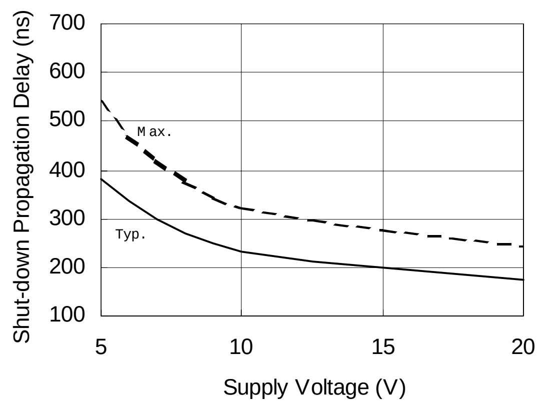


Figure 8B. Shut-down Propagation Delay vs. Supply Voltage

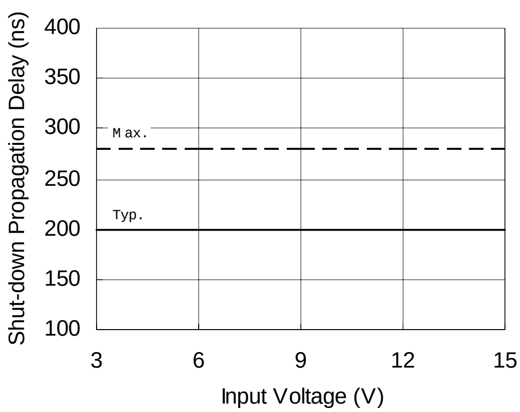


Figure 8C. Shut-down Propagation Delay vs. Input Voltage

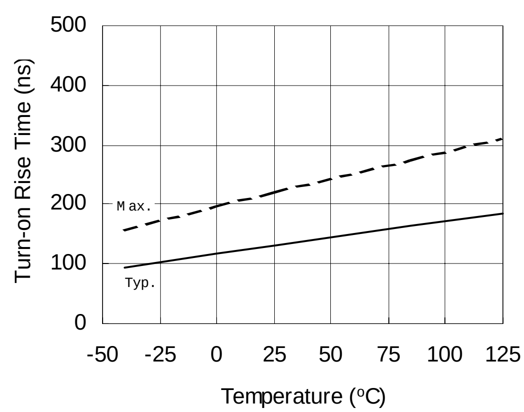


Figure 9A. Turn-on Rise Time vs. Temperature

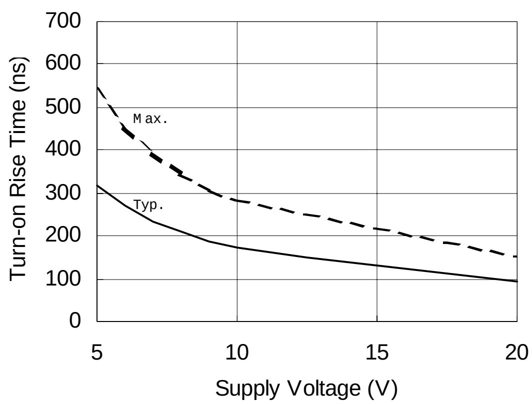


Figure 9B. Turn-on Rise Time vs. Supply Voltage

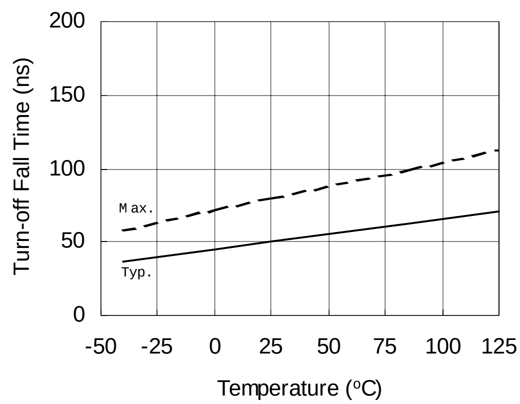


Figure 10A. Turn-off Fall Time vs. Temperature

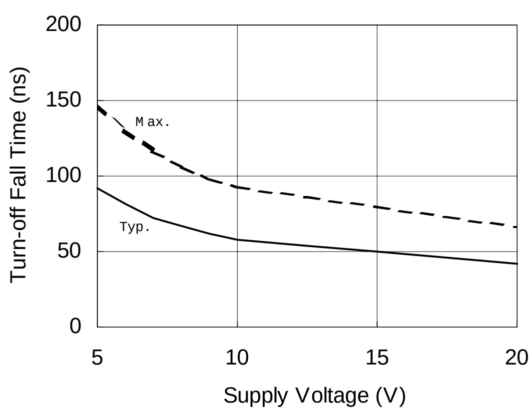


Figure 10B. Turn-off Fall Time vs. Supply Voltage

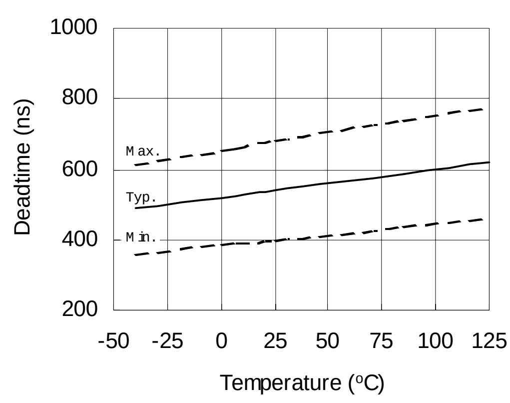


Figure 11A. Deadtime vs. Temperature

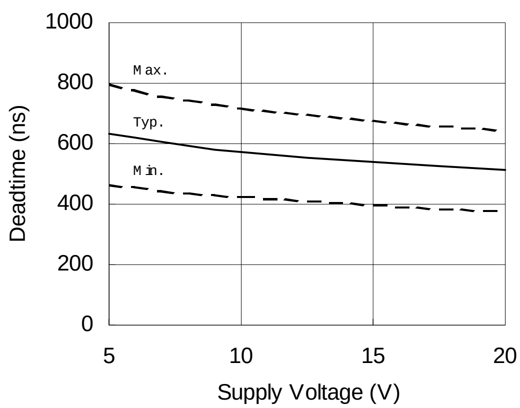


Figure 11B. Deadtime vs. Supply Voltage

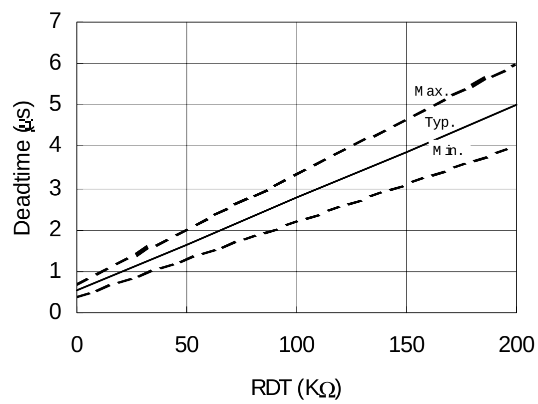


Figure 11C. Deadtime vs. RDT

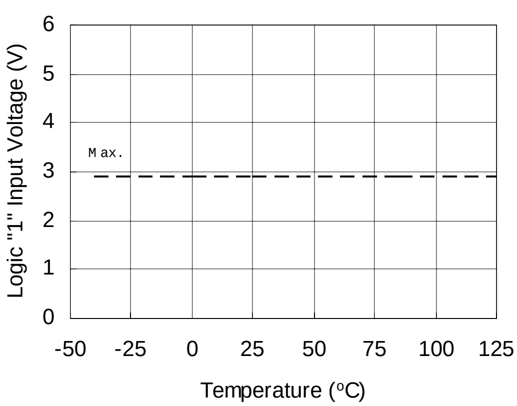


Figure 12A. Logic "1" Input Voltage vs. Temperature

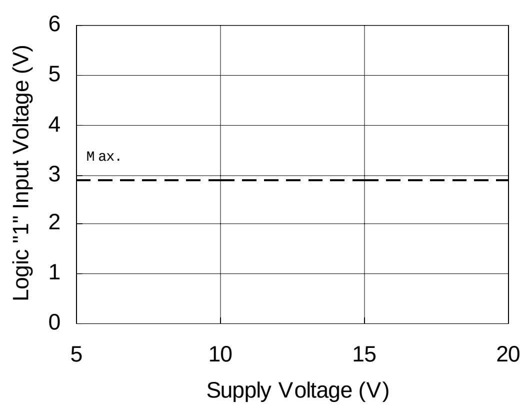


Figure 12B. Logic "1" Input Voltage vs. Supply Voltage

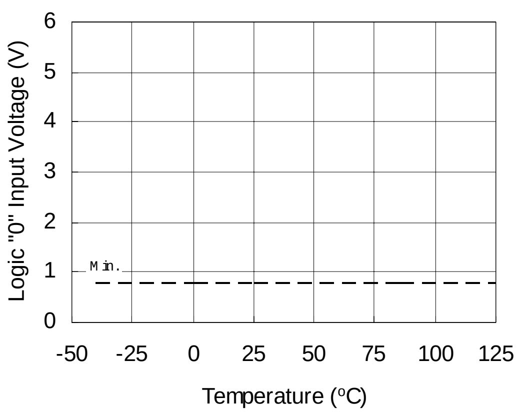


Figure 13A. Logic "0" Input Voltage vs. Temperature

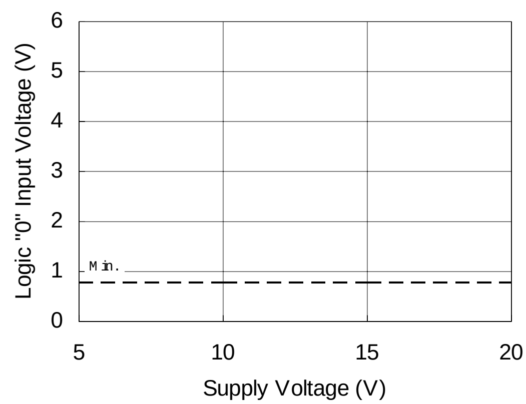


Figure 13B. Logic "0" Input Voltage vs. Supply Voltage

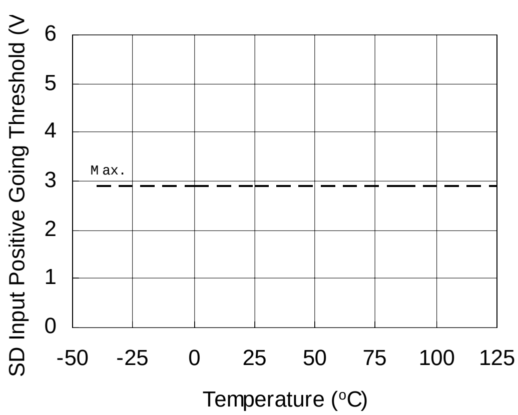


Figure 14A. SD Input Positive Going Threshold vs. Temperature

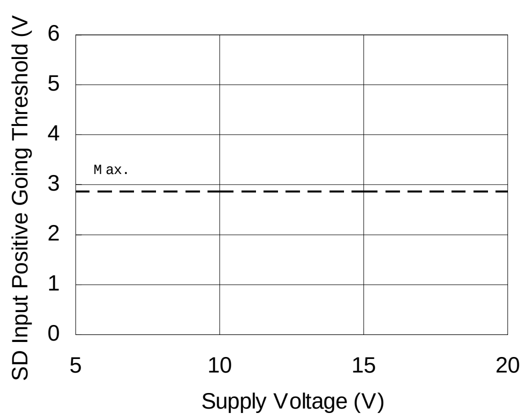


Figure 14B. SD Input Positive Going Threshold vs. Supply Voltage

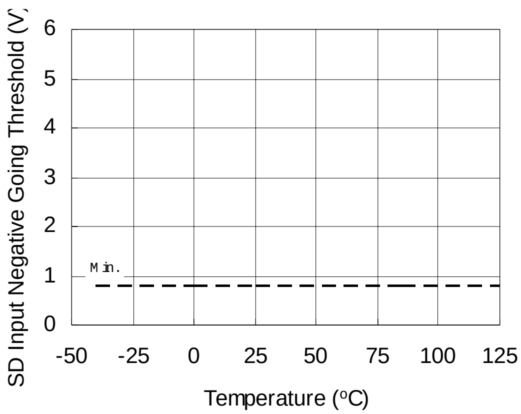


Figure 15A. SD Input Negative Going Threshold vs. Temperature

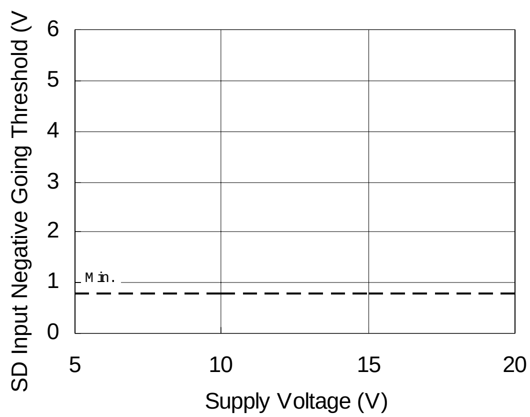


Figure 15B. SD Input Negative Going Threshold vs. Supply Voltage

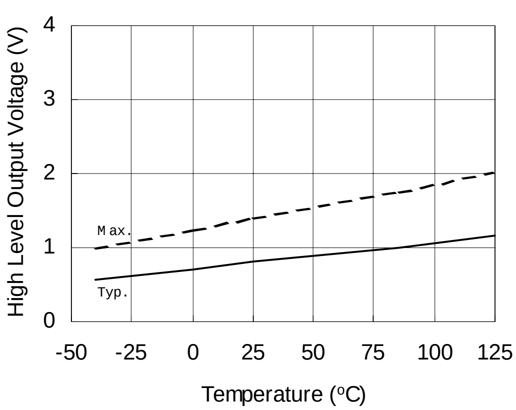


Figure 16A. High Level Output Voltage vs. Temperature

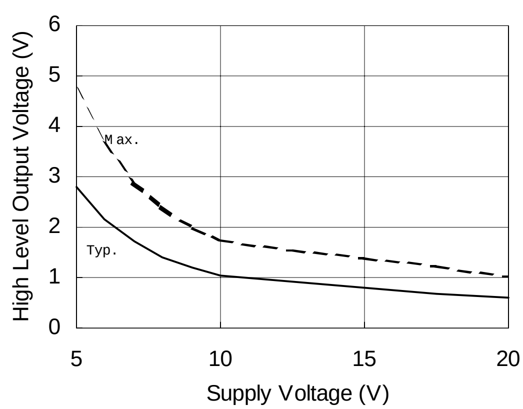


Figure 16B. High Level Output Voltage vs. Supply Voltage

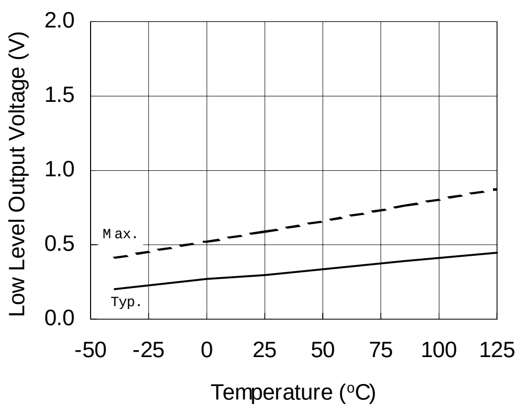


Figure 17A. Low Level Output Voltage vs. Temperature

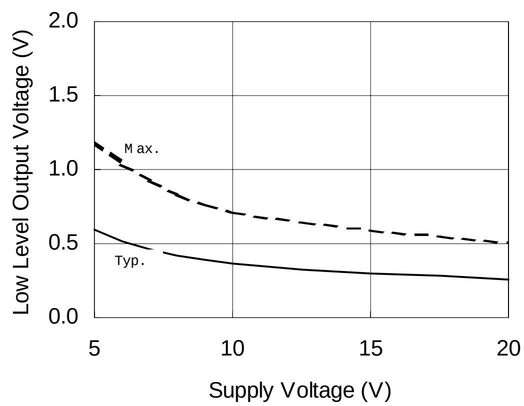


Figure 17B. Low Level Output Voltage vs. Supply Voltage

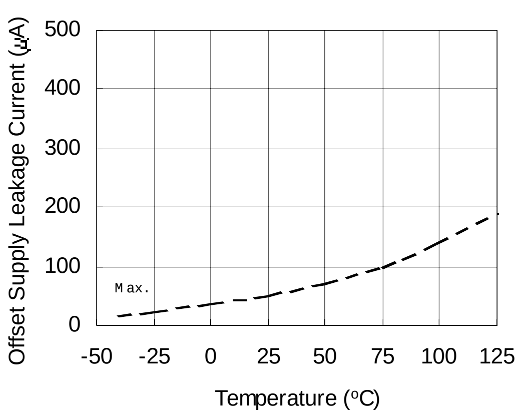


Figure 18A. Offset Supply Leakage Current vs. Temperature

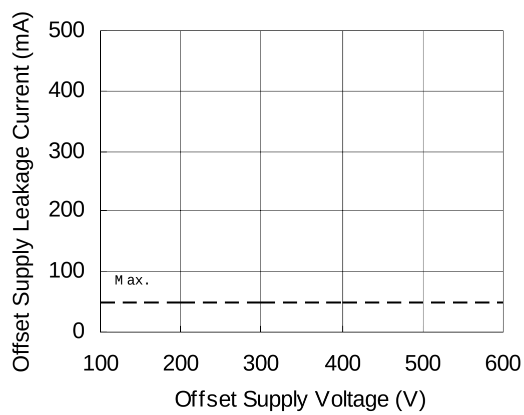


Figure 18B. Offset Supply Leakage Current vs. Offset Supply Voltage

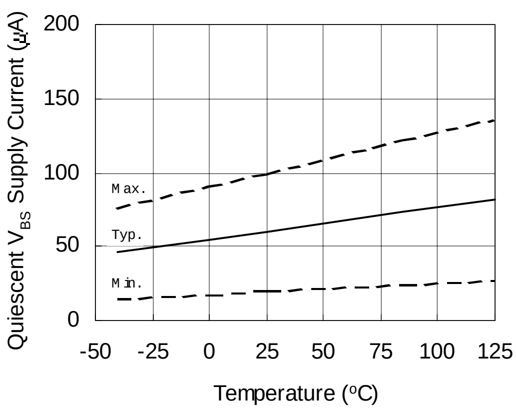


Figure 19A. Quiescent V_{BS} Supply Current vs. Temperature

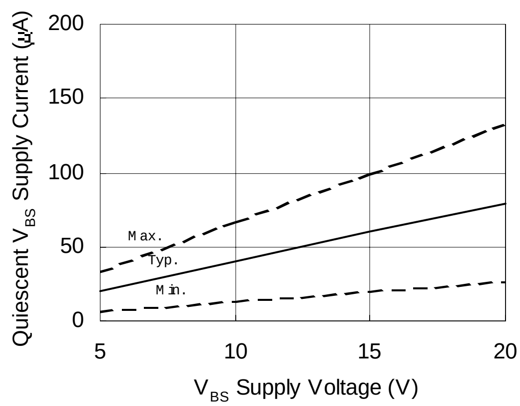


Figure 19B. Quiescent V_{BS} Supply Current vs. V_{BS} Supply Voltage

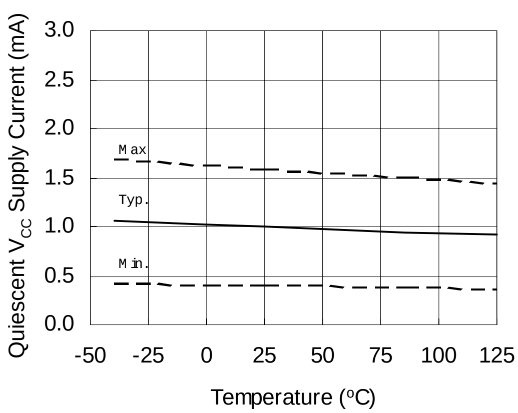


Figure 20A. Quiescent V_{CC} Supply Current vs. Temperature

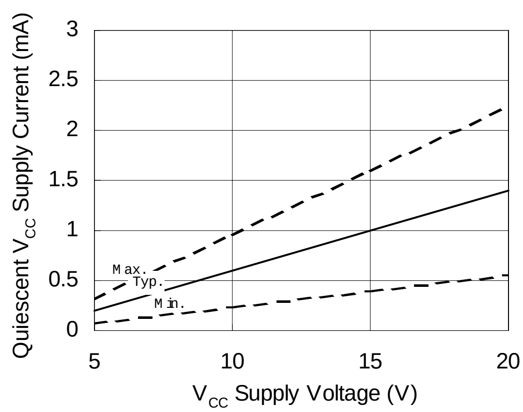


Figure 20B. Quiescent V_{CC} Supply Current vs. V_{CC} Supply Voltage

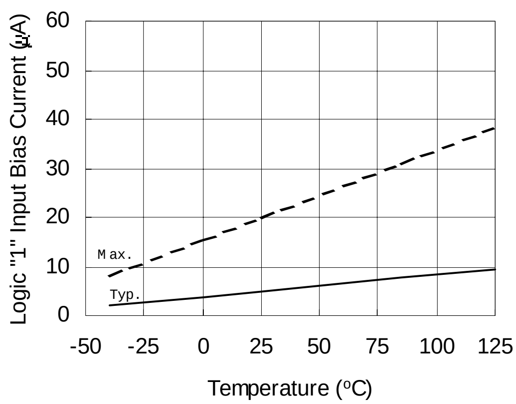


Figure 21A. Logic "1" Input Bias Current vs. Temperature

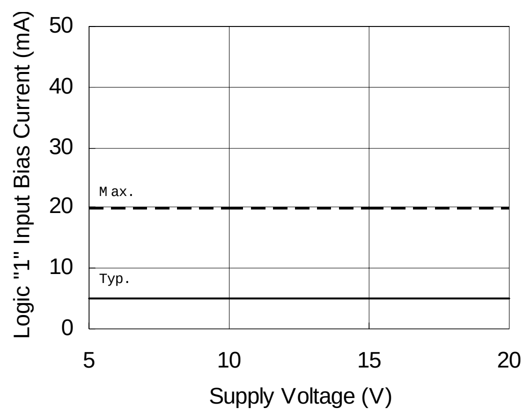


Figure 21B. Logic "1" Input Bias Current vs. Supply Voltage

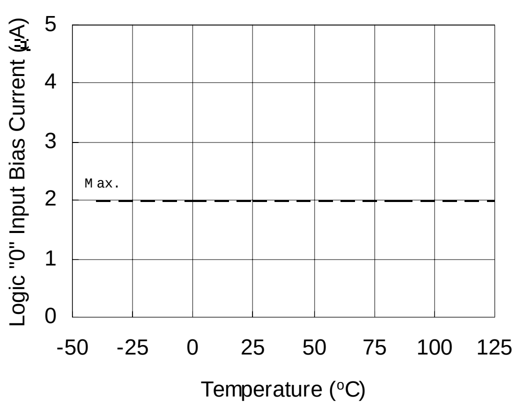


Figure 22A. Logic "0" Input Bias Current vs. Temperature

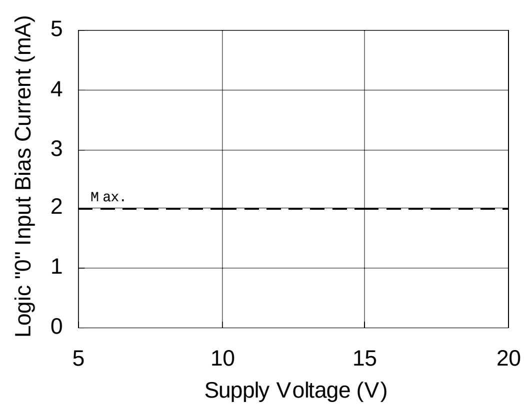


Figure 22B. Logic "0" Input Bias Current vs. Supply Voltage

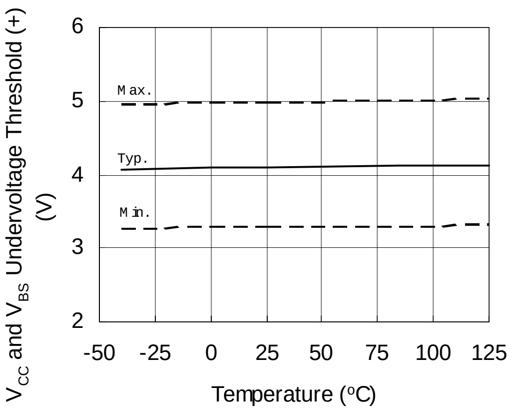


Figure 23. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

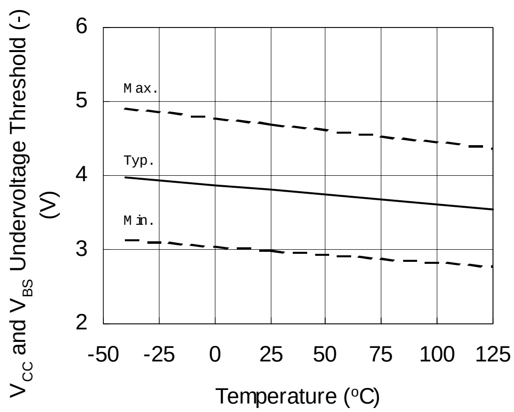


Figure 24. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

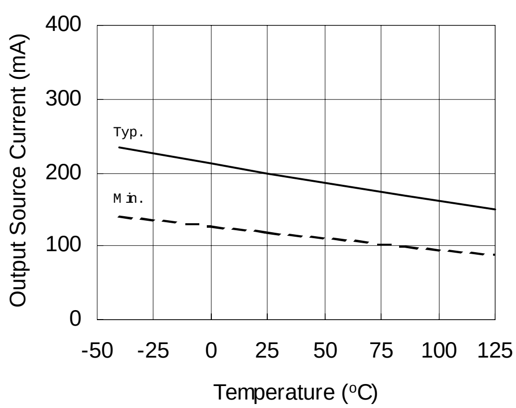


Figure 25A. Output Source Current vs. Temperature

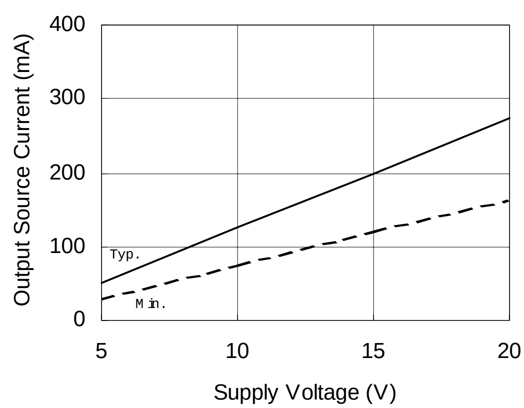


Figure 25B. Output Source Current vs. Supply Voltage

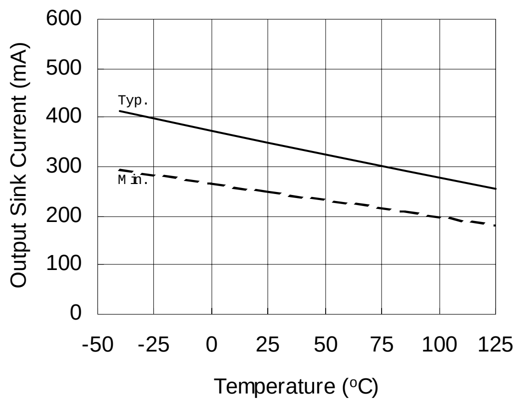


Figure 26A. Output Sink Current vs. Temperature

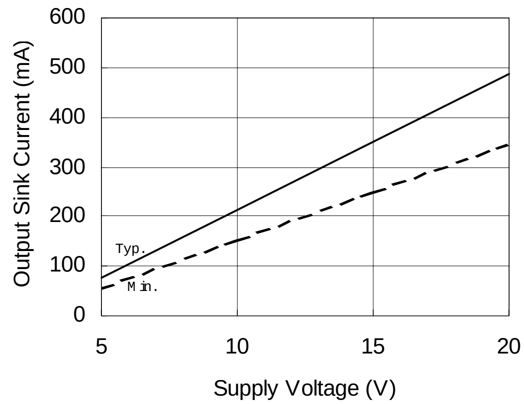


Figure 26B. Output Sink Current vs. Supply Voltage

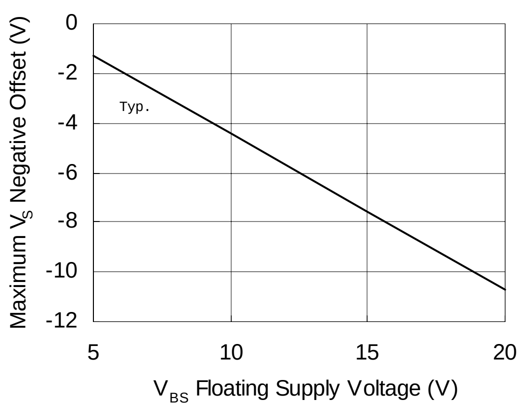


Figure 27. Maximum V_S Negative Offset vs. V_{BS} Floating Supply Voltage

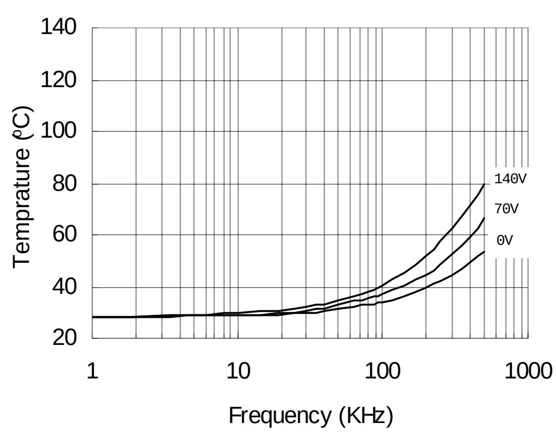


Figure 28. IR2302 vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15V

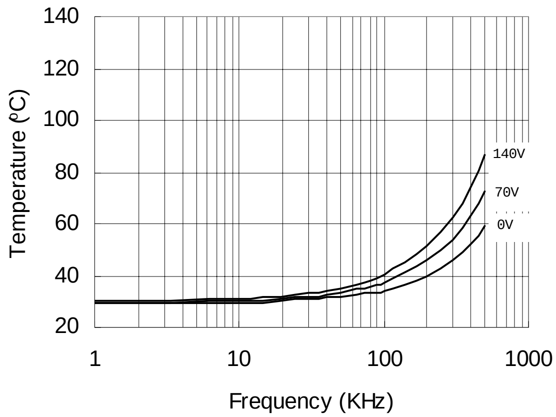


Figure 29. IR2302 vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15V

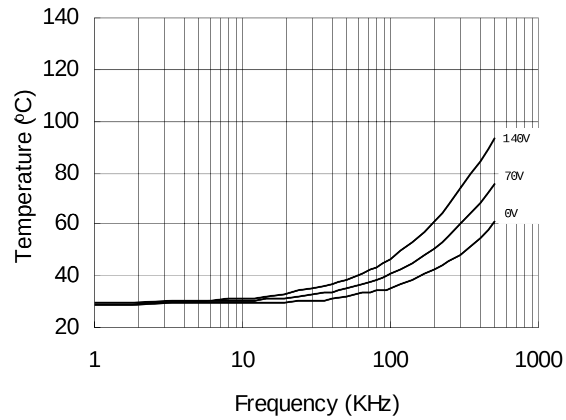


Figure 30. IR2302 vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15V

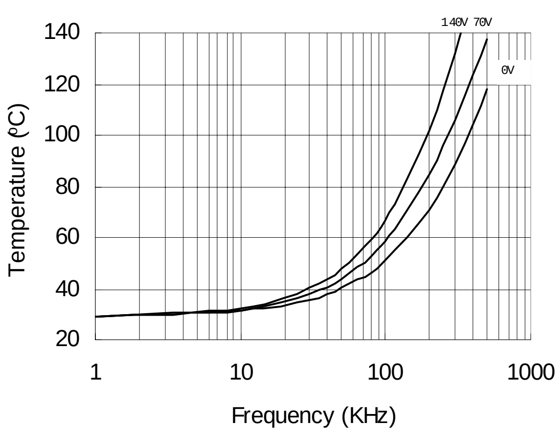


Figure 31. IR2302 vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V

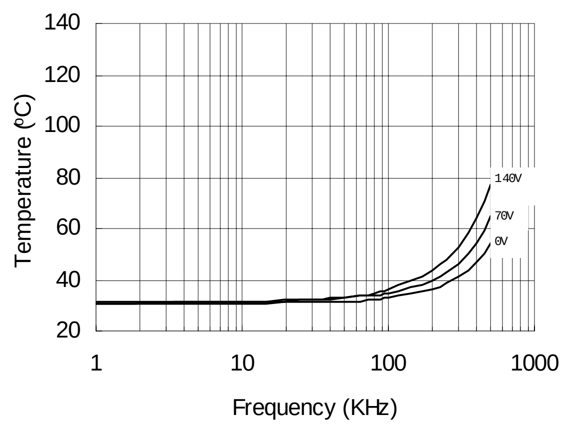


Figure 32. IR2302S vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15V

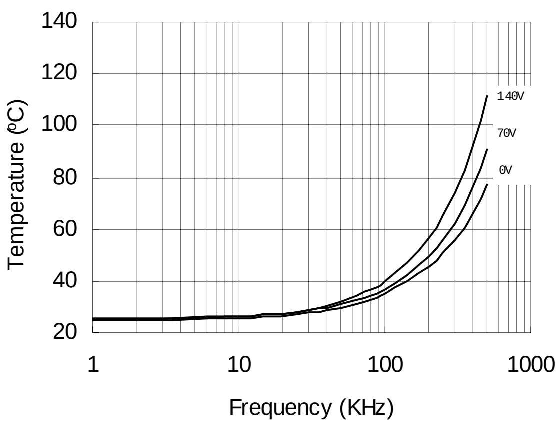


Figure 33. IR2302S vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15V

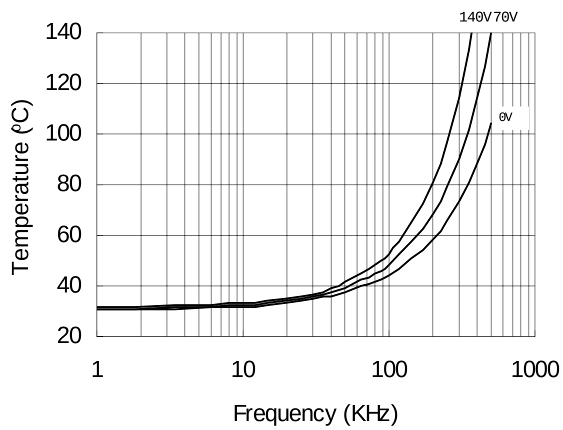


Figure 34. IR2302S vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15V

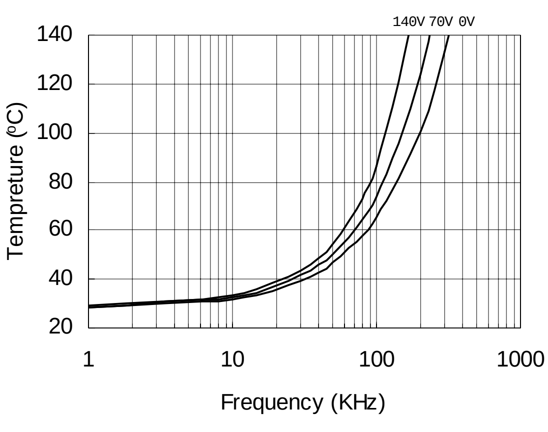
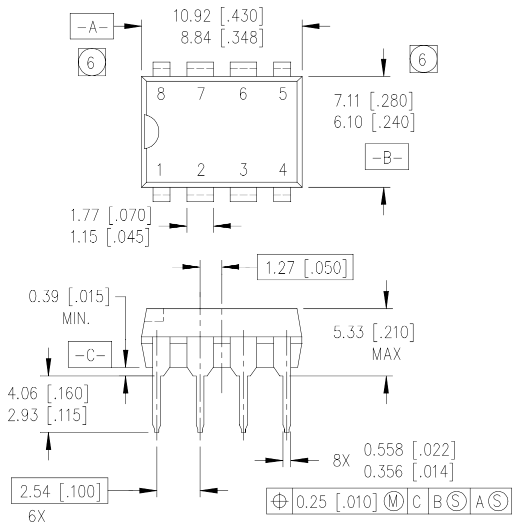
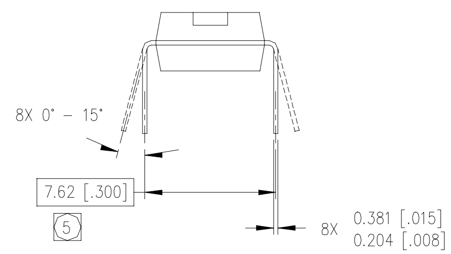


Figure 35. IR2302S vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V

Case Outlines

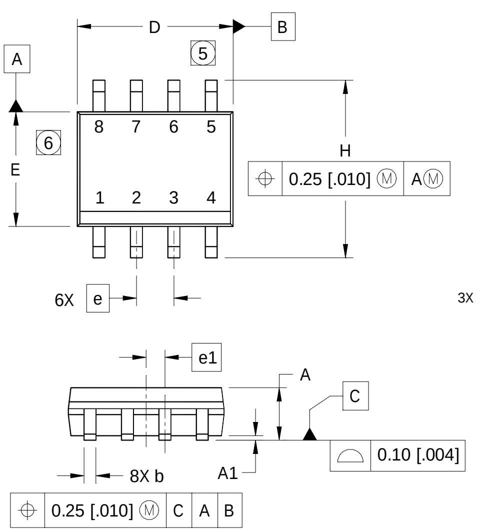


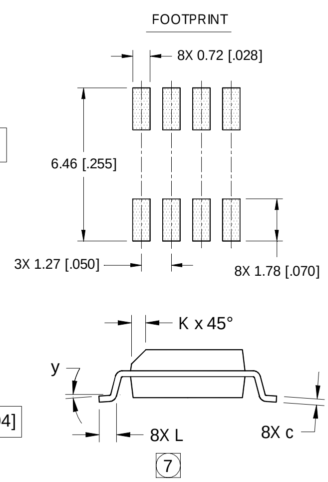
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



01-6014
01-3003 01 (MS-001AB)

8 Lead PDIP





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

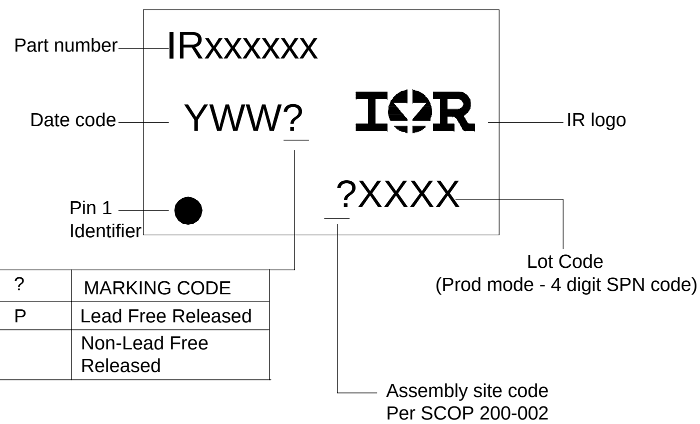
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8 Lead SOIC

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead PDIP IR2302 order IR2302
8-Lead SOIC IR2302S order IR2302S

Leadfree Part
8-Lead PDIP R2302 not available
8-Lead SOIC IR2302S order IR2302SPbF

International Rectifier

Thisproduct has been designed and qualified for the Automotive market.
Qualification Standards can be found on IR's Web Site *http://www.irf.com*
Data and specifications subject to change without notice.

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8/16/2004