International
IOR Rectifier

IR3081

DATA SHEET

XPHASE™ VR 10.0 CONTROL IC

DESCRIPTION

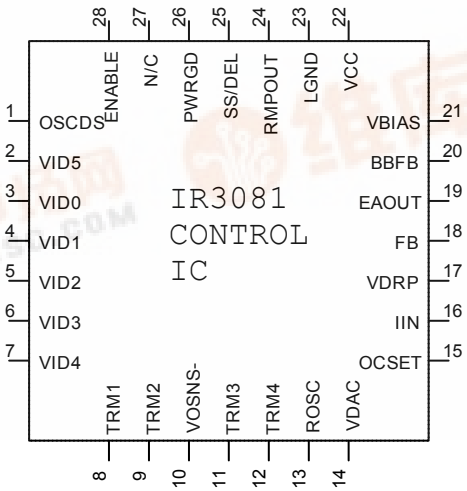
The IR3081 Control IC combined with an IR *XPhase*™ Phase IC provides a full featured and flexible way to implement a complete VR 10.0 power solution. The "Control" IC provides overall system control and interfaces with any number of "Phase ICs" which each drive and monitor a single phase of a multiphase converter. The X*Phase*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

The IR3081 is intended for VRD or VRM/EVRD 10.0 applications that use external VCCVID/VTT circuits.

FEATURES

- 6 bit VR 10.0 compatible VID with 0.5% overall system accuracy
- Programmable Dynamic VID Slew Rate
- No Discharge of output capacitors during Dynamic VID step-down (can be disabled)
- +/-300mV Differential Remote Sense
- Programmable 150kHz to 1MHz oscillator
- Programmable VID Offset and Load Line output impedance
- Programmable Softstart
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Simplified Powergood provides indication of proper operation and avoids false triggering
- Operates from 12V input with 9.1V Under-Voltage Lockout
- 6.8V/5mA Bias Regulator provides System Reference Voltage
- Enable Input
- Small thermally enhanced 28L MLPQ package

PACKAGE PINOUT



ORDERING INFORMATION

Device	Order Quantity
IR3081MTR	3000 per Reel
IR3081M	5 per Bag

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC standard

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	OSCDS	20V	-0.3V	1mA	1mA
2-7	VID0-5	20V	-0.3V	10mA	10mA
8, 9, 11,12	TRM1-4	Do Not Connect	Do Not Connect	Do Not Connect	Do Not Connect
10	VOSNS-	0.5V	-0.5V	10mA	10mA
13	ROSC	20V	-0.5V	1mA	1mA
14	VDAC	20V	-0.3V	1mA	1mA
15	OCSET	20V	-0.3V	1mA	1mA
16	IIN	20V	-0.3V	1mA	1mA
17	VDRP	20V	-0.3V	5mA	5mA
18	FB	20V	-0.3V	1mA	1mA
19	EAOUT	10V	-0.3V	10mA	20mA
20	BBFB	20V	-0.3V	1mA	1mA
21	VBIAS	20V	-0.3V	1mA	1mA
22	VCC	20V	-0.3V	1mA	50mA
23	LGND	n/a	n/a	50mA	1mA
24	RMPOUT	20V	-0.3V	1mA	1mA
25	SS/DEL	20V	-0.3V	1mA	1mA
26	PWRGD	20V	-0.3V	1mA	20mA
27	N/C	n/a	n/a	n/a	n/a
28	ENABLE	20V	-0.3V	1mA	1mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 9.5V ≤ V_{CC} ≤ 14V, 0 °C ≤ T_J ≤ 100 °C

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC Reference					
System Set-Point Accuracy	-0.3V ≤ VOSNS- ≤ 0.3V, Connect FB to EAOUT, Measure V(EAOUT) – V(VOSNS-) deviation from Table 1. Applies to all VID codes.		0.5		%
Source Current	R_{ROSC} = 41.9kΩ	68	80	92	μA
Sink Current	R_{ROSC} = 41.9kΩ	47	55	63	μA
VID Input Threshold		500	600	700	mV
VID Input Bias Current	0V ≤ VID0-5 ≤ VCC	-5	0	5	μA
Regulation Detect Comparator Input Offset		-5	0	5	mV
Regulation Detect to EAOUT Delay			130	200	ns
BBFB to FB Bias Current Ratio		0.95	1.00	1.05	μA/μA
VID 11111x Blanking Delay	Measure Time till PWRGD drives low		800		ns
VID Step Down Detect Blanking Time	Measure from VID inputs to EAOUT		1.7		μs
VID Down BB Clamp Voltage	Percent of VDAC voltage	70	75	80	%
VID Down BB Clamp Current		3.5	6.2	12	mA
Error Amplifier					
Input Offset Voltage	Connect FB to EAOUT, Measure V(EAOUT) – V(DAC). from Table 1. Applies to all VID codes and -0.3V ≤ VOSNS- ≤ 0.3V. Note 2	-3	4	8	mV
FB Bias Current	R_{ROSC} = 41.9kΩ	28	29.5	31	μA
DC Gain	Note 1	90	100	105	dB
Gain-Bandwidth Product	Note 1	4	7		MHz
Source Current		0.4	0.6	0.8	mA
Sink Current		0.7	1.2	1.7	mA
Max Voltage	VBIAS–VEAOUT (referenced to VBIAS)	125	250	375	mV
Min Voltage	Normal operation or Fault mode	30	100	150	mV
VDRP Buffer Amplifier					
Input Offset Voltage	V(VDRP) – V(IIN), 0.8V ≤ V(IIN) ≤ 5.5V	-8	0	8	mV
Input Voltage Range		0.8		5.5	V
Bandwidth (-3dB)	Note 1	1	6		MHz
Input Voltage Range		0.8		5.5	V
Slew Rate			10		V/μs
IIN Bias Current		0	0.75	1.5	μA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillator					
Switching Frequency	R_{ROSC} = 41.9kΩ	255	300	345	kHz
Peak Voltage (5V typical, measured as % of VBIAS)	R_{ROSC} = 41.9kΩ	70	71	74	%
Valley Voltage (1V typical, measured as % of VBIAS)	R_{ROSC} = 41.9kΩ	11	14	16	%
VBIAS Regulator					
Output Voltage	0 ≤ I(VBIAS) ≤ 5mA	6.5	6.8	7.1	V
Current Limit		6	15	30	mA
Soft Start and Delay					
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.85	1.3	1.5	V
Charge Current		40	70	100	μA
Discharge Current		4	6	9	μA
Charge/Discharge Current Ratio		10	11.5	13	μA/μA
Charge Voltage		3.7	4.0	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage	70	90	110	mV
Discharge Comparator Threshold		150	200	250	mV
Over-Current Comparator					
Input Offset Voltage	1V ≤ V(OCSET) ≤ 5V	-10	0	10	mV
OCSET Bias Current	R_{ROSC} = 41.9kΩ	28	29.5	31	μA
PWRGD Output					
Output Voltage	I(PWRGD) = 4mA		150	400	mV
Leakage Current	V(PWRGD) = 5.5V		0	10	μA
Enable Input					
Threshold voltage		500	600	700	mV
Bias Current	0V ≤ V(ENABLE) ≤ VCC	-5	0	5	μA
VCC Under-Voltage Lockout					
Start Threshold		8.6	9.1	9.6	V
Stop Threshold		8.4	8.9	9.4	V
Hysteresis	Start – Stop	150	200	300	mV
General					
VCC Supply Current		8	11	14	mA
VOSNS- Current	-0.3V ≤ VOSNS- ≤ 0.3V, All VID Codes	3.5	4.5	5.5	mA

Note 1: Guaranteed by design, but not tested in production
Note 2: VDAC Output is trimmed to compensate for Error Amp input offsets errors

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	OSCDS	Apply a voltage greater than VBIAS to disable the oscillator. Used during factory testing & trimming. Ground or leave open for normal operation.
2-7	VID0-5	Inputs to VID D to A Converter
8, 9, 11,12	TRM1-4	Used for precision post-package trimming of the VDAC voltage. Do not make any connection to these pins.
10	VOSNS-	Remote Sense Input. Connect to ground at the Load.
13	ROSC	Connect a resistor to VOSNS- to program oscillator frequency and FB, OCSET, BBFB, and VDAC bias currents
14	VDAC	Regulated voltage programmed by the VID inputs. Current Sensing and PWM operation are referenced to this pin. Connect an external RC network to VOSNS- to program Dynamic VID slew rate.
15	OCSET	Programs the hiccup over-current threshold through an external resistor tied to VDAC and an internal current source. Over-current protection can be disabled by connecting this pin to a DC voltage no greater than 6.5V (do not float this pin as improper operation will occur).
16	IIN	Current Sense input from the Phase IC(s). To ensure proper operation bias to at least 250mV (don't float this pin).
17	VDRP	Buffered IIN signal. Connect an external RC network to FB to program converter output impedance
18	FB	Inverting input to the Error Amplifier. Converter output voltage is offset from the VDAC voltage through an external resistor connected to the converter output voltage at the load and an internal current source.
19	EAOUT	Output of the Error Amplifier
20	BBFB	Input to the Regulation Detect Comparator. Connect to converter output voltage and VDRP pin through resistor network to program recovery from VID step-down. Connect to ground to disable Body Braking™ during transition to a lower VID code.
21	VBIAS	6.8V/5mA Regulated output used as a system reference voltage for internal circuitry and the Phase ICs.
22	VCC	Power for internal circuitry
23	LGND	Local Ground and IC substrate connection
24	RMPOUT	Oscillator Output voltage. Used by Phase ICs to program Phase Delay
25	SS/DEL	Controls Converter Softstart, Power Good, and Over-Current Timing. Connect an external capacitor to LGND to program the timing. An optional resistor can be added in series with the capacitor to program the over-current delay time.
26	PWRGD	Open Collector output that drives low during Softstart and any external fault condition. Connect external pull-up.
27	N/C	No internal connection
28	ENABLE	Enable Input. A logic low applied to this pin puts the IC into Fault mode.

SYSTEM THEORY OF OPERATION

XPhase™ Architecture

The *XPhase*™ architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current and fast transient response. The architecture can be used in any multiphase converter ranging from 1 to 16 or more phases where flexibility facilitates the design trade-off of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 1, the *XPhase*™ architecture consists of a Control IC and a scalable array of phase converters each using a single Phase IC. The Control IC communicates with the Phase ICs through a 5-wire analog bus, i.e. bias voltage, phase timing, average current, error amplifier output, and VID voltage. The Control IC incorporates all the system functions, i.e. VID, PWM ramp oscillator, error amplifier, bias voltage, and fault protections etc. The Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over-voltage protection, and current sensing and sharing.

There is no unused or redundant silicon with the *XPhase*™ architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation. PCB Layout is easier since the 5 wire bus eliminates the need for point-to-point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.

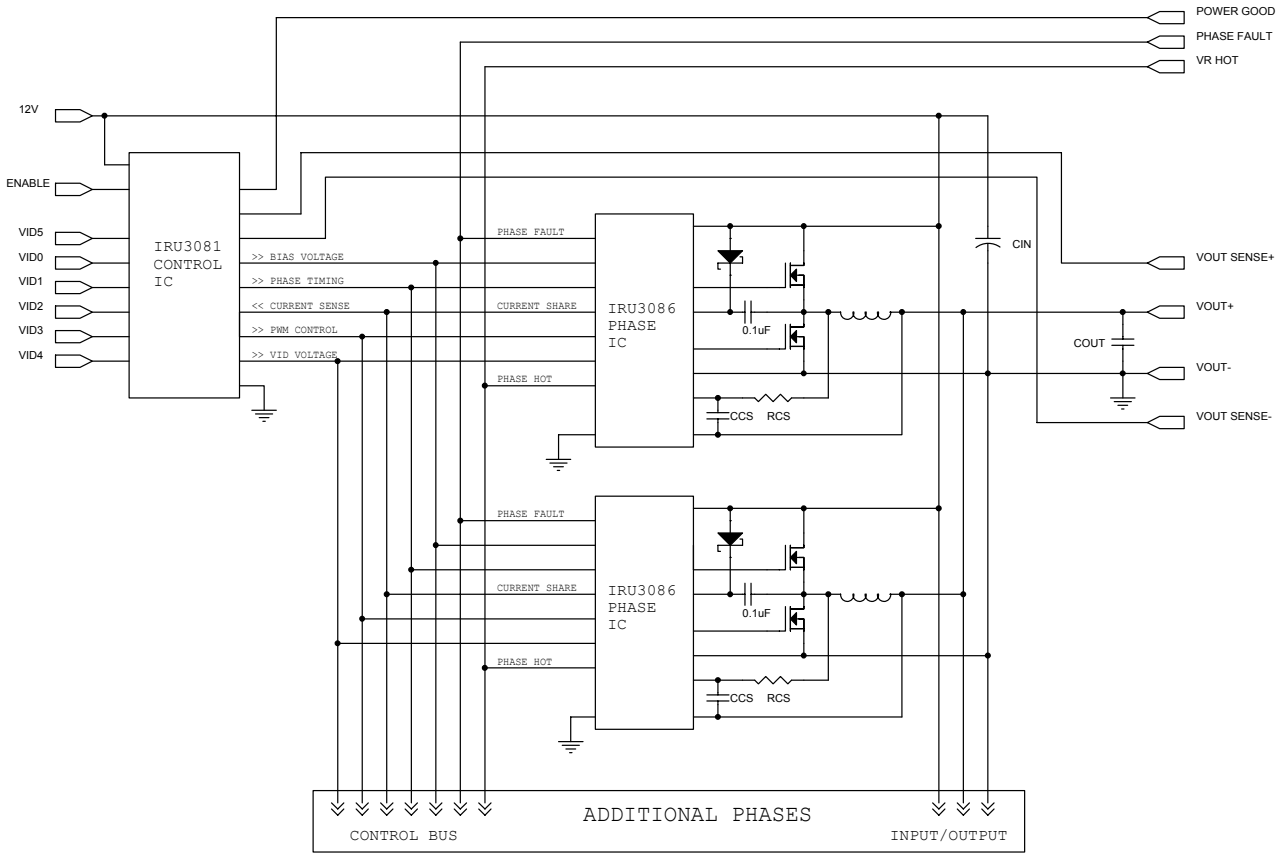


Figure 1 – System Block Diagram

PWM Control Method

The PWM block diagram of the *XPhase*™ architecture is shown in Figure 2. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed-forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to drops in the PCB related to changes in load current.

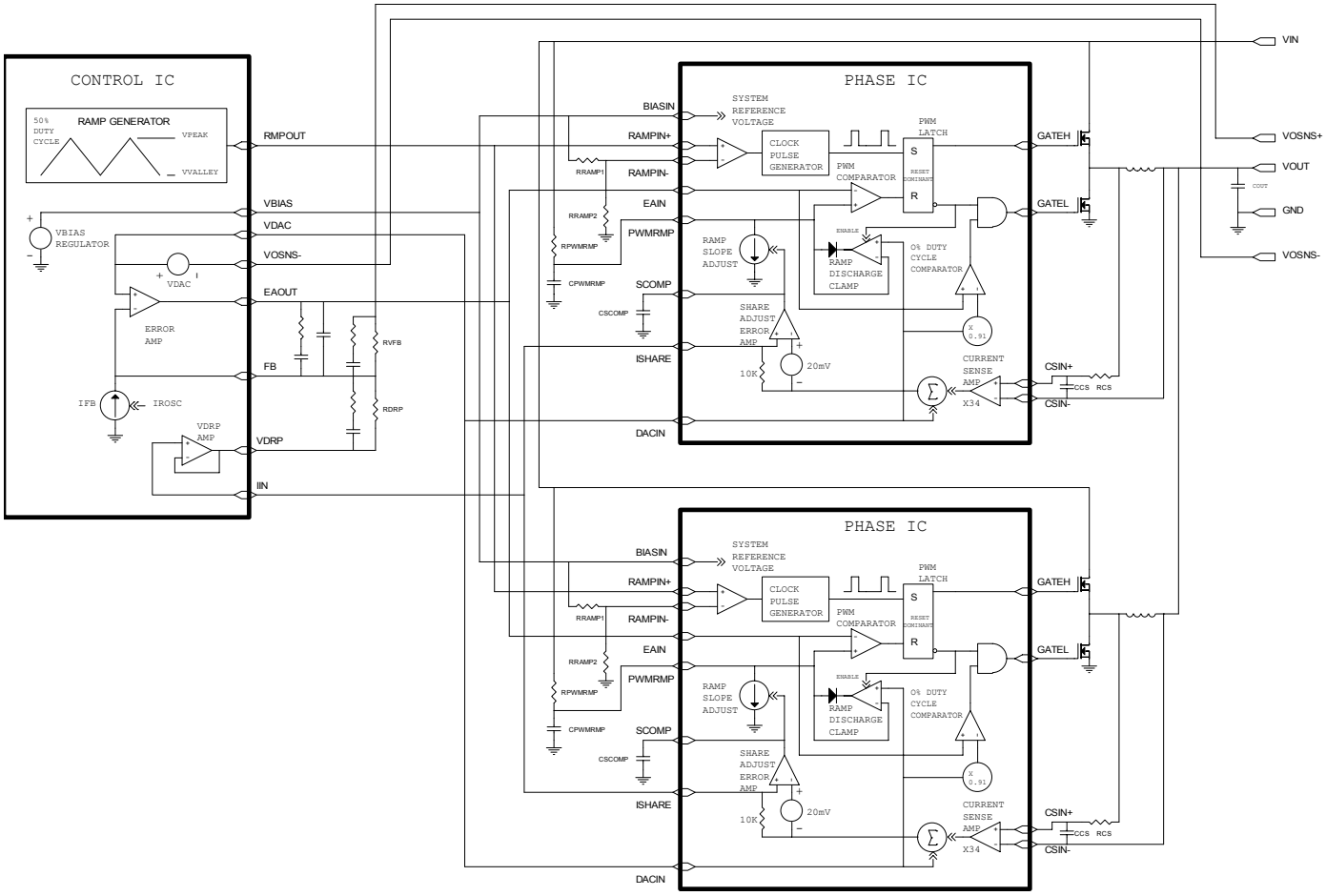


Figure 2 – PWM Block Diagram

Frequency and Phase Timing Control

The oscillator is located in the Control IC and its frequency is programmable from 150kHz to 1MHZ by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 5V and 1V. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider RRAMP1 and RRAMP2 connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform with the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 3 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for synchronization by swapping the RAMP + and – pins.

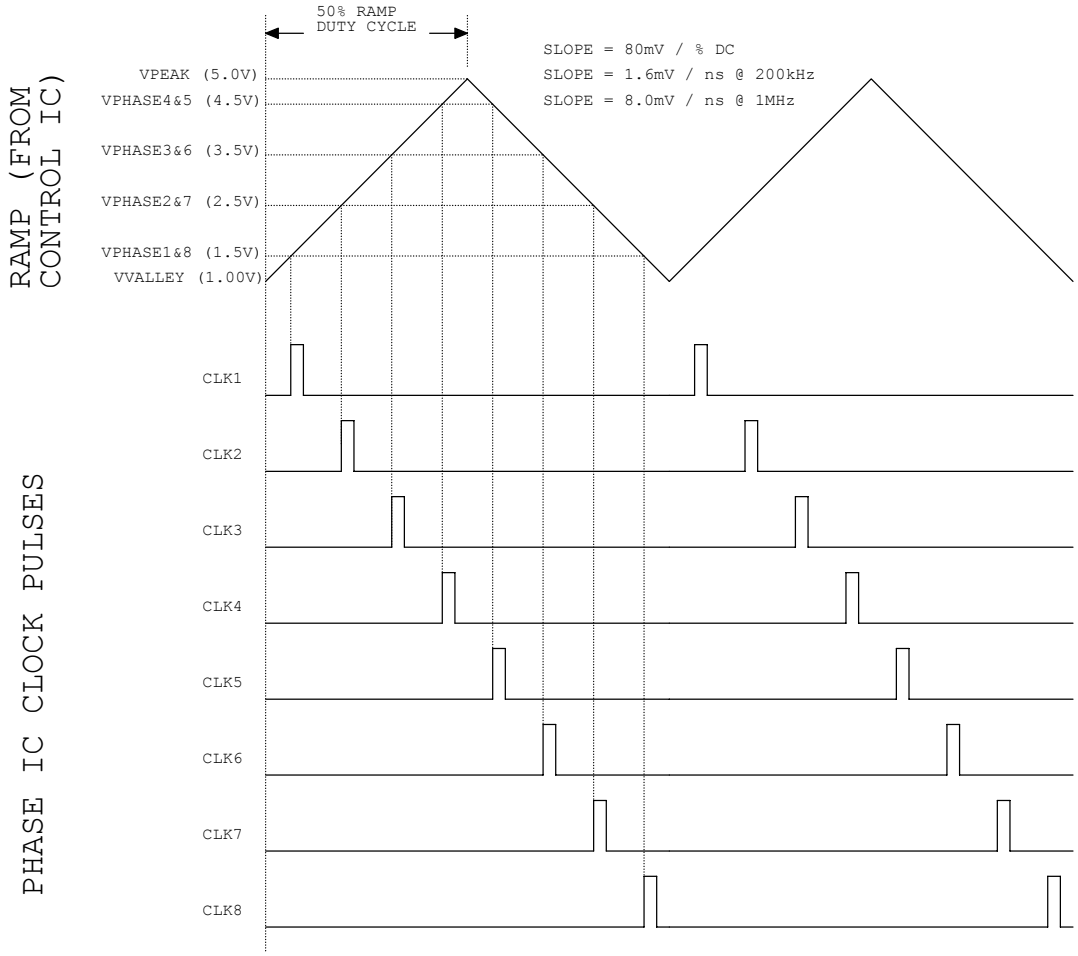


Figure 3 – 8 Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set, the PWMRMP voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. When the PWMRMP voltage exceeds the Error Amp's output voltage the PWM latch is reset. This turns off the high side driver, turns on the low side driver, and activates the Ramp Discharge Clamp. The clamp quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amp output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amp is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide “single cycle transient response” where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / Vout$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response
to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier’s body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (Vout + V_{BODY\ DIODE})$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as “body braking” and is accomplished through the “0% Duty Cycle Comparator” located in the Phase IC. If the Error Amp’s output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

Figure 4 depicts PWM operating waveforms under various conditions

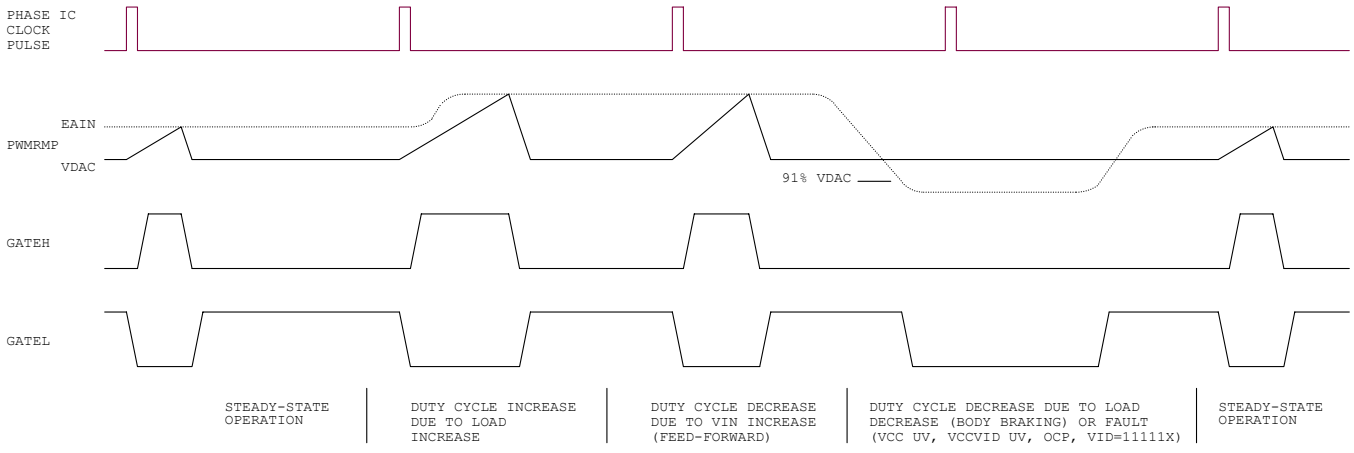


Figure 4 – PWM Operating Waveforms

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_SC_S} = i_L(s)\frac{R_L+sL}{1+sR_SC_S}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the Phase IC, as shown in figure 5. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (-1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to -20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the total current through all the inductors and is used by the Control IC for voltage positioning and current limit protection.

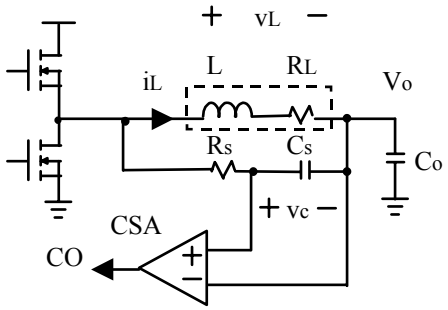


Figure 5 – Inductor Current Sensing and Current Sense Amplifier

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a 20mV offset. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

IR3081 THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3081 is shown in figure 6 and discussed in the following section.

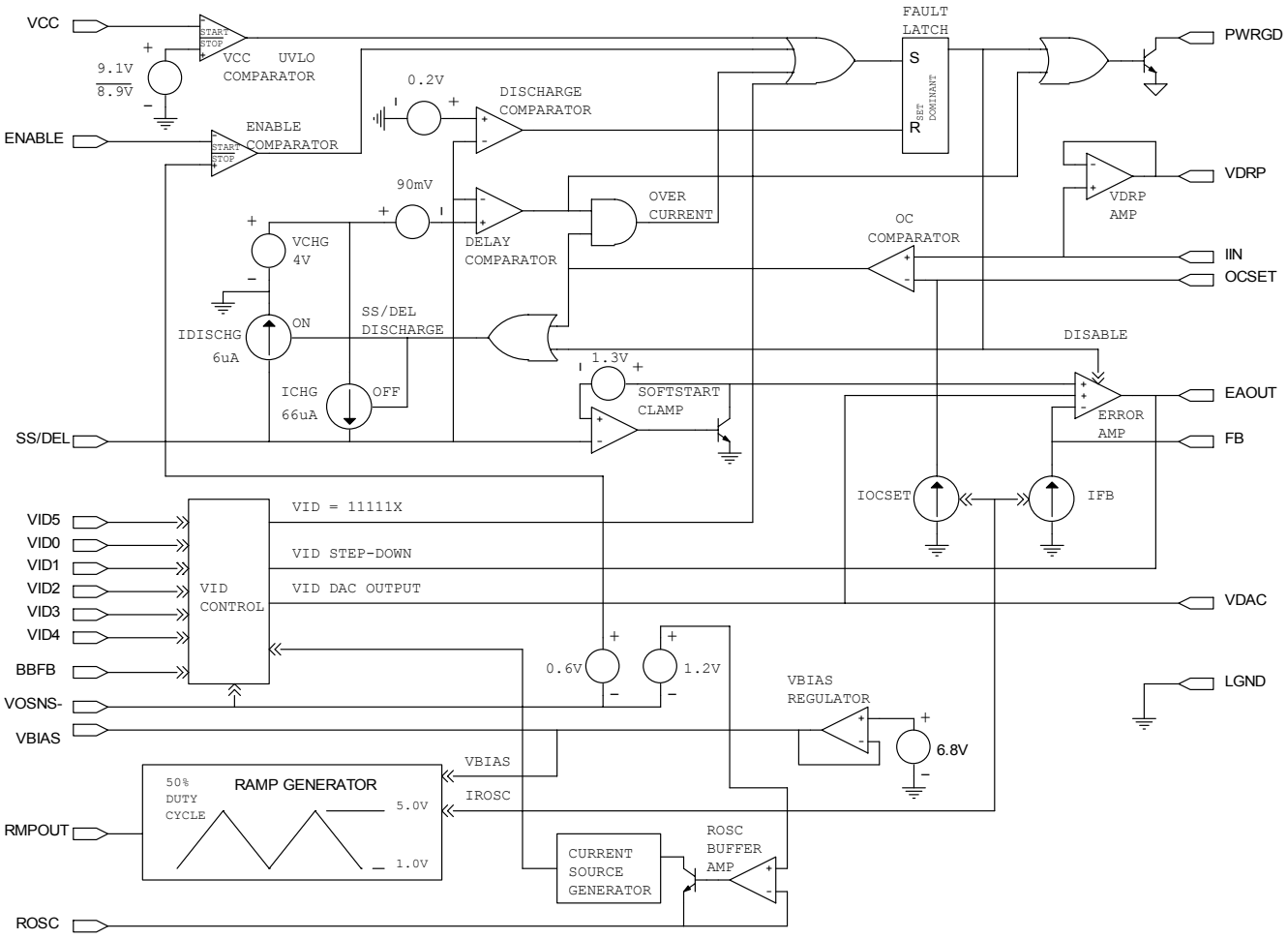


Figure 6 – IR3081 Block Diagram

VID Control

A 6-bit VID voltage compatible with VR 10.0, as shown in Table 1 is available at the VDAC pin. A detailed block diagram of the VID control circuitry can be found in Figure 7. The VID pins are require an external bias voltage and should not be floated. The VID input comparators, with 0.6V reference, monitor the VID pins and control the 6 bit Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amp is the VDAC pin. The VDAC voltage is post-package trimmed to compensate for the input offsets of the Error Amp to provide a 1.0% **system** accuracy. The actual VDAC voltage does not determine the system accuracy and has a wider tolerance.

The IR3081 can accept changes in the VID code while operating and vary the DAC voltage accordingly. The sink/source capability of the VDAC buffer amp is programmed by the same external resistor that sets the oscillator frequency. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and the VOSNS- pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

It is desirable to prevent negative inductor currents in response to a request for a lower VID code. Negative current transforms the buck converter into a boost converter and transfers energy from the output capacitors back into the input voltage. This energy can cause voltage spikes and damage the silver box or other components unless they are specifically designed to handle it. Furthermore, power is wasted during the transfer of energy from the output back to the input.

The IR3081 includes circuitry that turns off both control and synchronous MOSFETs in response to a lower VID code so that the load current discharges the output capacitors instead of the inductors. A lower VID code is detected by the VID step-down detect comparator which monitors the “fast” output of the DAC (plus 7mV for noise immunity) compared to the “slow” output of the VDAC pin. If a dynamic VID step down is detected, the body brake latch is set and the output of the error amplifier is pulled down to 75% of the DAC voltage by the VID body brake clamp. This triggers the Body Braking™ function in the phase ICs causing them to turn off both their drivers.

The converter’s output voltage needs to be monitored and compared to the VDAC voltage to determine when to resume normal operation. Unfortunately, the voltage on the FB pin can be pulled down by its compensation network during the sudden decrease in the Error Amp’s output voltage so an additional pin BBFB is provided. The BBFB pin is connected to the converter output voltage and VDRP pin with resistors of the same value as on the FB pin and therefore provides an un-corrupted representation of converter output voltage. The regulation detect comparator compares the BBFB to the VDAC voltage and resets the body brake latch releasing the error amp’s output and allowing normal operation to resume. Body Braking™ during a transition to a lower VID code can be disabled by connecting the BBFB pin to ground.

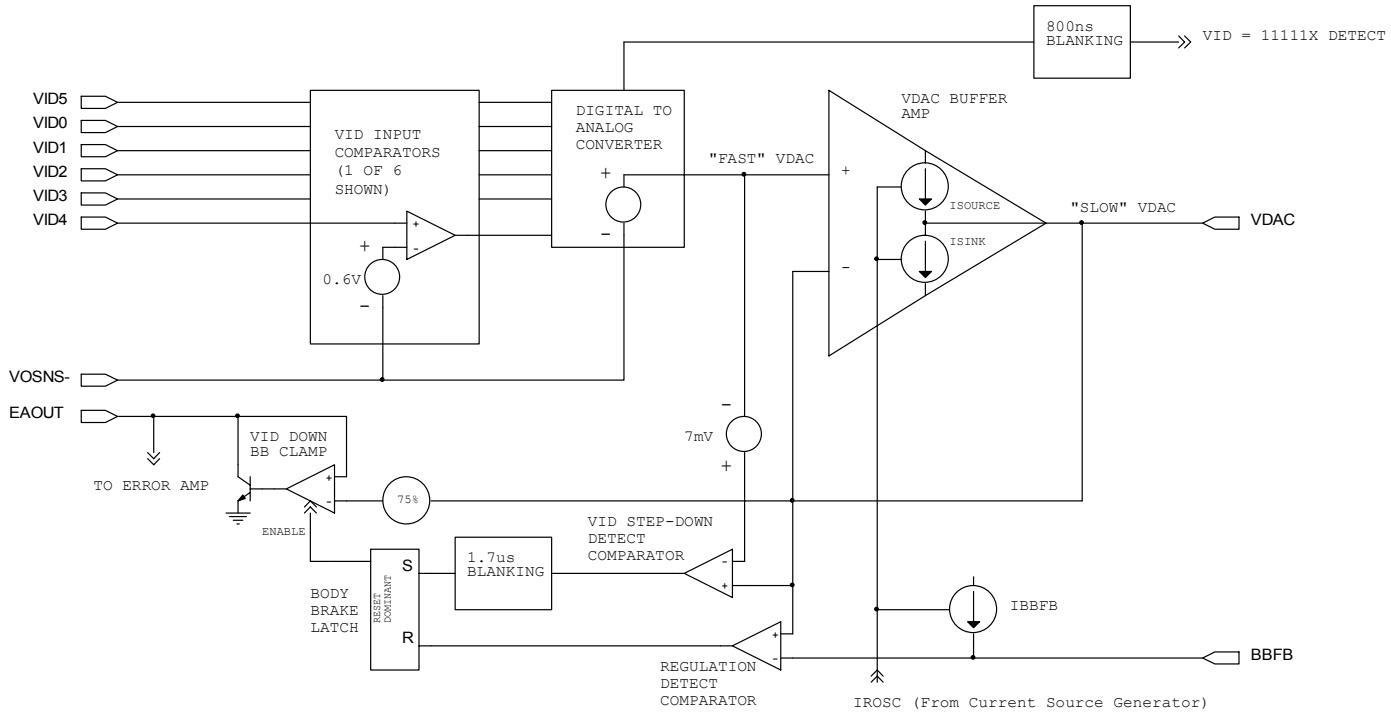


Figure 7– VID Control Block Diagram

Processor Pins (0 = low, 1 = high)						Vout (V)		Processor Pins (0 = low, 1 = high)						Vout (V)
VID4	VID3	VID2	VID1	VID0	VID5			VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375		1	1	0	1	0	0	1.2125
0	1	0	0	1	1	0.8500		1	1	0	0	1	1	1.2250
0	1	0	0	1	0	0.8625		1	1	0	0	1	0	1.2375
0	1	0	0	0	1	0.8750		1	1	0	0	0	1	1.2500
0	1	0	0	0	0	0.8875		1	1	0	0	0	0	1.2625
0	0	1	1	1	1	0.9000		1	0	1	1	1	1	1.2750
0	0	1	1	1	0	0.9125		1	0	1	1	1	0	1.2875
0	0	1	1	0	1	0.9250		1	0	1	1	0	1	1.3000
0	0	1	1	0	0	0.9375		1	0	1	1	0	0	1.3125
0	0	1	0	1	1	0.9500		1	0	1	0	1	1	1.3250
0	0	1	0	1	0	0.9625		1	0	1	0	1	0	1.3375
0	0	1	0	0	1	0.9750		1	0	1	0	0	1	1.3500
0	0	1	0	0	0	0.9875		1	0	1	0	0	0	1.3625
0	0	0	1	1	1	1.0000		1	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.0125		1	0	0	1	1	0	1.3875
0	0	0	1	0	1	1.0250		1	0	0	1	0	1	1.4000
0	0	0	1	0	0	1.0375		1	0	0	1	0	0	1.4125
0	0	0	0	1	1	1.0500		1	0	0	0	1	1	1.4250
0	0	0	0	1	0	1.0625		1	0	0	0	1	0	1.4375
0	0	0	0	0	1	1.0750		1	0	0	0	0	1	1.4500
0	0	0	0	0	0	1.0875		1	0	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[4]		0	1	1	1	1	1	1.4750
1	1	1	1	1	0	OFF[4]		0	1	1	1	1	0	1.4875
1	1	1	1	0	1	1.1000		0	1	1	1	0	1	1.5000
1	1	1	1	0	0	1.1125		0	1	1	1	0	0	1.5125
1	1	1	0	1	1	1.1250		0	1	1	0	1	1	1.5250
1	1	1	0	1	0	1.1375		0	1	1	0	1	0	1.5375
1	1	1	0	0	1	1.1500		0	1	1	0	0	1	1.5500
1	1	1	0	0	0	1.1625		0	1	1	0	0	0	1.5625
1	1	0	1	1	1	1.1750		0	1	0	1	1	1	1.5750
1	1	0	1	1	0	1.1875		0	1	0	1	1	0	1.5875
1	1	0	1	0	1	1.2000		0	1	0	1	0	1	1.6000

Note: 3. Output disabled (Fault mode)

Table 1 - Voltage Identification (VID)

Adaptive Voltage Positioning

Adaptive voltage positioning is needed to reduce the output voltage deviations during load transients and the power dissipation of the load when it is drawing maximum current. The circuitry related to voltage positioning is shown in Figure 8. Resistor R_{FB} is connected between the Error Amp's inverting input pin FB and the converter's output voltage. An internal current source whose value is programmed by the same external resistor that programs the oscillator frequency pumps current into the FB pin. The error amp forces the converter's output voltage lower to maintain a balance at its inputs. R_{FB} is selected to program the desired amount of fixed offset voltage below the DAC voltage.

The voltage at the VDRP pin is a buffered version of the share bus and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor RDRP. Since the Error Amp will force the loop to maintain FB to be equal to the VDAC reference voltage, a current will be flow into the FB pin equal to (VDRP-VDAC) / R_{DRP}. When the load current increases, the adaptive positioning voltage increases accordingly. More current flows through the feedback resistor R_{FB}, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor R_{DRP} so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

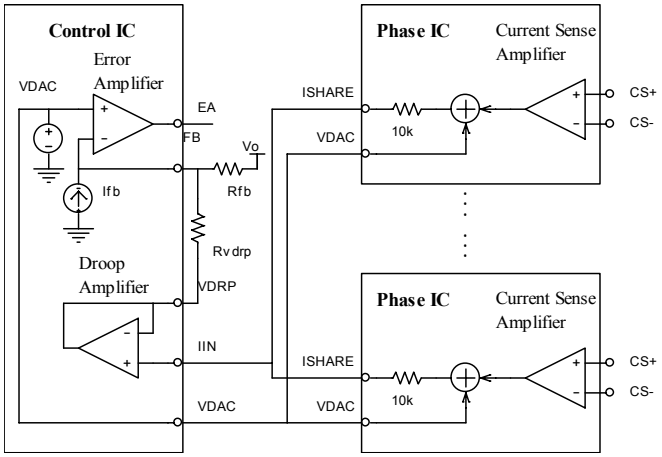


Figure 8 - Adaptive voltage positioning

Inductor DCR Temperature Correction

If the thermal compensation of the inductor DCR provided by the temperature dependent gain of the current sense amplifier is not adequate, a negative temperature coefficient (NTC) thermistor can be used for additional correction. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 9. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor. A similar network must be placed on the BBFB to ensure proper operation during a transition to a lower VID code with Body Braking™.

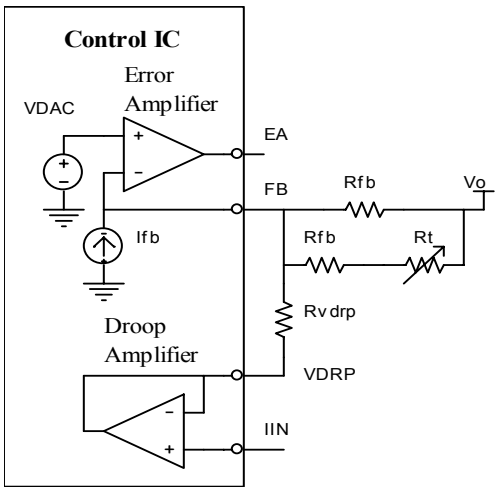


Figure 9 - Temperature compensation of inductor DCR

Remote Voltage Sensing

To compensate for impedance in the ground plane, the VOSNS- pin is used for remote sensing and connects directly to the load. The VDAC voltage is referenced to VOSNS- to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VDAC and VOSNS- pins ensure that high speed transients are fed directly into the error amp without delay.

Soft Start, Over-Current Fault Delay, and Hiccup Mode

The IR3081 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start as well as over-current protection delay and hiccup mode timing. A charge current of 66uA and discharge current of 6uA control the up slope and down slope of the voltage at the SS/DEL pin respectively

Figure 11 depicts the various operating modes as controlled by the SS/DEL function. If there is no fault, the SS/DEL pin will begin to be charged. The error amplifier output is clamped low until SS/DEL reaches 1.3V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.3V offset until it reaches the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.91V and allows the PWRGD signal to be asserted. SS/DEL finally settles at 4V, indicating the end of the soft start.

Under Voltage Lock Out and VID=11111x faults as well as a low signal on the ENABLE input immediately sets the fault latch causing SS/DEL to begin to discharge. The SS/DEL capacitor will continue to discharge down to 0.2V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

A delay is included if an over-current condition occurs after a successful soft start sequence. This is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation it will initiate the discharge of the capacitor at SS/DEL but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 90mV offset of the delay comparator, the Fault latch will be set pulling the error amp's output low inhibiting switching in the phase ICs and de-asserting the PWRGD signal. The delay can be reduced by adding a resistor in series with the delay capacitor. The delay comparator's offset voltage is reduced by the drop in the resistor caused by the discharge current. To prevent the charge current from creating an offset exceeding the SS/DEL to FB input offset voltage the value of the resistor should be 10KΩ or less to avoid interference with the soft start function.

The SS/DEL capacitor will continue to discharge until it reaches 0.2V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the 11 to 1 charge to discharge ratio results in a 9% hiccup mode duty cycle regardless of at what point the over-current condition occurs.

If SS/DEL pin is pulled below 0.9V, the converter can be disabled.

Under Voltage Lockout (UVLO)

The UVLO function monitors the IR3081's VCC supply pin and ensures that IR3081 has a high enough voltage to power the internal circuit. The IR3081's UVLO is set higher than the minimum operating voltage of compatible Phase ICs thus providing UVLO protection for them as well. During power-up the fault latch is reset when VCC exceeds 9.1V and there is no other fault. If the VCC voltage drops below 8.9V the fault latch will be set. For converters using a separate 5V supply for gate driver bias an external UVLO circuit can be added to prevent operation until adequate voltage is present. A diode connected between the 5V supply and the SS/DEL pin provides a simple 5V UVLO function.

Over Current Protection (OCP)

The current limit threshold is set by a resistor connected between the OCSET and VDAC pins. If the IIN pin voltage, which is proportional to the average current plus DAC voltage, exceeds the OCSET voltage, the over-current protection is triggered.

VID = 11111X Fault

VID codes of 111111 and 111110 will set the fault latch and disable the error amplifier. An 800ns delay is provided to prevent a fault condition from occurring during Dynamic VID changes.

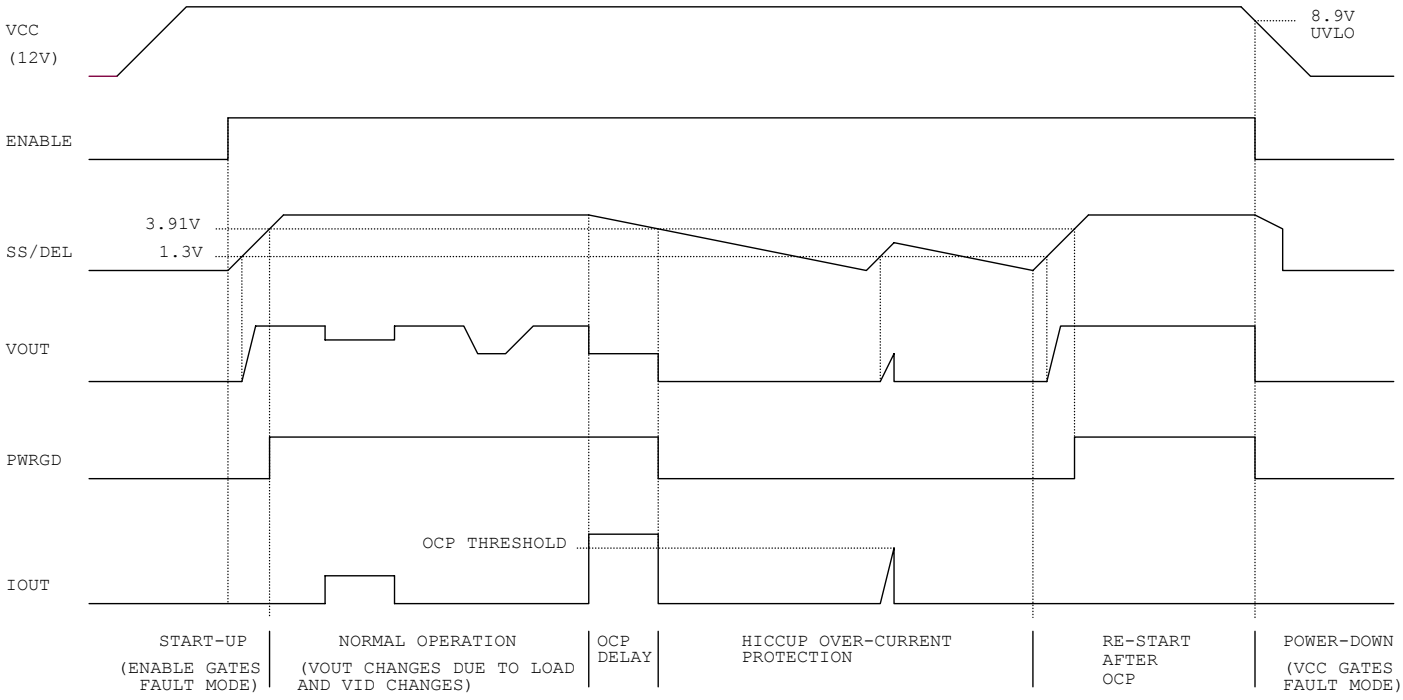


Figure 11 – Operating Waveforms

Power Good Output

The PWRGD pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PWRGD remains low until the output voltage is in regulation and SS/DEL is above 3.91V. The PWRGD pin becomes low if the fault latch is set. A high level at the PWRGD pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

Load Current Indicator Output

The IIN pin voltage represents the average current of the converter plus the DAC voltage. The load current can be retrieved by subtracting the VDAC voltage from the IIN voltage.

System Reference Voltage (VBIAS)

The IR3081 supplies a 6.8V/5mA precision reference voltage from the VBIAS pin. The oscillator ramp trip points are based on the VBIAS voltage so it should be used to program the Phase ICs phase delay to minimize phase errors.

Enable Input

Pulling the ENABLE pin below 0.6V sets the Fault Latch.

APPLICATIONS INFORMATION

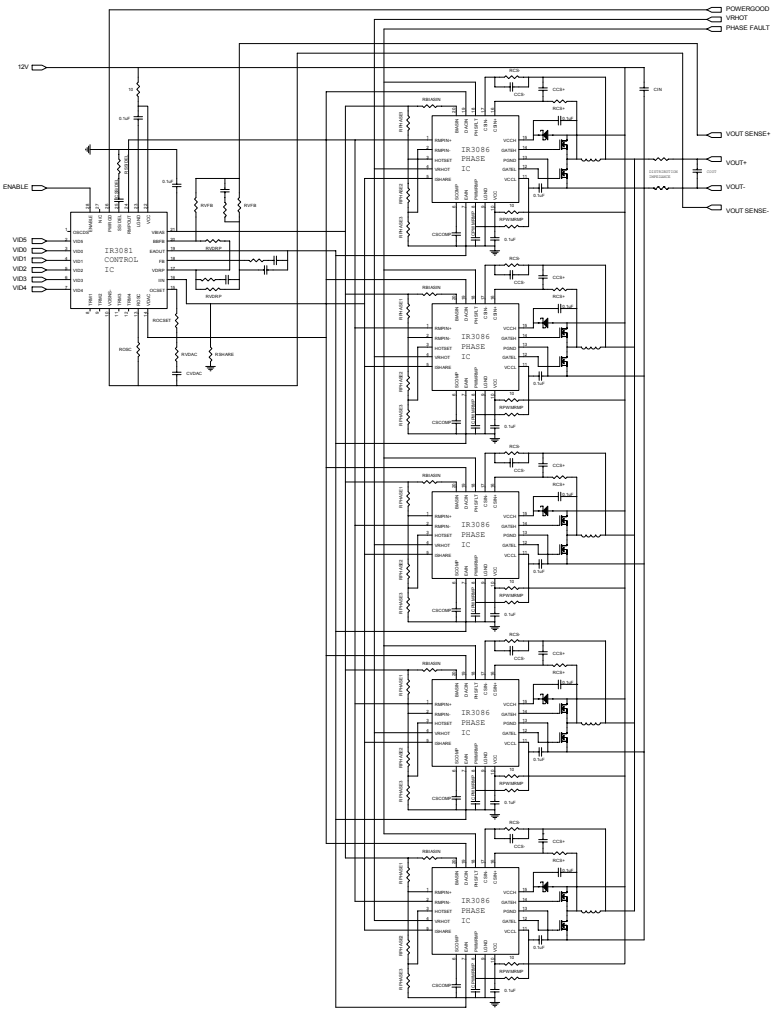


Figure 8 – IR3081/3086 5 Phase VRM/EVRD 10.0 Converter

LAYOUT GUIDELINES

The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane, which is then split into signal ground plane (LGND) and power ground plane (PGND).
- Connect the ground tab under the control IC to LGND plane through vias. Place the resistor ROSC as close as possible to ROSC pin of the control IC, and place the over-current limit resistor ROCSET as close as possible to OCSET and VDAC pins of the control IC.
- Bus signals should not cross over the fast transition nodes, such as switching nodes and gate drive output.
- Use Kelvin connections for the current sense signals, and use the ground plane to shield the current sense traces.
- Use Kelvin connections for the remote voltage sense signals, and avoid crossing over the fast transition nodes.

PERFORMANCE CHARACTERISTICS

Figure 13 - Oscillator Frequency versus ROSC

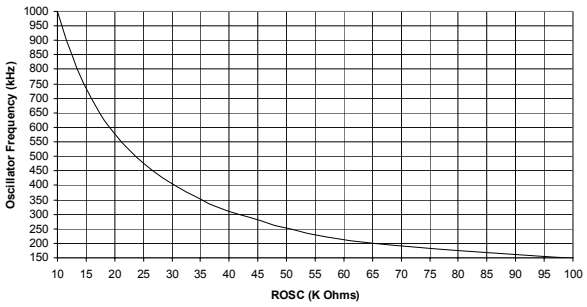


Figure 14 - IFB, BBFB, & OCSET Bias Currents vs ROSC

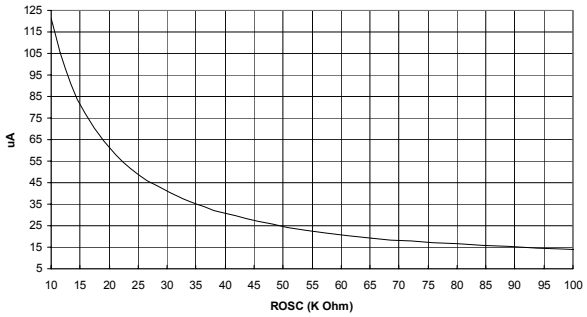


Figure 15 - VDAC Source & Sink Currents vc ROSC (includes OCSET Bias Current)

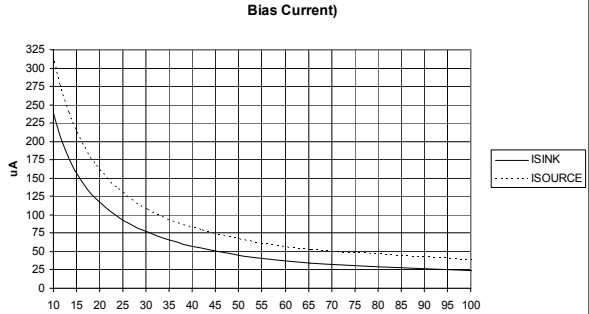
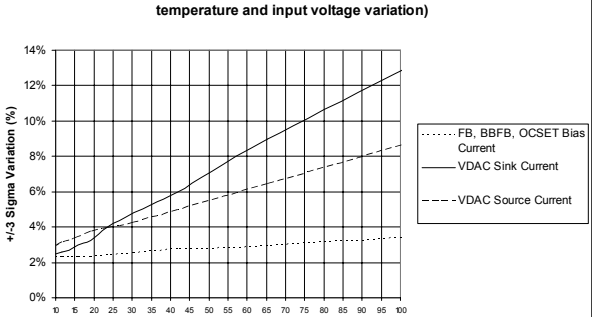
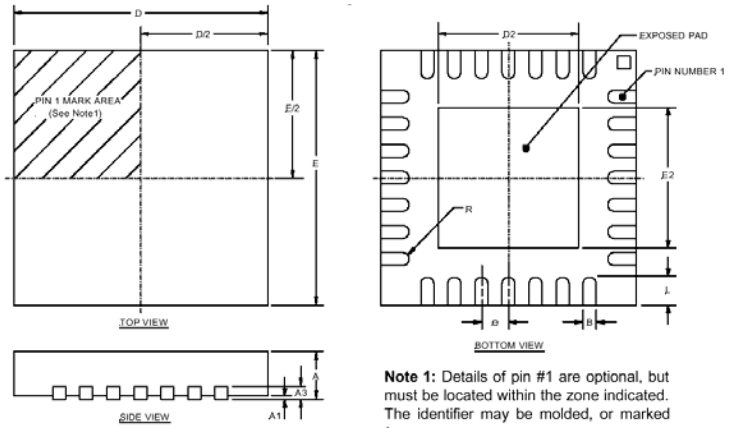


Figure 16 - Bias Current Accuracy versus ROsC (includes temperature and input voltage variation)



PACKAGE INFORMATION

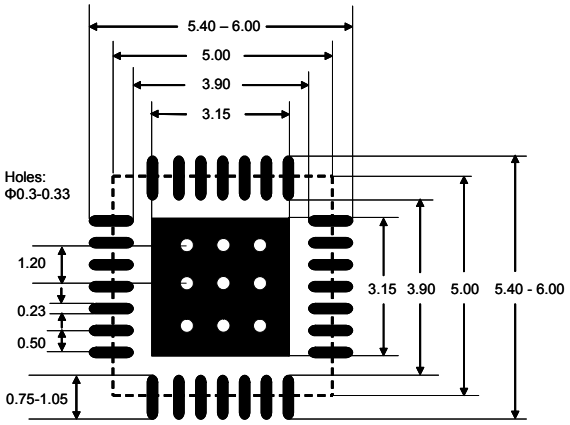
28L MLPQ (5 x 5 mm Body) – θ_{JA} = 30°C/W, θ_{JC} = 3°C/W



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL	28-PIN 5x5		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		5.00 BSC	
D2	3.00	3.15	3.25
E		5.00 BSC	
E2	3.00	3.15	3.25
e		0.50 BSC	
L	0.45	0.55	0.65
R	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.



Note: All dimensions are in Millimeters.

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