

Bulletin I27401 rev. A 09/97

International IOR Rectifier

IRK.500.. SERIES

THYRISTOR / DIODE and
THYRISTOR / THYRISTOR

SUPER MAGN-A-pak™ Power Modules

Features

- High current capability
- 3000 V_{RMS} isolating voltage with non-toxic substrate
- High surge capability
- Industrial standard package
- UL E78996 approved 

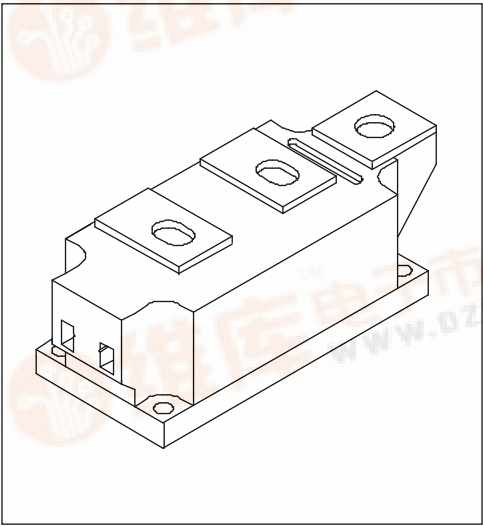
500 A

Typical Applications

- Motor starters
- DC motor controls - AC motor controls
- Uninterruptable power supplies

Major Ratings and Characteristics

Parameters	IRK.500..	Units
$I_{T(AV)}$ or $I_{F(AV)}$	500	A
@ T_C	82	°C
$I_{T(RMS)}$	785	A
@ T_C	82	°C
I_{TSM} or I_{FSM} @ 50Hz	17.8	KA
@ 60Hz	18.7	KA
I^2t @ 50Hz	1591	KA ² s
@ 60Hz	1452	KA ² s
$I^2\sqrt{t}$	15910	KA ² √s
V_{DRM}/V_{RRM} range	800 to 1600	V
T_{STG} range	-40 to 150	°C
T_J range	-40 to 130	°C



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ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{RRM}/V_{DRM} , maximum repetitive peak reverse voltage V	V_{RSM} , maximum non-repetitive peak rev. voltage V	I_{RRM}/I_{DRM} max. @ $T_J = T_J$ max. mA
IRK.500..	08	800	900	100
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

On-state Conduction

Parameter	IRK.500..	Units	Conditions
$I_{T(AV)}$ Maximum average on-state current	500	A	180° conduction, half sine wave
$I_{F(AV)}$ @ Case temperature	82	°C	
$I_{T(RMS)}$ Maximum RMS on-state current	785	A	180° conduction, half sine wave @ $T_C = 82^\circ\text{C}$
I_{TSM} Maximum peak, one-cycle, non-repetitive surge current	17.8	KA	t = 10ms No voltage
I_{FSM}	18.7		t = 8.3ms reapplied
	15.0		t = 10ms 100% V_{RRM}
	15.7		t = 8.3ms reapplied
I^2t Maximum I^2t for fusing	1591	KA²s	t = 10ms No voltage
	1452		t = 8.3ms reapplied
	1125		t = 10ms 100% V_{RRM}
	1027		t = 8.3ms reapplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	15910	KA²/s	t = 0.1 to 10ms, no voltage reapplied
$V_{T(TO)1}$ Low level value of threshold voltage	0.85	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}), T_J = T_J$ max.
$V_{T(TO)2}$ High level value of threshold voltage	0.93		$(I > \pi \times I_{T(AV)}), T_J = T_J$ max.
r_{t1} Low level value of on-state slope resistance	0.36	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}), T_J = T_J$ max.
r_{t2} High level value of on-state slope resistance	0.32		$(I > \pi \times I_{T(AV)}), T_J = T_J$ max.
V_{TM} Maximum on-state or forward voltage drop	1.50	V	$I_{pk} = 1500\text{A}, T_J = 25^\circ\text{C}, t_p = 10\text{ms}$ sine pulse
I_H Maximum holding current	500	mA	$T_J = 25^\circ\text{C}$, anode supply 12V resistive load
I_L Typical latching current	1000		

Switching

Parameter	IRK.500..	Units	Conditions
di/dt Maximum rate of rise of turned-on current	1000	A/μs	$T_J = T_J$ max., $I_{TM} = 400\text{A}$, V_{DRM} applied
t_d Typical delay time	2.0	μs	Gate current 1A, $di_g/dt = 1\text{A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$, $T_J = 25^\circ\text{C}$
t_q Typical turn-off time	200	μs	$I_{TM} = 750\text{A}, T_J = T_J$ max, $di/dt = -60\text{A}/\mu\text{s}$, $V_R = 50\text{V}$, $dv/dt = 20\text{V}/\mu\text{s}$, Gate 0 V 100Ω

Blocking

Parameter	IRK.500..	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	1000	V/ μ s	$T_J = 130^\circ\text{C}$., linear to $V_D = 80\% V_{DRM}$
V_{INS} RMS isolation voltage	3000	V	$t = 1 \text{ s}$
I_{RRM} Maximum peak reverse and off-state leakage current I_{DRM}	100	mA	$T_J = T_J \text{ max.}$, rated V_{DRM}/V_{RRM} applied

Triggering

Parameter	IRK.500..	Units	Conditions
P_{GM} Maximum peak gate power	10	W	$T_J = T_J \text{ max.}$, $t_p \leq 5 \text{ ms}$
$P_{G(AV)}$ Maximum peak average gate power	2.0	W	$T_J = T_J \text{ max.}$, $f = 50 \text{ Hz}$, $d\% = 50$
$+I_{GM}$ Maximum peak positive gate current	3.0	A	$T_J = T_J \text{ max.}$, $t_p \leq 5 \text{ ms}$
$+V_{GM}$ Maximum peak positive gate voltage	20	V	
$-V_{GM}$ Maximum peak negative gate voltage	5.0	V	
I_{GT} Max. DC gate current required to trigger	200	mA	$T_J = 25^\circ\text{C}$ $V_{ak} 12 \text{ V}$
V_{GT} DC gate voltage required to trigger	3.0	V	$T_J = 25^\circ\text{C}$ $V_{ak} 12 \text{ V}$
I_{GD} DC gate current not to trigger	10	mA	$T_J = T_J \text{ max.}$
V_{GD} DC gate voltage not to trigger	0.25	V	

Thermal and Mechanical Specifications

Parameter	IRK.500..	Units	Conditions
T_J Max. junction operating temperature range	- 40 to 130	$^\circ\text{C}$	
T_{stg} Max. storage temperature range	- 40 to 150		
R_{thJC} Max. thermal resistance, junction to case	0.065	K/W	Per junction, DC operation
R_{thCHS} Max. thermal resistance, case to heatsink	0.02	K/W	
T Mounting torque $\pm 10\%$ SMAP to heatsink busbar to SMAP	6 - 8	Nm	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound
	12 - 15		
wt Approximate weight	1500	g	
Case style	SUPER MAGN-A-pak		See outline table

IRK.500.. Series

Bulletin I27401 rev. A 09/97

ΔR_{thJC} Conduction

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.009	0.006	K/W	$T_J = T_{J \text{ max.}}$
120°	0.011	0.011		
90°	0.014	0.015		
60°	0.021	0.022		
30°	0.037	0.038		

Ordering Information Table

Device Code

IRK

T

500

-

16

1

2

3

4

1

 - Module type

2

 - Circuit configuration (See Circuit Configurations Table)

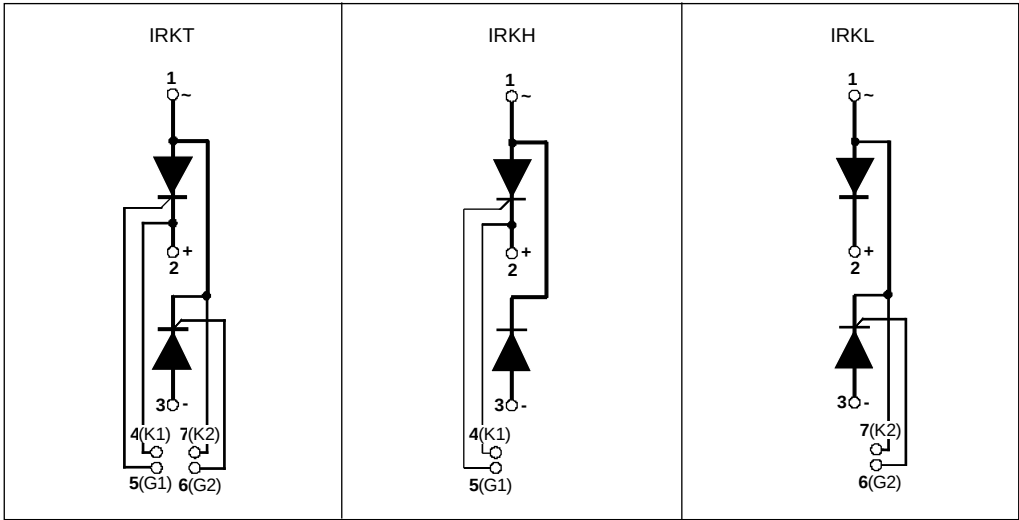
3

 - Current rating

4

 - Voltage code: Code x 100 = V_{RRM} (See Voltage Ratings Table)

Circuit Configurations Table



NOTE: To order the Optional Hardware see Bulletin I27900

Outline Table

All dimensions in millimeters (inches)

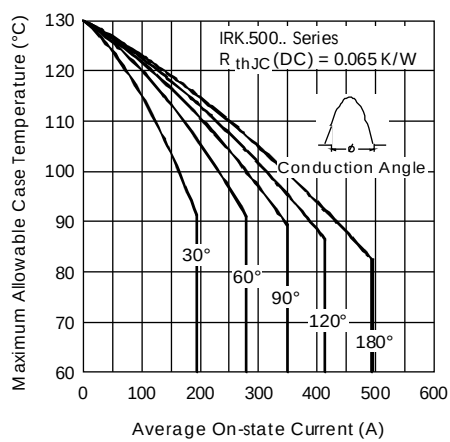
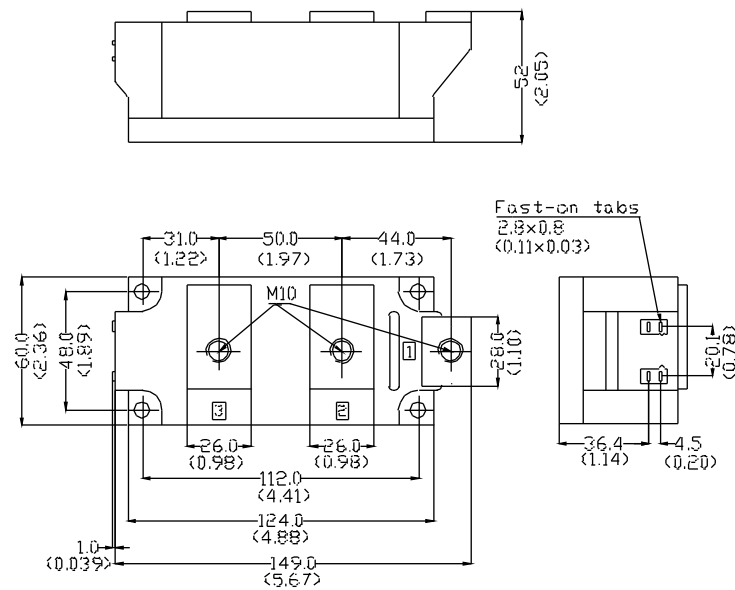


Fig. 1 - Current Ratings Characteristics

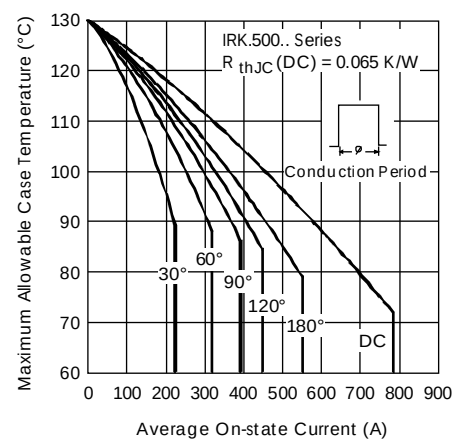


Fig. 2 - Current Ratings Characteristics

IRK.500.. Series

Bulletin I27401 rev. A 09/97

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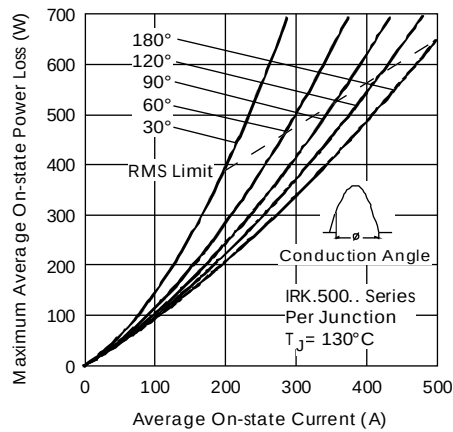


Fig. 3 - On-state Power Loss Characteristics

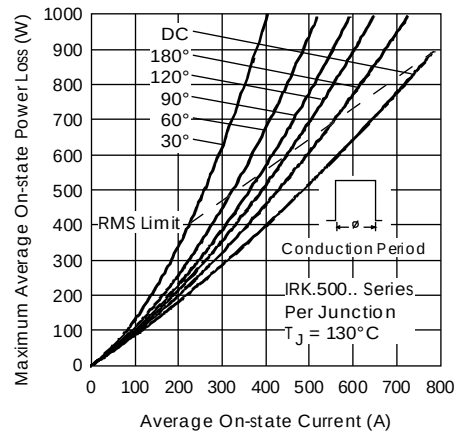


Fig. 4 - On-state Power Loss Characteristics

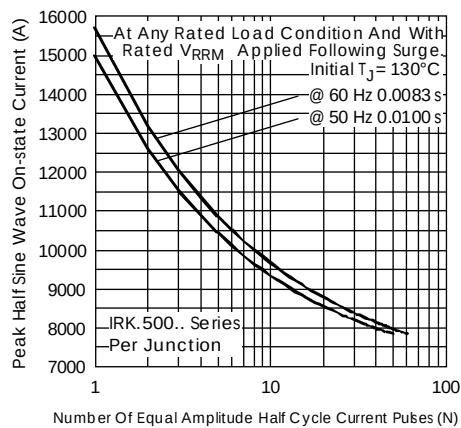


Fig. 5 - Maximum Non-Repetitive Surge Current

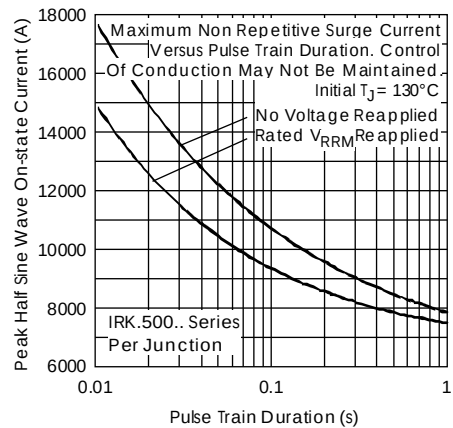


Fig. 6 - Maximum Non-Repetitive Surge Current

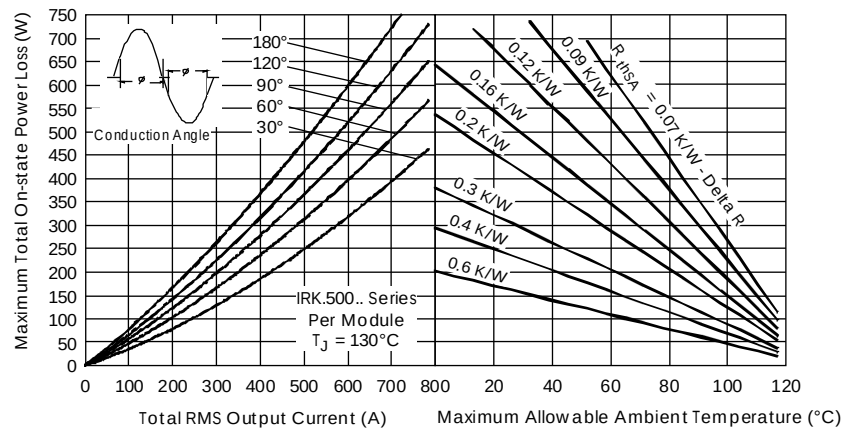


Fig. 7 - On-state Power Loss Characteristics

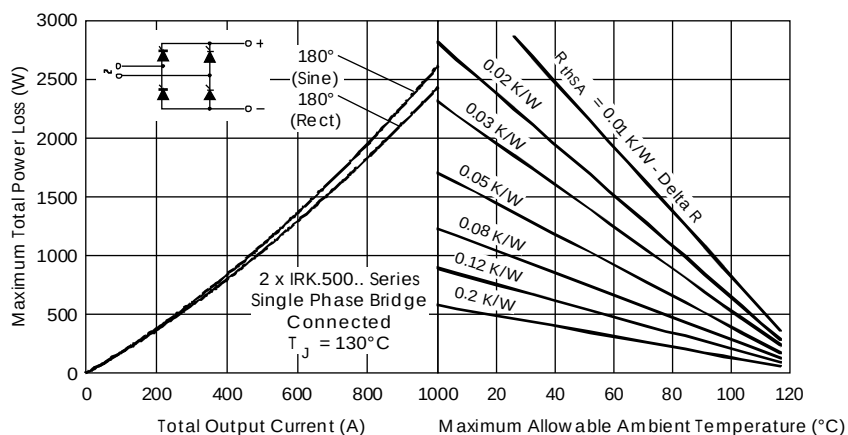


Fig. 8 - On-state Power Loss Characteristics

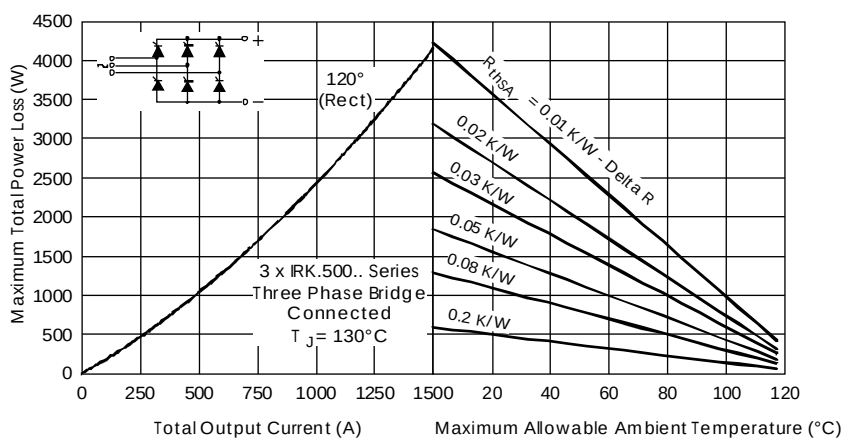


Fig. 9 - On-state Power Loss Characteristics

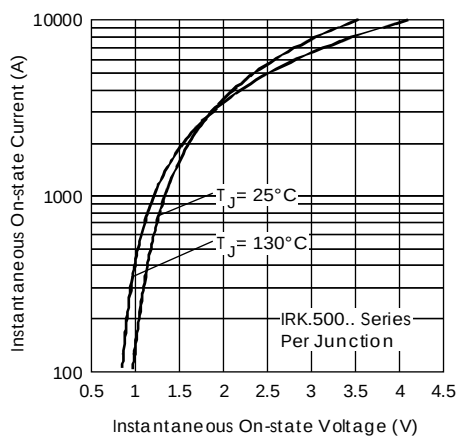


Fig. 10 - On-state Voltage Drop Characteristics

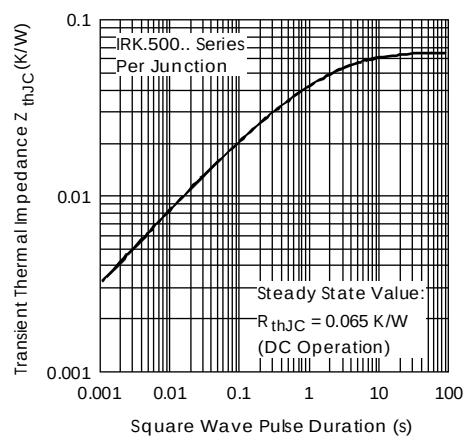


Fig. 11 - Thermal Impedance $Z_{\theta JC}$ Characteristics

IRK.500.. Series

Bulletin I27401 rev. A 09/97

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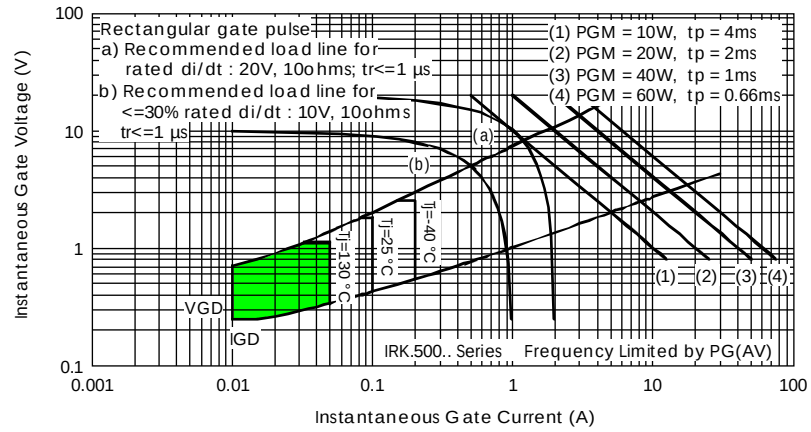


Fig. 12 - Gate Characteristics