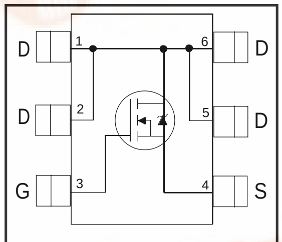
International
IOR Rectifier

PD- 93758D

IRLMS2002

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- N-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 2.5V Rated



Top View

V_{DSS} = 20V

$R_{DS(on)}$ = 0.030Ω

Description

These N-Channel MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

The Micro6™ package with its customized leadframe produces a HEXFET® power MOSFET with $R_{DS(on)}$ 60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and $R_{DS(on)}$ reduction enables a current-handling increase of nearly 300% compared to the SOT-23.

Micro6™

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	6.5	A
I_D @ T_A= 70°C	Continuous Drain Current, V_{GS} @ 4.5V	5.2	
I_{DM}	Pulsed Drain Current ①	20	
P_D @T_A = 25°C	Power Dissipation	2.0	W
P_D @T_A = 70°C	Power Dissipation	1.3	
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

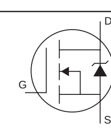
	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	62.5	°C/W

01/13/03

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.016	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.030	Ω	V_{GS} = 4.5V, I_D = 6.5A ②
		——	——	0.045		V_{GS} = 2.5V, I_D = 5.2A ②
$V_{GS(th)}$	Gate Threshold Voltage	0.60	——	1.2	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	13	——	——	S	V_{DS} = 10V, I_D = 6.5A
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	µA	V_{DS} = 16V, V_{GS} = 0V
		——	——	25		V_{DS} = 16V, V_{GS} = 0V, T_J = 70°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	-100	nA	V_{GS} = -12V
	Gate-to-Source Reverse Leakage	——	——	100		V_{GS} = 12V
Q_g	Total Gate Charge	——	15	22	nC	I_D = 6.5A
Q_{gs}	Gate-to-Source Charge	——	2.2	3.3		V_{DS} = 10V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	3.5	5.3		V_{GS} = 5.0V ②
$t_{d(on)}$	Turn-On Delay Time	——	8.5	——	ns	V_{DD} = 10V
t_r	Rise Time	——	11	——		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	——	36	——		R_G = 6.0Ω
t_f	Fall Time	——	16	——		R_D = 10Ω ②
C_{iss}	Input Capacitance	——	1310	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	150	——		V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	——	36	——		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	20		
V_{SD}	Diode Forward Voltage	——	——	1.2	V	T_J = 25°C, I_S = 1.7A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	——	19	29	ns	T_J = 25°C, I_F = 1.7A
Q_{rr}	Reverse Recovery Charge	——	13	20	nC	di/dt = 100A/µs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ Surface mounted on FR-4 board, t ≤ 5sec.

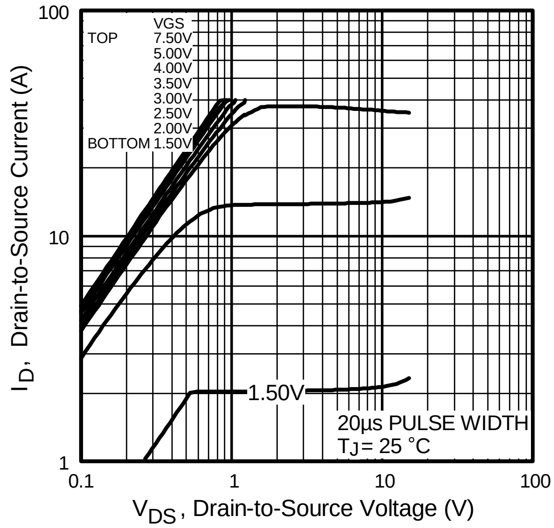


Fig 1. Typical Output Characteristics

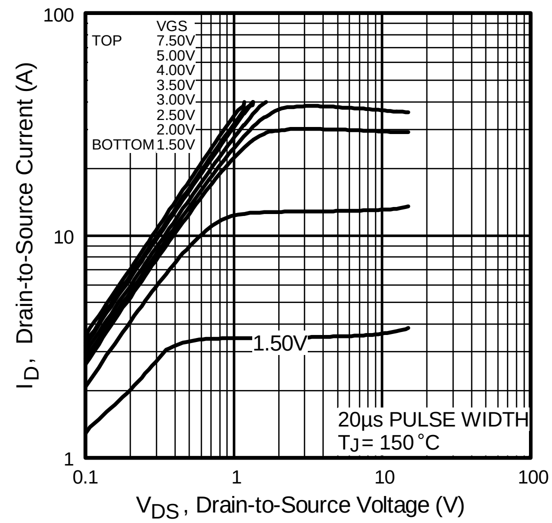


Fig 2. Typical Output Characteristics

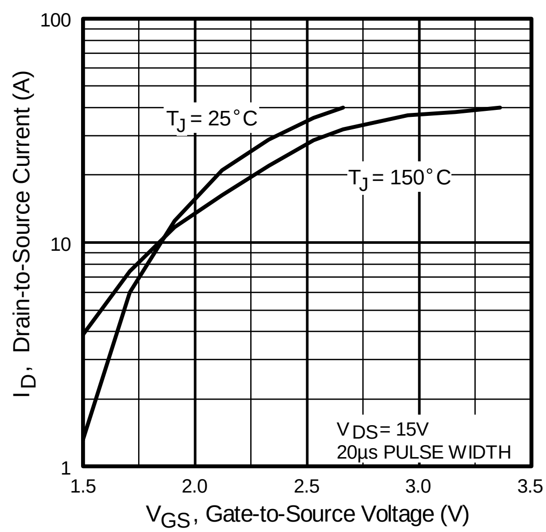


Fig 3. Typical Transfer Characteristics

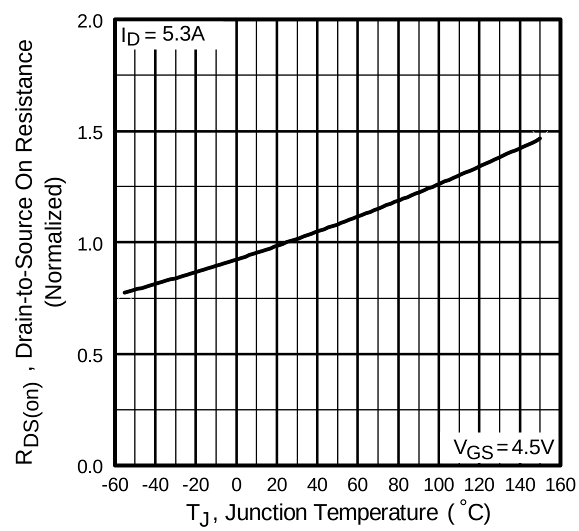


Fig 4. Normalized On-Resistance
Vs. Temperature

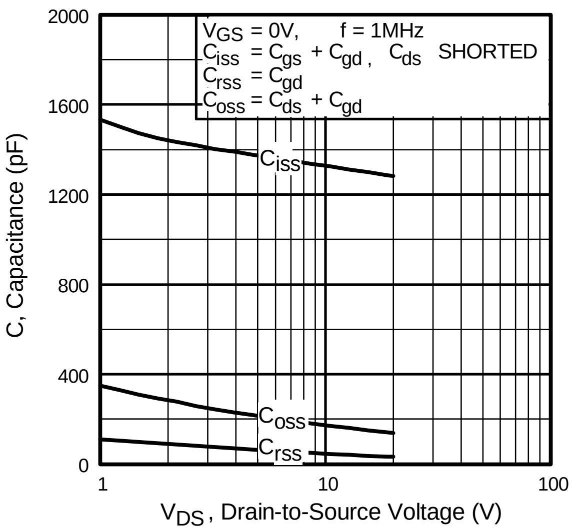


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

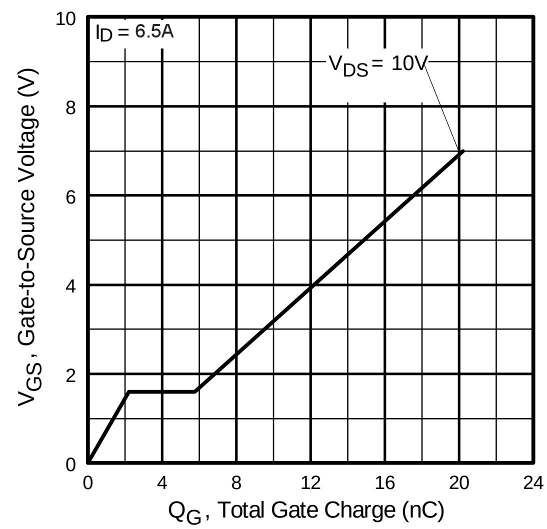


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

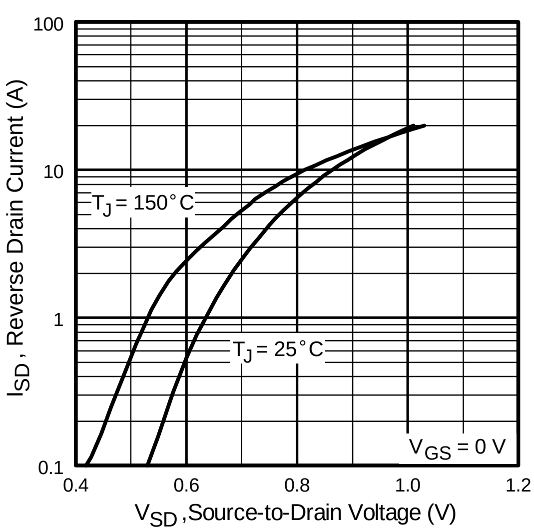


Fig 7. Typical Source-Drain Diode Forward Voltage

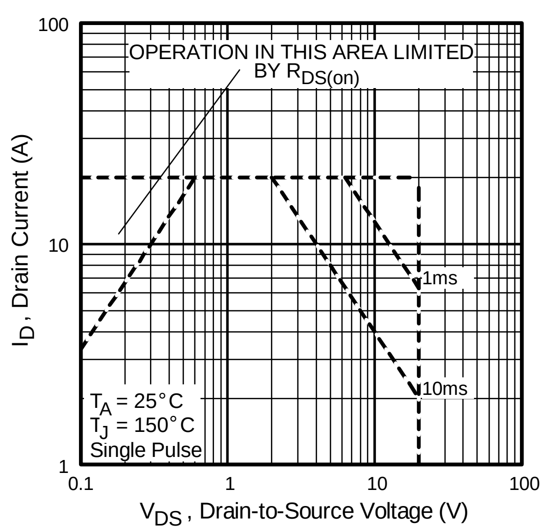


Fig 8. Maximum Safe Operating Area

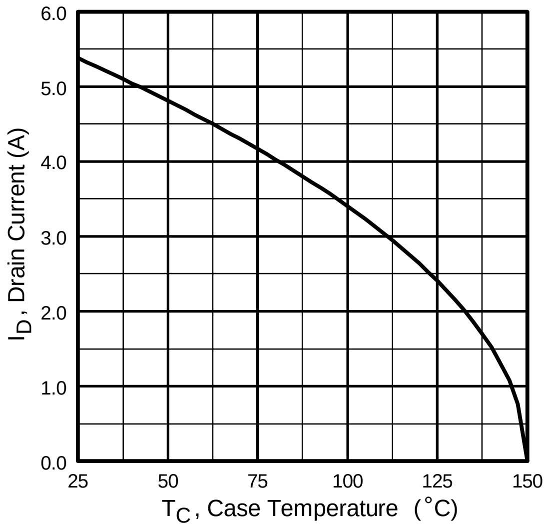


Fig 9. Maximum Drain Current Vs. Case Temperature

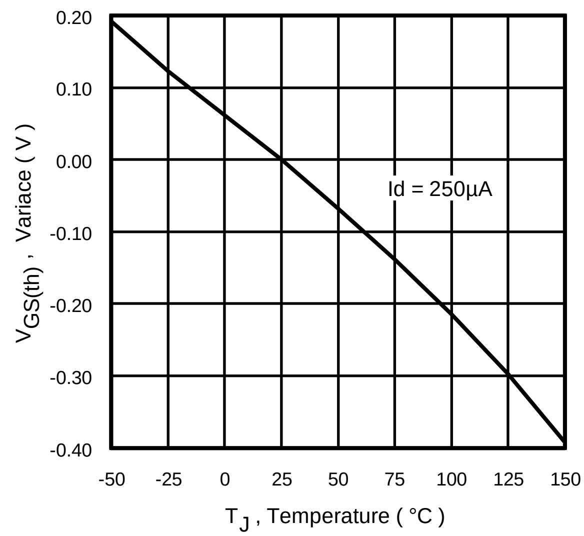


Fig 10. Typical Vgs(th) Variance Vs. Juction Temperature

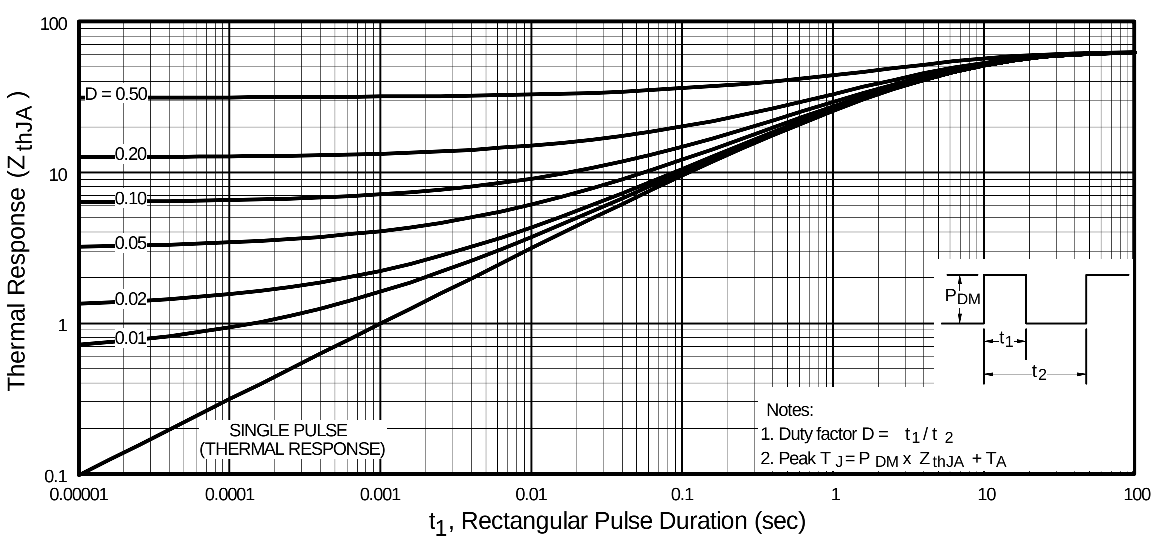


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

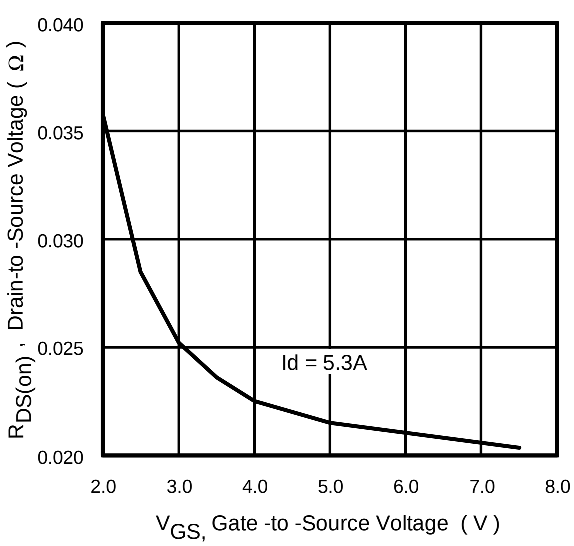


Fig 12. Typical On-Resistance Vs. Gate Voltage

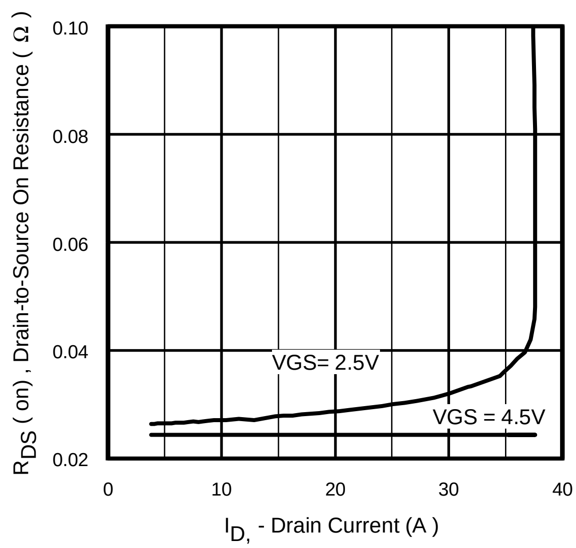
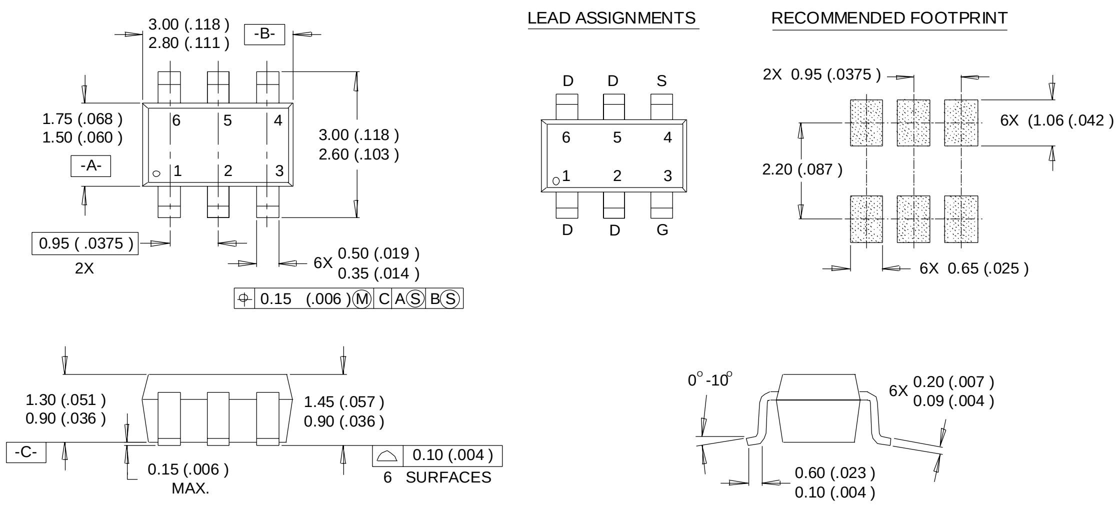


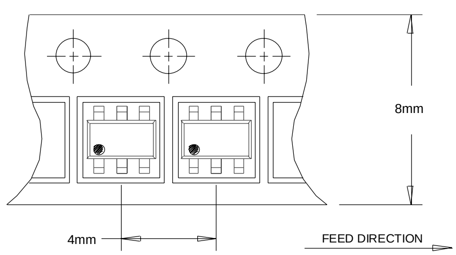
Fig 13. Typical On-Resistance Vs. Drain Current

Micro6™ Package Outline

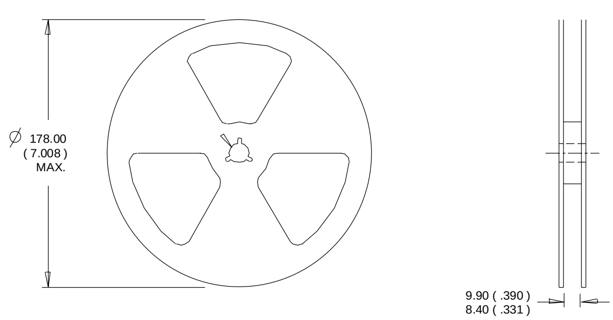


NOTES :
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Micro6™ Tape & Reel Information



NOTES :
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

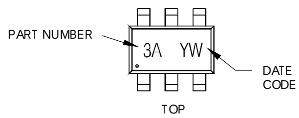


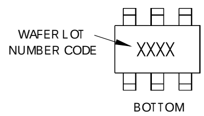
NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Micro6™ Part Marking Information

Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRLMS6702





PART NUMBER CODE REFERENCE:

2A = IRLMS1902
2B = IRLMS1503
2C = IRLMS6702
2D = IRLMS5703
2E = IRLMS6802
2F = IRLMS4502
2G = IRLMS2002
2H = IRLMS6803

DATE CODE EXAMPLES:

YWW = 9603 = 6C
YWW = 9632 = FF

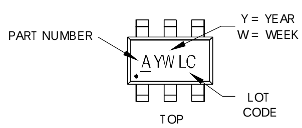
WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6	↓	↓
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

WW = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F	↓	↓
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

Notes: This part marking information applies to devices produced after 02/26/2001



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W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6	↓	↓
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F	↓	↓
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

This product has been designed and qualified for the consumer market.
Qualification Standards can be found on IR's Web site.

International
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