# IRU1237SC

## THREE INTEGRATED, FIXED OUTPUT LINEAR VOLTAGE REGULATORS

**PRELIMINARY DATA SHEET**

## FEATURES

- **Stable with Ceramic Capacitor**
- Fixed 8V, 3.3V and 2.6V
- Fast Transient Response
- Output Current Limiting for each outputs
- Built-In Thermal Shutdown

## APPLICATIONS

- Hard Disk Drive
- Multi-Outputs Applications
- High Efficiency Linear Regulator

## DESCRIPTION

The IRU1237SC voltage regulator solution contains three integrated, fixed, linear voltage regulators in one 7-pin surface mount package. The first is a 2.6V regulator to power the read channel and integrated controller/µP. The second is a 3.3V regulator to power the controller I/O and memory chips requiring 3.3V. The last is an 8V regulator to power the preamp chip. The bandgap reference, the 8V ground, and the substrate are all tied to a common ground pin, while the 2.6V and 3.3V ground is tied to a separate ground pin. This grounding scheme allows for improved noise isolation between the 8V regulator and the 2.6V and 3.3V regulators.

The 2.6V and 3.3V regulators shall each be capable of 1.2A continuous for a 5.25V input. The 8V regulator shall be capable of 0.2A continuous for a 13.2V input.

## TYPICAL APPLICATION

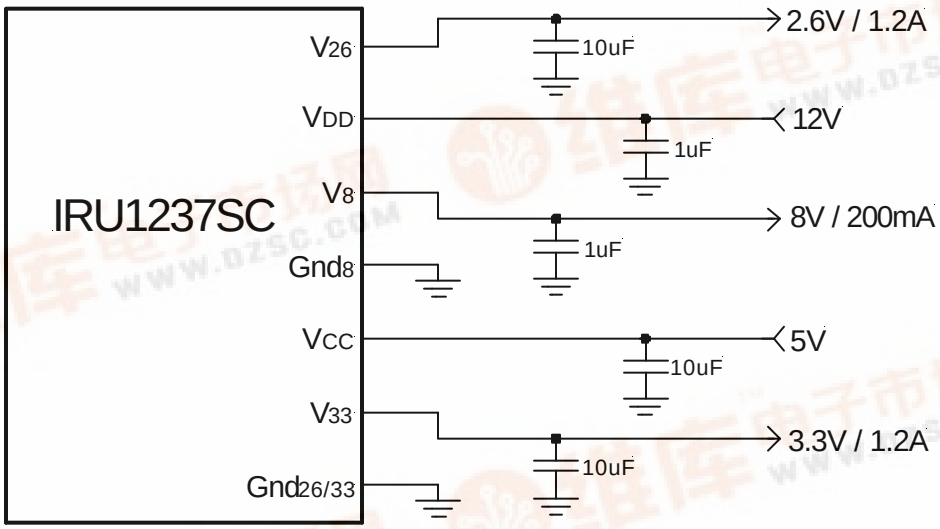



Figure 1 - Typical application of IRU1237SC.

## PACKAGE ORDER INFORMATION

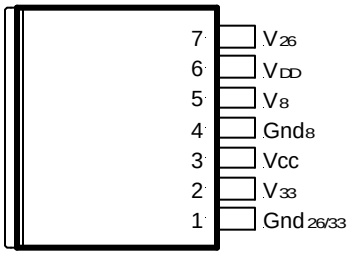
| TJ (°C) | 7-PIN PLASTIC Ultra Thin-Pak™ (P) | PACKAGE MARKING |
|---|---|---|
| 0 To 150 | IRU1237SCCP | US1237SCCP |

## ABSOLUTE MAXIMUM RATINGS

Input Voltage ($V_{CC}$) ..... 18V
Input Voltage ($V_{DD}$) ..... 18V
Operating Junction Temperature Range ..... 0°C To 150°C
Operating Ambient Temperature Range ..... 0°C To 70°C
Storage Temperature Range ..... -65°C To +150°C
ESD Capability (Human Body Model) ..... 2000V

## PACKAGE INFORMATION

7-PIN ULTRA THIN-PAK™ (P)




$\theta_{JA}$=30°C/W for 1"sq pad

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over $V_{CC}$=5V, $V_{DD}$=12V, $C_{IN}$=$C_{OUT}$=0.1µF(X7R), $T_J$=0 to 125°C. Typical values refer to $T_J$=25°C. $I_{FL1}$=1.2A, $I_{FL2}$ =1.2A and $I_{FL3}$ =0.2A.

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Voltage #1 | $V_{O1}$ | Over all operating conditions | 2.522 | 2.60 | 2.678 | V |
| Output Voltage #1 | $V_{O1}$ | 0V<$V_{DD}$<10.8V, $I_{O1}$=0.5A | 2.20 | 2.60 | 2.65 | V |
| Output Voltage #2 | $V_{O2}$ | Over all operating conditions | 3.20 | 3.30 | 3.40 | V |
| Output Voltage #2 | $V_{O2}$ | 0V<$V_{DD}$<10.8V, $I_{O1}$=0.5A | 2.90 | 3.30 | 3.40 | V |
| Output Voltage #3 | $V_{O3}$ | Over all operating conditions | 7.76 | 8.00 | 8.24 | V |
| Line Regulation | $Reg_{LINE}$ | $I_O$=10mA, $V_{CC}$ ± 5%, $V_{DD}$ ± 10% | | 0.2 | | %Vo |
| Load Regulation | $Reg_{LOAD}$ | Note 1, 10mA < $I_O$ < $I_{FL}$ | | 0.4 | | %Vo |
| Dropout Voltage (Output #1) | $V_{DO1}$ | Note 2, $I_{O1}$=$I_{FL1}$ | | 1.3 | 1.7 | V |
| Dropout Voltage (Output #2) | $V_{DO2}$ | Note 2, $I_{O2}$=$I_{FL2}$ | | 1.1 | 1.3 | V |
| Dropout Voltage (Output #3) | $V_{DO3}$ | Note 3, $I_{O3}$=$I_{FL3}$ | | 2.0 | 2.2 | V |
| Transient Response | $t_{TR}$ | Note 3 and 7 | | 1.0 | | µs |
| Current Limit (Output #1) | $I_{OL1}$ | $\Delta V_{O1}$=125mV | 1.50 | 1.65 | 2.50 | A |
| Current Limit (Output #2) | $I_{OL2}$ | $\Delta V_{O2}$=165mV | 1.50 | 1.65 | 2.50 | A |
| Current Limit (Output #3) | $I_{OL3}$ | $\Delta V_{O3}$=400mV | 0.25 | 0.30 | 0.50 | A |
| Min Load Current (Output #1) | $L_{O1(MIN)}$ | Note 4 and 7 | | | 0 | mA |
| Min Load Current (Output #2) | $L_{O2(MAX)}$ | Note 4 and 7 | | | 0 | mA |
| Min Load Current (Output #3) | $L_{O3(MAX)}$ | Note 4 and 7 | | | 0 | mA |
| Output Capacitor | $C_O$ | Note 5 and 7 | 0.1 | | 33 | µF |
| Input Capacitor | $C_{IN}$ | Note 7 | 0.1 | | | µF |
| Thermal Regulation | $Reg_{THERM}$ | Note 7, 30ms pulse, $I_O$=$I_{FL}$ | | 0.1 | 0.3 | %/W |

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Ripple Rejection ($V_{CC}$ to Output #1) | $PSRR_1$ | Note 7, 100Hz<f<100KHz, $I_O=I_{FL1}/10$ | 30 | 40 | | dB |
| Ripple Rejection ($V_{CC}$ to Output #2) | $PSRR_2$ | Note 7, 100Hz<f<100KHz, $I_O=I_{FL2}/10$ | 30 | 40 | | dB |
| Ripple Rejection ($V_{DD}$ to Output #3) | $PSRR_3$ | Note 7, 100Hz<f<100KHz, $I_O=I_{FL3}/10$ | 40 | 50 | | dB |
| $T_J$ Thermal Shutdown | $T_{THERM}$ | Note 7 | | 150 | | °C |
| Temperature Stability | $Stab_{TEMP}$ | Note 6 and 7, $I_O$=10mA | | 0.5 | | %Vo |
| Long Term Stability | $Stab_{LONG}$ | Note 7, $T_J$=125°C, 1000Hrs | | 0.3 | | %Vo |
| RMS Output Noise | $V_N$ | Note 7, 10Hz<f<10KHz | | 0.003 | | %Vo |
| $V_{CC}$ Quiescent current | $I_{Q1}$ | $I_{O1}=I_{O2}=I_{O3}=0$ | | 4 | 8 | mA |
| $V_{DD}$ Quiescent current | $I_{Q2}$ | $I_{O1}=I_{O2}=I_{O3}=0$ | | 12 | 20 | mA |

**Note 1:** Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

**Note 2:** Dropout voltage is defined as the minimum differential voltage between $V_{IN}$ and $V_{OUT}$ required to maintain regulation at $V_{OUT}$. It is measured when the output voltage drops 1% below its nominal value.

**Note 3:** Transient response is defined with a step change in load from 10mA to $I_{FL}/2$, as the time from the load step until the output voltage reaches its minimum value.

**Note 4:** Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation.

**Note 5:** The regulator shall withstand 100,000 reverse bias discharges of the maximum output capacitance, with no degradation, when the input voltage is switched to ground in 1µs.

**Note 6:** Temperature stability is the change in output from nominal over the operating temperature range.

**Note 7:** Guaranteed by design, but not tested in production.

## PIN DESCRIPTIONS

| PIN# | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1,4 | $Gnd_{26/33}$, $Gnd_8$ | These pins are connected to ground. It is also the tab of the device. |
| 2 | $V_{33}$ | Output #1. Fixed regulator output (3.3V). |
| 3 | $V_{CC}$ | Positive unregulated supply input for the regulator. This pin must always be higher than both $V_{OUT}$ pins by the amount of the dropout voltage in order for the device to regulate properly. Bypass to ground with low ESR and ESL capacitance. |
| 5 | $V_8$ | Output #3. Fixed regulator output (8V). |
| 6 | $V_{DD}$ | Input voltage to supply the base current for the pass transistor for both regulators. |
| 7 | $V_{26}$ | Output #2. Fixed regulator output (2.6V). |

## BLOCK DIAGRAM

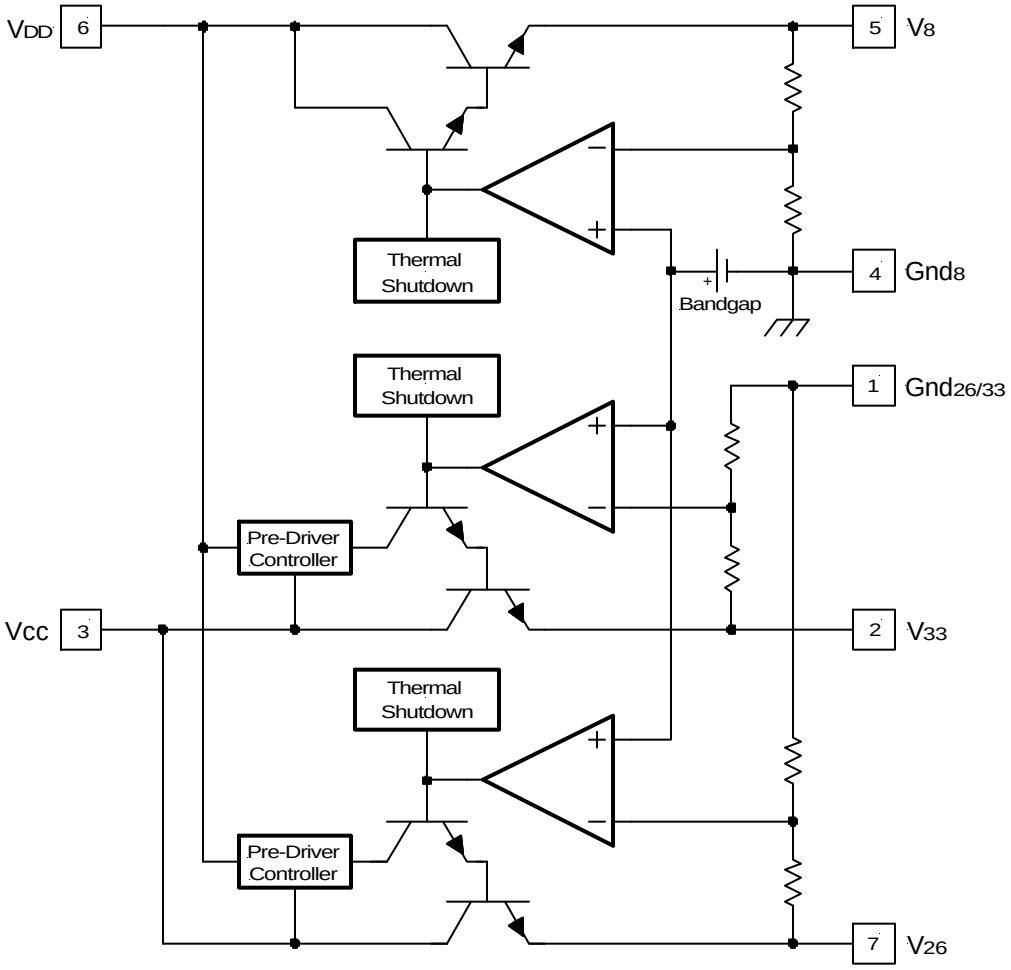



Figure 2 - Simplified block diagram of the IRU1237SC.

# APPLICATION INFORMATION

**Introduction**

The IRU1237SC regulator is 7-pin terminal device and contains three integrated, fixed, linear regulators. The dual inputs provide a low dropout voltage for $V_{33}$ and $V_{26}$ by biasing the base current to power NPN transistors. The IRU1237SC is designed to meet the fast current transient needs as well as an accurate initial voltage, thus reducing the overall system cost with the need for fewer number of output capacitors.

**Thermal Protection**

The IRU1237SC provides thermal protection for all three outputs. All outputs will be disabled for any over-temperature condition. When one of the outputs exceeds the thermal limit (typically 150°C), the IRU1237SC shuts down all three outputs simultaneously. The outputs will be re-enabled when the temperature drops below the thermal limit.

**Current Limit Protection**

The IRU1237SC provides over current protection when one the outputs' current exceeds the current limit level.

**Stability**

The IRU1237SC doesn't require input and output capacitors for stability, however to improve the transient response and guarantee stability, it is recommended that a 0.1μF (minimum) ceramic for input and output capacitors be used.

**Transient Response and PSRR**

The input and output capacitors are critical in order to ensure good transient response and PSSR. The most important aspects of this are capacitor selection, placement, and trace routing. Place each capacitor as close as physically possible to it's corresponding regulator pin. Use wide traces for low inductance path. Couple directly to the ground and power planes as possible. The use of low ESR capacitors is crucial to achieving good results. An input capacitance of at least 0.1μF is recommended. An output capacitance of at least 0.1μF with low ESR is recommended for good PSSR at high frequencies. Ceramic capacitors are a good choice for low ESR. Larger capacitance and lower ESR will improve both PSSR and transient response.

**Thermal Design**

The IRU1237SC incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the allowable maximum junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number.

The following thermal design illustrates the method used to calculate the maximum junction temperature of the regulator.

| | | |
|---|---|---|
| $V_{IN1}$=5.25V | $V_{OUT1}$=2.6V | $I_{OUT1}$=0.5A |
| $V_{IN2}$=12V | $V_{OUT2}$=3.3V | $I_{OUT2}$=0.5A |
| | $V_{OUT3}$=8V | $I_{OUT3}$=0.1A |

Calculating the maximum power dissipation:

$P_D = (V_{IN1}-V_{OUT1}) \times I_{OUT1}+(V_{IN1}-V_{OUT2}) \times I_{OUT2}+(V_{IN2}-V_{OUT3}) \times I_{OUT3}$

$P_D = (5.25-2.6) \times 0.5+(5.25-3.3) \times 0.5+(12-8) \times 0.1$

$P_D = 2.7W$

For Ultra Thin-Pak™ we have:

$R_{TH(JA)}$=30W/°C

$T_A = 50°C$

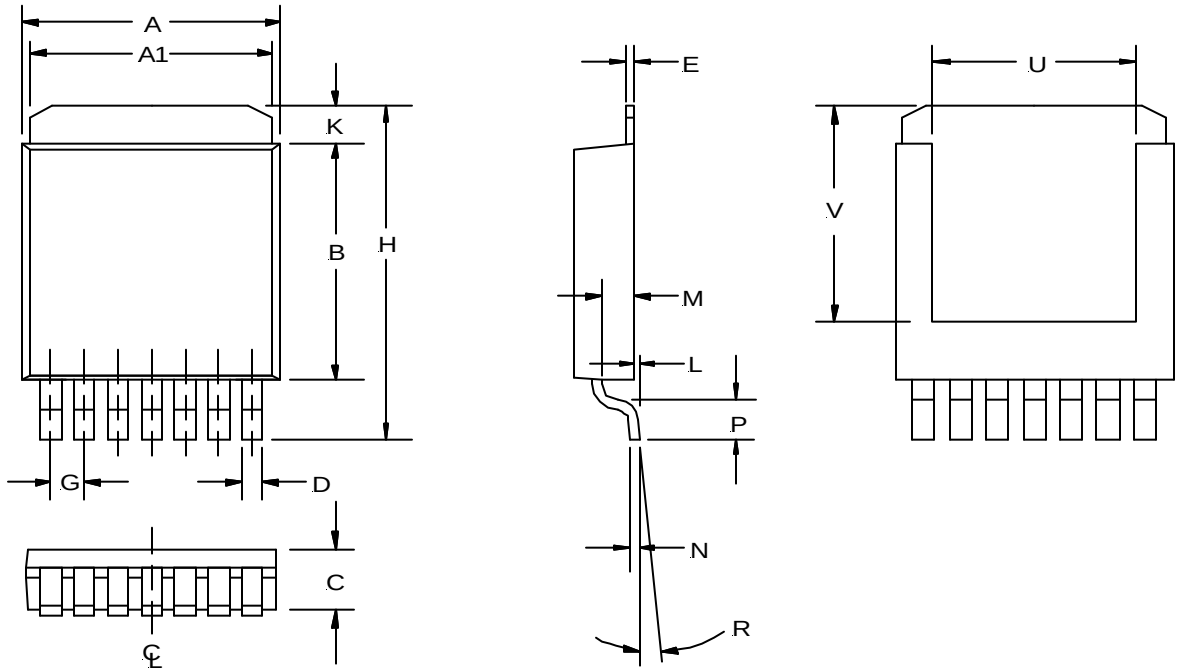
$\Delta T = P_D \times R_{TH(JA)} = 2.7W \times 30 = 81°C$

$T_J = T_A+\Delta T = 131°C$

**Layout Consideration**

The IRU1237SC, like many other high-speed regulators, requires that the output capacitors be close to the device for stability. For power consideration, a ground plane pad of approximately one-inch square on the component side must be dedicated to device where all ground pins are connected to dissipate the power. The copper area under the package shall have vias to the internal ground plane. The thermal ground plane shall extend out from the regulator to open areas of the PCB. All open areas shall be filled with copper to help radiate heat from the PCB.

## (P) Ultra Thin-Pak™
## 7-Pin

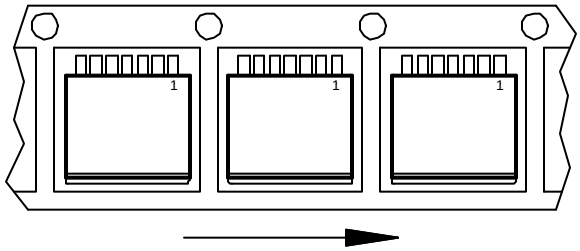



| SYMBOL | MIN | MAX |
|---|---|---|
| A | 9.27 | 9.52 |
| A1 | 8.89 | 9.14 |
| B | 7.87 | 8.13 |
| C | 1.78 | 2.03 |
| D | 0.63 | 0.79 |
| E | 0.25 NOM | |
| G | 1.27 | |
| H | 10.41 | 10.67 |
| K | 0.76 | 1.27 |
| L | 0.03 | 0.13 |
| M | 0.89 | 1.14 |
| N | 0.25 | |
| P | 0.79 | 1.04 |
| R | 3° | 6° |
| U | 5.59 NOM | |
| V | 7.49 NOM | |

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

## PACKAGE SHIPMENT METHOD

| PKG DESIG | PACKAGE DESCRIPTION | PIN COUNT | PARTS PER TUBE | PARTS PER REEL | T & R Orientation |
|---|---|---|---|---|---|
| P | Ultra Thin-Pak™ | 7 | 75 | 2500 | Fig A |




Feed Direction
Figure A

International
IOR Rectifier

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