20-PIN SYNCHRONOUS PWM CONTROLLER/ 3 LDO CONTROLLER

FEATURES

- Synchronous Controller plus 3-LDO controllers
- Current Limit using MOSFET Sensing
- Dual Soft-Start Function allows power sequencing
- Single 5V/12V Supply Operation
- Programmable Switching Frequency up to 400KHz
- Fixed Frequency Voltage Mode
- 1A Peak Output Drive Capability

APPLICATIONS

- Graphic Card
- DDR memory source sink V_{TT} application
- Applications with Multiple Outputs
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Hard Disk Drive

DESCRIPTION

The IRU3072 controller IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter for multi-output applications. The outputs can be programmed as low as 0.8V for low voltage applications.

The IRU3072 features dual soft-starts which allows power sequencing between outputs.

Over current limit is provided by using external MOSFET's on-resistance for optimum cost and performance.

This device features a programmable frequency set from 200KHz to 400KHz, under-voltage lockout for all input supplies, dual external programmable soft-start functions as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

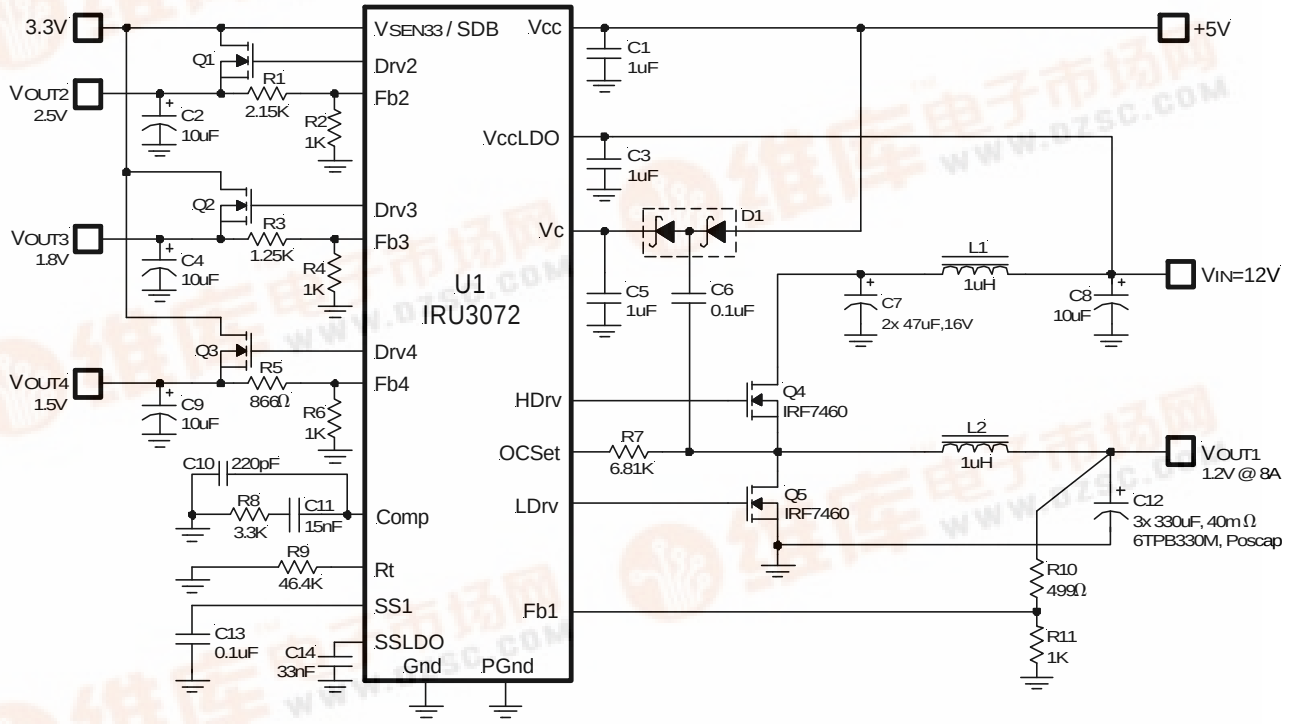


Figure 1 - Typical application of IRU3072.

PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3072CH	20-Pin MLPQ 4x4 (H)

ABSOLUTE MAXIMUM RATINGS

Vcc and VccLDO Supply Voltage 25V
Vc Supply Voltage 25V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

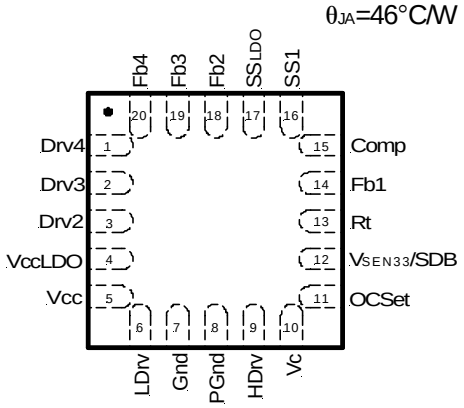
CAUTION: For all pins, voltage should not be below -0.5V.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

PACKAGE INFORMATION

20-PIN MLPQ 4x4 (H)

θ_{JA}=46°C/W



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the typical specification value applies over Vcc=5V, Vc=12V, VccLDO=5V and T_A=25°C. the Min and Max limits apply to the temperature range from 0 to 70°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
Feedback Voltage	V_{FB}		0.784	0.8	0.816	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2	0.625	%
UVLO						
UVLO Threshold - Vcc	UVLO V_{CC}	Supply Ramping Up	3.8	4.2	4.6	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO V_C	Supply Ramping Up	3.2	3.5	3.8	V
UVLO Hysteresis - Vc				0.2		V
UVLO Threshold - VccLDO	UVLO V_{CCLDO}	Supply Ramping Up	2.25	2.5	2.75	V
UVLO Hysteresis - VccLDO				0.15		V
UVLO Threshold - V_{SEN33}	UVLO V_{SEN33}	Supply Ramping Up	1.17	1.27	1.37	V
UVLO Hysteresis - V_{SEN33}				0.07		V
UVLO Threshold - Fb1, 2, 3, 4	UVLO Fb1	Fb Ramping Down	0.3	0.4	0.5	V
UVLO Hysteresis - Fb1, 2, 3, 4				0.02		V
Supply Current						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=3000pF		11	14	mA
Vc Dynamic Supply Current	Dyn I_C	Freq=200KHz, C_L=3000pF		11	14	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		5	8	mA
Vc Static Supply Current	I_{CQ}	SS=0V		3	5	mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Soft-Start Section						
Charge Current	SS I_{B1},I_{B2}	SS1=SS2=0V	15	25	35	µA
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS1=3V		0.1	1	µA
Fb Voltage Input Bias Current	I_{FB2}	SS1=0V	35		75	µA
Transconductance			500	900	1300	µmho
Oscillator						
Frequency	Freq	Rt=100K	170	200	230	KHz
		Rt=39K	340	400	460	
Ramp Amplitude	V_{RAMP}	Note 1		1.27		V_{PP}
Output Drivers						
Rise Time	Tr	C_{LOAD}=3000pF (10% to 90%) Vcc=12V		50	100	ns
Fall Time	Tf	C_{LOAD}=3000pF (90% to 10%), Vcc=12V		50	100	ns
Dead Band Time 1	T_{DB}	Vcc=12V, C_{LOAD}=3000pF HDrv falls,LDrv rises	50	115	150	ns
Dead Band Time 2		Vcc=12V, C_{LOAD}=3000pF LDrv falls, HDrv rises	20	50	100	ns
Max Duty Cycle	D_{MAX}	Fb=0.7V, Freq=200KHz	85	92	99	%
Min Duty Cycle	D_{MIN}	Fb=0.9V		0		%
LDO Controller Section						
Drive Current		Drv2, 3 and 4	40	60		mA
Fb Voltage			0.784	0.8	0.816	V
Input Bias Current				0.5	2	µA
Thermal Shutdown		Note 1		150		°C
Current Limit						
OC Threshold Set Current	I_{OCSET}		23	30	37	µA
OC Comp Off-Set Voltage	$V_{OC(OFFSET)}$		-7	0	+7	mV

Note 1: Guaranteed by design but not tested in production.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Drv4	Outputs of the linear regulator controllers.
2	Drv3	
3	Drv2	
4	VccLDO	This pin provides power for the LDO controllers.
5	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
6	LDrv	Output driver for the synchronous power MOSFET.
7	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from Vcc, Vc and VccLDO pins to this pin for noise free operation.
8	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to system's ground plane.
9	HDrv	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from this pin to ground for the application when the inductor current goes negative (Source/ Sink), soft-start at no load and for the fast load transient from full load to no load.

PIN#	PIN SYMBOL	PIN DESCRIPTION
10	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
11	OCSet	This pin is connected to the Drain of the synchronous MOSFET and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the current sense (CS) threshold depending on the R_{DS} of the power MOSFET.
12	V_{SEN33}/SDB	This pin is used to monitor the 3.3V rail. This pin can be pulled-low to shutdown the outputs.
13	Rt	This pin sets the switching frequency with a resistor to Gnd.
14	Fb1	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
15	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
16	SS1	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current.
17	SS_{LDO}	This pin provides soft-start for the LDO controllers. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the LDO controller, preventing it from overshooting as well as limiting the input current.
18 19 20	Fb2 Fb3 Fb4	These pins provide feedback for the linear regulator controllers.

BLOCK DIAGRAM

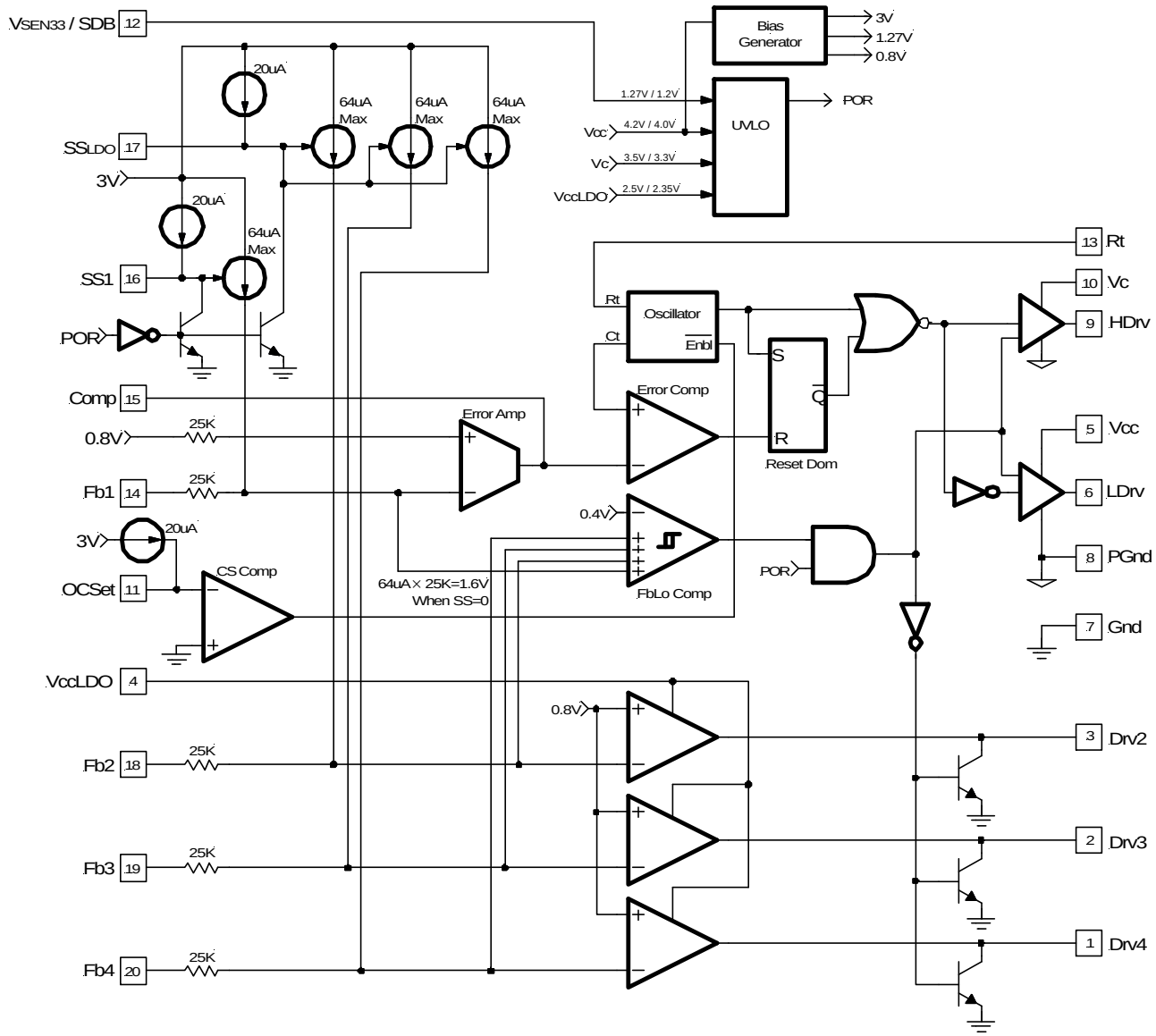


Figure 2 - Simplified block diagram of the IRU3072.

TYPICAL APPLICATION

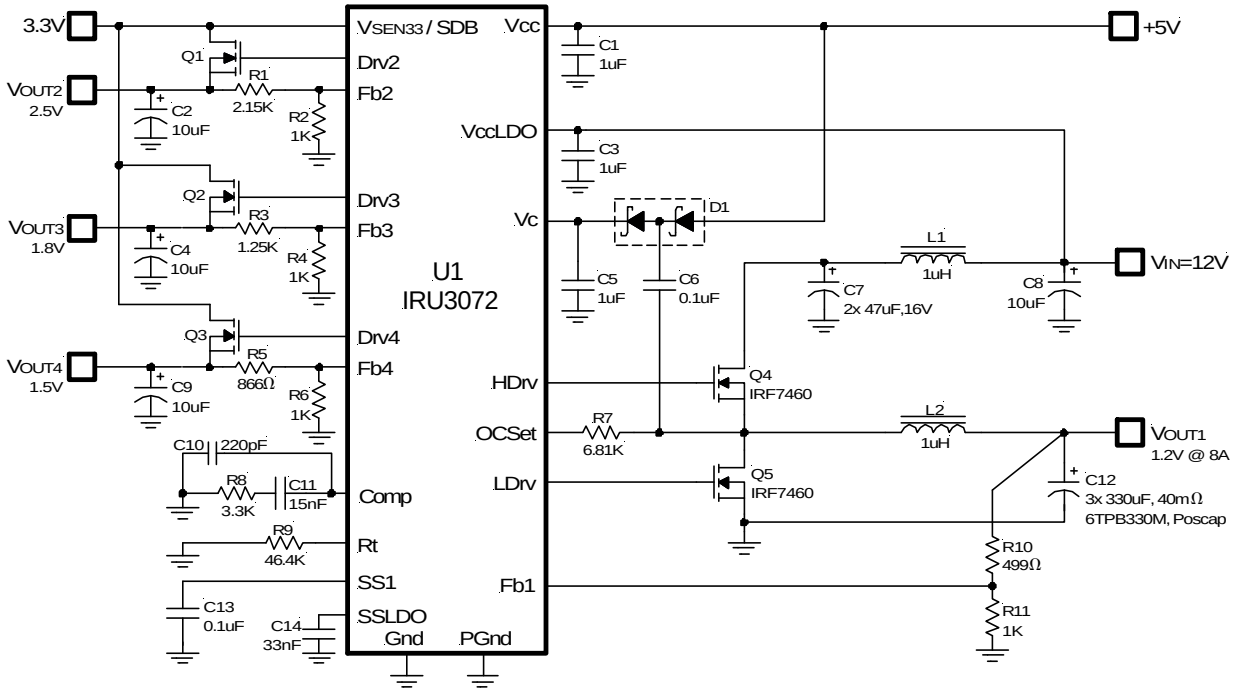


Figure 3 - Typical application of IRU3072.

PARTS LIST

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q2,Q3	MOSFET	30V, 65mΩ, 22A	3	IRLR2703	IR	irf.com
Q4,Q5	MOSFET	20V, 10mΩ, 12A	2	IRF7460	IR	
U1	Controller	Synchronous PWM	1	IRU3072	IR	
D1	Schottky Diode	0.2A, 30V	1	BAT54S	IR	
L1	Inductor	1μH, 2A	1	DS1608C-102	Coilcraft	coilcraft.com
L2	Inductor	1μH	1	DO3316P-102HC	Coilcraft	
C1,C3	Capacitor	1μF, Y5V, 16V	2	ECJ-2VF1C105Z	Panasonic	maco.panasonic.co.jp
C2,C4,C9	Capacitor	10μF	3			
C5	Capacitor	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C6,C13	Capacitor	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	
C7	Capacitor	47μF, 16V	2	16TPB47M	Sanyo	sanyo.com
C8	Capacitor	10μF	1		Any	
C10	Capacitor	220pF, X7R	1	ECU-V1H221KB	Panasonic	maco.panasonic.co.jp
C11	Capacitor	15nF	1	ECJ-2VB1H153K	Panasonic	
C12	Capacitor	330μF, 6.3V, 40mΩ	3	6TPB330M	Sanyo	sanyo.com
C14	Capacitor	33nF, X7R	1	ECJ-2VB1H333K	Panasonic	maco.panasonic.co.jp
R1	Resistor	2.15K, 1%	1		Any	
R2,R4,R6	Resistor	1K, 1%	3		Any	
R3	Resistor	1.25K, 1%	1		Any	
R5	Resistor	866Ω, 1%	1		Any	
R7	Resistor	6.81K, 1%	1		Any	
R8	Resistor	3.3K, 1%	1		Any	
R9	Resistor	46.4K, 1%	1		Any	
R10	Resistor	499Ω, 1%	1		Any	
R11	Resistor	1K, 1%	1		Any	

APPLICATION INFORMATION

The IRU3072 controller IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter as well as three linear regulator controllers. It is specially designed for multiple output applications. The outputs can be programmed as low as 0.8V.

The IRU3072 provides two separate soft-starts. It not only allows different output power sequences, but also allows shutdown of LDO and PWM output regulators individually.

The IRU3072 provides cycle-by-cycle current limit and output feedback under-voltage lockout.

Power Sequence and Under-Voltage Lockout

For correct operation, proper power sequence should be ensured. Typically, there are four or five input voltages involved.

Vcc: IC biasing voltage.
V_{SEN33}: LDO Input voltage, for example 3.3V
VccLDO: Input biasing voltage for IRU3072 internal LDO controller.
V_{BUS}: Input voltage for synchronous buck converter.
Vc: Input biasing voltage for IRU3072 internal high side MOSFET drivers.

The power sequence should be proper such that soft-start capacitors (for both LDO and PWM) start to be linearly charged up right after the above five voltages enter into steady state, as shown in the following figure.

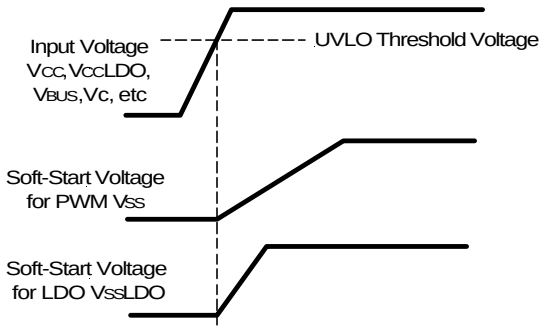


Figure 4 - Desired power sequence.

The IRU3072 senses four voltages with under-voltage lockout (UVLO) block. The voltages Vcc, Vc and VccLDO are sensed through the UVLO block. The LDO input voltage can be sensed through pin V_{SEN33}. Although synchronous bus voltage (V_{BUS}) is not sensed, in practical, it can be sensed indirectly. Typically, only two or three input voltages are available. Some of the five input voltages have to either share or be generated by another method such as charge pump. One example of IRU3072 application with only two input voltages, 5V and 3.3V, is shown in figure 5. In this example:

V_{BUS} = Vcc = 5V
Vc = VccLDO created by charge pump
V_{SEN33} = 3.3V

The IRU3072 will sense all four voltages to ensure all these voltages enter into steady state before the soft-start capacitor is charged up. The operation waveforms are shown in Figure 6.

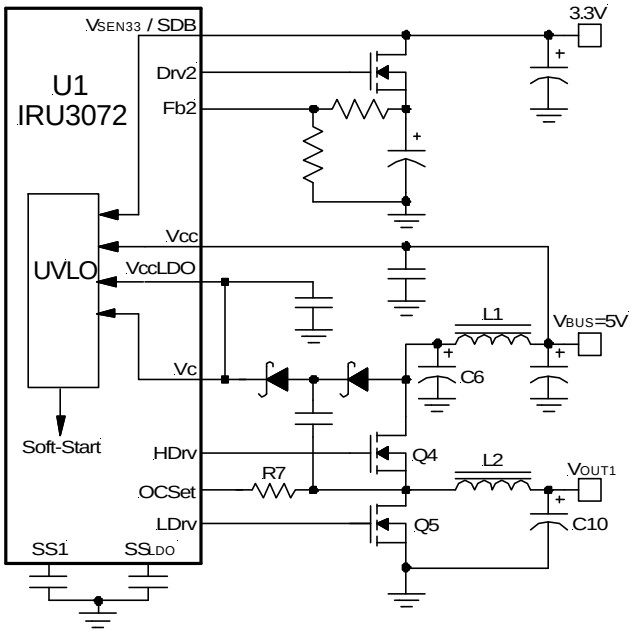


Figure 5 - IRU3072 application with only two power inputs: 5V and 3.3V.

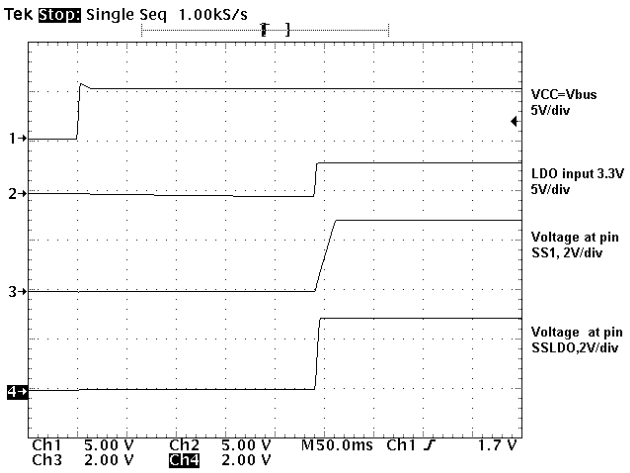


Figure 6 - Power sequence.

If there are three input voltage sources available, such as 3.3V, 5V and 12V, the possible connections to ensure proper operation are shown in the following table.

Option	Vcc	V_{BUS}	Vc	VccLDO	LDO Input
1	5V	5V	12V	12V	3.3V
2	5V	12V	CP	12V	3.3V
3	12V	12V	CP	12V	3.3V
4	12V	5V	12V	12V	3.3V
more					

Table: Possible combination of input voltage source connections to ensure proper start-up operation. (CP refers to Charge Pump)

There are many possible combinations of input voltage source connections and the table above lists only a few of them. Most importantly for a proper power sequence, the soft-start capacitor has to be charged up after all the input voltage sources are established.

Soft-Start

One of the useful features of IRU3072 is that it allows different start-up times for PWM output and LDO output by programming two separate soft-start capacitors. Figure 7 just shows the soft-start for PWM section.

The soft-start operation can ensure the output voltage ramps up to the regulated voltage without surge of the current. The IRU3072 also has an output feedback UVLO block, which will turn off both high side and low side MOSFET driver when the voltage at pin Fb1,Fb2,Fb3 or Fb4 is below 0.4V. The feedback UVLO is used to protect the system when the output is in short circuit. However, during the power on of the buck converter, the output of buck converter starts from zero and the voltage at pin Fb1 will be below 0.4V. The feedback UVLO should be disabled when soft-start capacitor voltage ramps up and down. This is achieved by injecting a current into the Fb1 pin (also Fb2, Fb3 and Fb4) during the soft-start and the magnitude of this current is inversely proportional to the voltage at soft-start pin (SS or SSLDO). The diagram is shown in Figure 7 and operation waveforms are shown in Figure 8. The operation principle is as follows:

Initially, the buck converter's output voltage and the voltage at pin Fb1 are both zero. The voltage at soft-start pin "SS" is almost zero and about 64μA current will inject to the pin of Fb1 through a 25KΩ internal resistor. The voltage at the negative input of Error Amplifier and the positive input of the feedback UVLO comparator is approximately:

$$64\mu A \times 25K\Omega = 1.6V$$

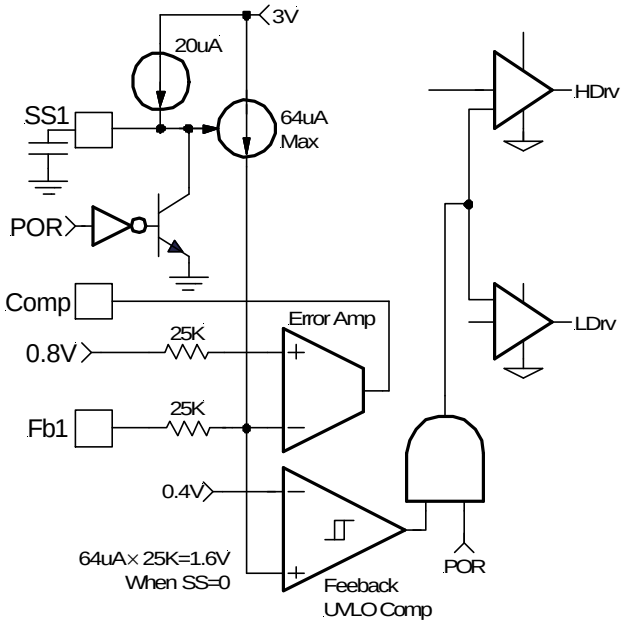


Figure 7 - IRU3072 soft-start diagram.

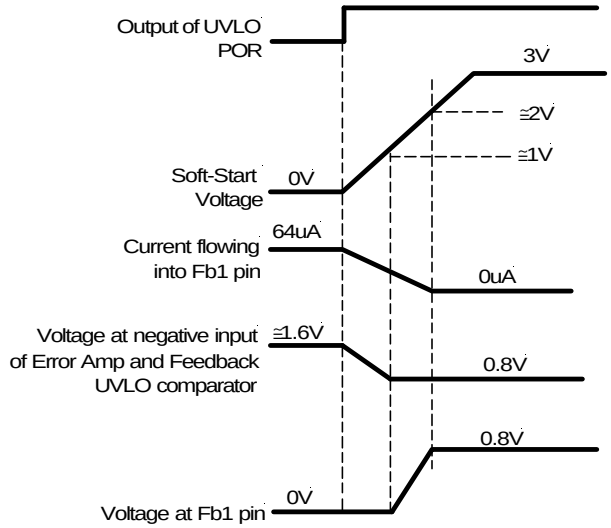


Figure 8 - Theoretical operation waveforms during soft-start.

When the power voltage such as Vcc go into steady state and the output of voltage UVLO "POR" goes high, a 20uA current source charges the external soft-start capacitors. The soft-start voltage ramps up. In the mean time, the current flowing into pin Fb1 starts to decrease linearly and so does the voltage at the positive pin of feedback UVLO comparator and the voltage at the negative input of Error amplifier. When the soft-start capacitor voltage is around 1V, the current flowing into the Fb1 pin is approximately 32μA. The voltage at the positive input of the Error amplifier is approximately:

$$32\mu A \times 25K\Omega = 0.8V$$

The Error Amplifier will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb1 pin will keep decreasing. Because the voltage at pin of Error Amplier is regulated to reference voltage 0.8V, the voltage at the Fb1 pin is:

$$V_{FB1} = 0.8V - 25K\Omega \times (\text{Injecting Current})$$

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 2V and the output voltage goes into steady state.

Figure 8 shows that the voltage at the positive pin of feedback UVLO comparator is always higher than 0.4V, therefore, feedback UVLO is not functional during soft-start.

From the above analysis, the output start up time is the period when soft-start capacitor voltage increases from 1V to 2V. The start up time will be dependent on the size of the external soft-start capacitor. The start up time can be estimated by:

$$20\mu A \times t_{START}/C_{SS} \cong 2V\text{-}1V$$

For a given start up time, the soft-start capacitor can be estimated as:

$$C_{SS} \cong 20\mu A \times t_{START}/1V \quad \text{---(1)}$$

For 5ms start up time, a 0.1μF soft-start capacitor is required. In practice, the 20μA current will slightly decrease as the soft-start voltage goes up. Therefore, for a 0.1μF soft-start capacitor, start up time may be slightly longer, e.g. 6ms.

The soft-start waveforms are shown in Figure 9. In this figure, the start up time for the buck converter V_{OUT1} and LDOs is different by selecting separate soft-start capacitors.

For PWM: C_{SS} = 0.1μF, $t_{START} \cong$ 5ms
For LDOs: C_{SSLDO} = 33nF, $t_{START} \cong$ 2ms

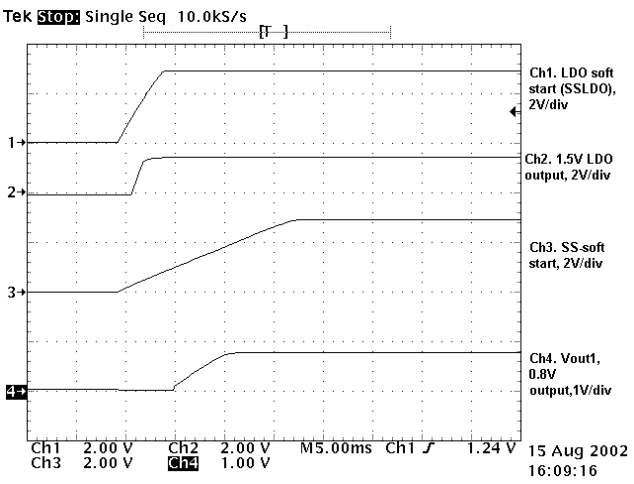
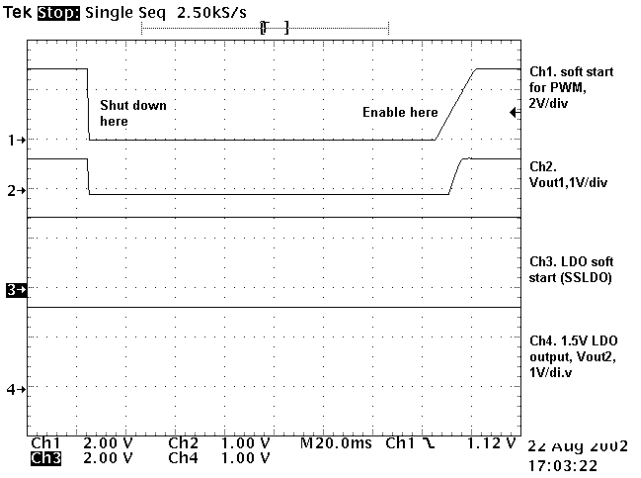


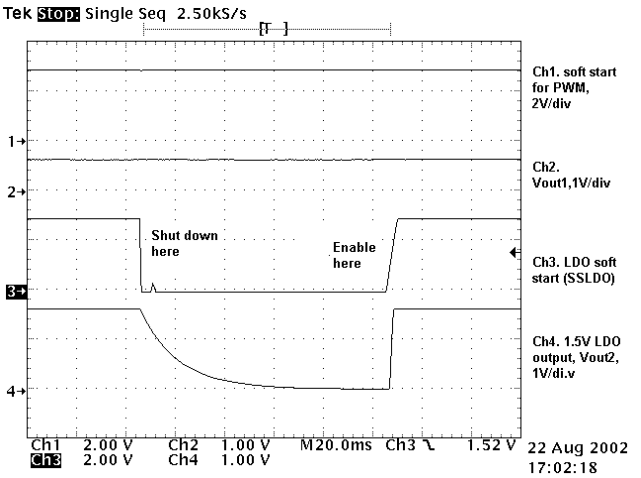
Figure 9 - Soft-start of buck converter (PWM) and LDO.

Shutdown

The PWM output and LDO output can be turned on and off individually by pulling up and down the corresponding soft start capacitors.



(a). Shutdown and start up PWM output by controlling soft start SS1. LDO output such as Vout2 will not be affected.



(b). Shutdown and start up LDO output by controlling soft-start SSLDO. PWM output V_{OUT1} will not be affected.

Figure 10 - Shutdown PWM or LDO by controlling soft-start.

One issue related to shutdown of PWM output by pulling down the soft-start, there is a small negative voltage shown in the output during the shutdown. It is because the low side MOSFET driver is on when the soft-start capacitor voltage is pulling down. The output inductor resonates with output capacitor and load. This occurs especially often when output current is small (light load or no load condition). The operation waveforms are shown as follows.

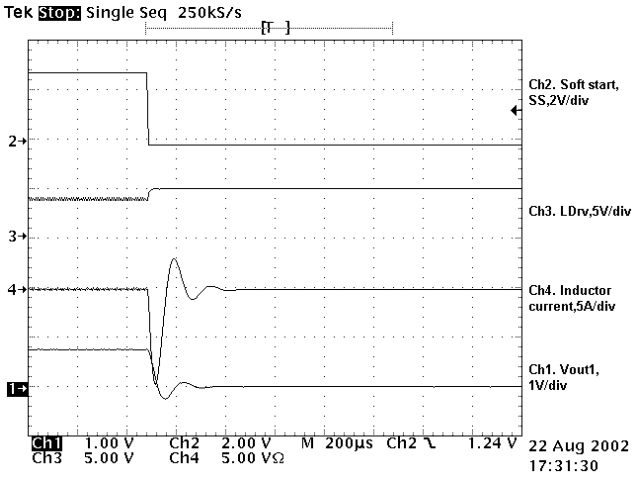


Figure 11 - Operation waveforms when PWM converter is shutdown by pulling down the soft-start capacitor.

Both PWM output and LDO output can be shutdown by pulling the pin V_{SEN33}/SDB down. One example is shown as follows.

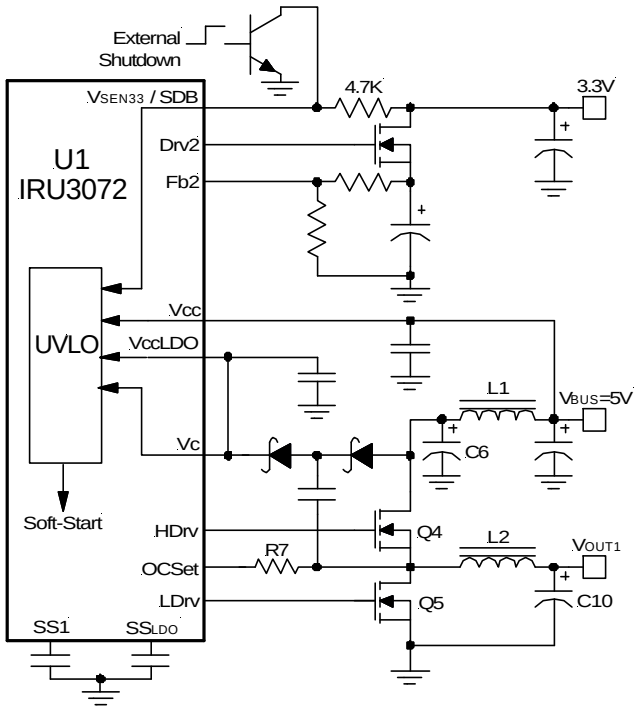


Figure 12 - External shutdown by using pin V_{SEN33}/SDB.

The LDO and PWM output can be shutdown by using a transistor to pull down the pin V_{SEN33}/SDB as shown in Figure 12. Because the V_{SEN33}/SDB pin also senses the LDO input voltage for the power UVLO block, a high impedance resistor such as 4.7K has to be inserted between V_{SEN33}/SDB pin and the input of LDO such as 3.3V. The input voltage UVLO operation will not be affected due to the high input impedance nature of V_{SEN33}/SDB pin. The operation waveforms is shown as follows:

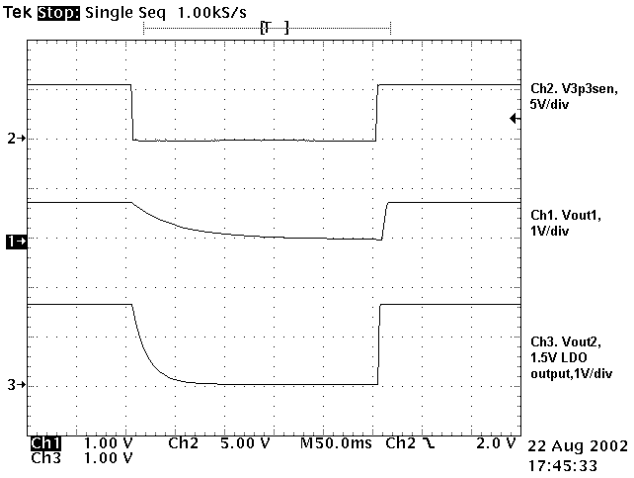


Figure 13 - Shutdown by pulling down pin V_{SEN33}/SDB.

One feature of shutdown by pulling down V_{SEN33}/SDB is that there is no negative voltage shown in the buck converter output because both high side and low side MOSFET drivers are off after shutdown.

Over Current Protection

The IRU3072 over current protection is achieved with a cycle-by-cycle current limit and an output voltage undervoltage lockout scheme. The diagram is shown in Figure 14. It includes an over current comparator and an output voltage UVLO comparator. The current is sensed through the $R_{DS(ON)}$ of the low side MOSFET. A resistor, R_{SET}, is connected from OCSet pin to the drain of the low side MOSFET in order to set the over-current limit. When the low side MOSFET Q2 is ON, the inductor current flows through MOSFET Q2. The voltage at OCSet pin is given as:

$$V_{OCSet} = 20\mu A \times R_{SET} - i_L \times R_{DS(ON)}$$

When voltage V_{OCSet} is below zero, the current sensing comparator flips and disables the oscillator. The high side MOSFET is turned off and the low side MOSFET is on until the inductor currents reduces to below current setting value. The critical inductor current can be calculated by setting:

$$V_{OCSet} = 20\mu A \times R_{SET} - i_L \times R_{DS(ON)} = 0$$
$$I_{SET} = i_L(critical) = 20\mu A \times R_{SET}/R_{DS(ON)} \quad ---(2)$$

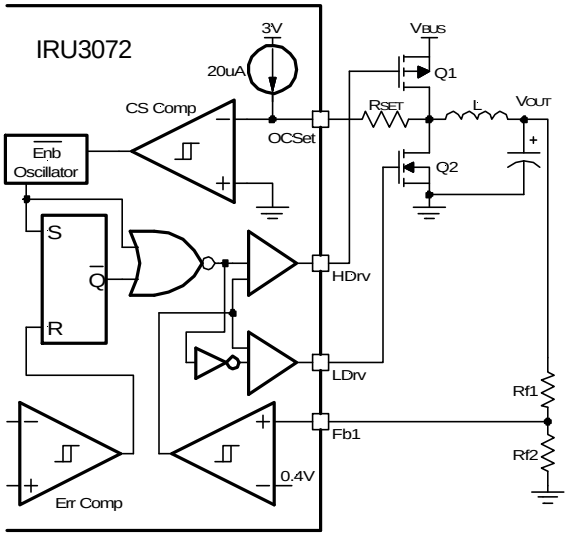


Figure 14 - IRU3072 current limit diagram.

The operation is illustrated in Figure 15.

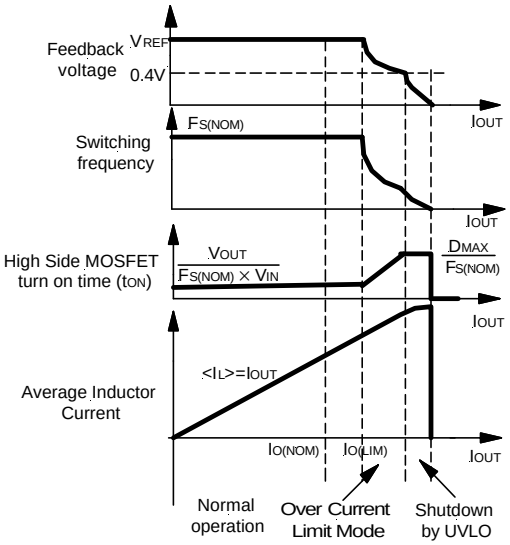


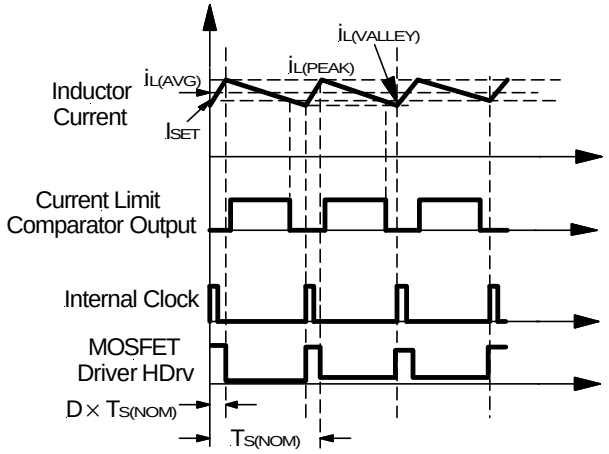
Figure 15 - Operation of IRU3072 current limit and UVLO.

During the normal operation mode, the synchronous buck converter operates in fixed frequency $F_{S(NOM)}$, which is the normal operation switching frequency and it is determined by the external resistor Rt. The output voltage is regulated to the desired voltage and the feedback voltage is equal to the reference voltage V_{REF}. The turn on time of the high side MOSFET is given as:

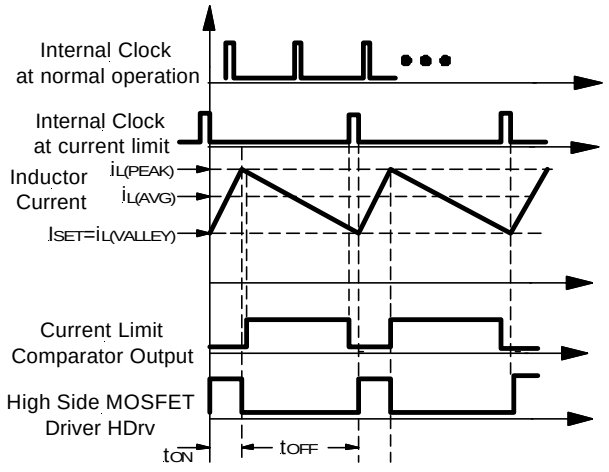
$$t_{ON}(normal) \cong D \times T_{S(NOM)} = V_{OUT}/(F_{S(NOM)} \times V_{IN})$$

As the load current goes up, the inductor current increases and the high side MOSFET's turn on time increases a little due to the voltage drop across the high side MOSFET $R_{DS(ON)}$.

As the output current increases to limit current, $I_L=I_{O(LIM)}$, which is set by the resistor R_{SET}. The buck converter will go into cycle-by-cycle current limit mode. The operation waveforms of IRU3072 during cycle-by-cycle current mode is shown in Figure 16.



(a) Normal operation.



(b). Operation at current limit mode.

Figure 16 - Cycle-by-Cycle operation when IRU3072 is in over-current limit mode.

From Figure 16, first, the high side MOSFET is on for t_{ON} period and the inductor current increases during this time. Then, the high side MOSFET is off and low side MOSFET is on. Because the inductor current is higher than the critical inductor current I_{SET}, the current sensing comparator goes high and the low side MOSFET keeps on. The inductor current is discharged by the output voltage. When the inductor current is below setting current or critical current I_{SET}, the current sensing comparator goes low and enables the oscillator. The high side MOSFET is turned on again and next cycle starts. The operation frequency is only dependent on the current sensing comparator and the internal clock frequency is modified by current limit.

In conclusion, from Figures 15 and 16, two big differences exist between normal operation and current limit mode. First, during current limit mode, the valley inductor current is determined by I_{SET}.

$$I_{SET} = i_{L(VALLEY)}$$

Second, in Figures 15 and 16, the frequency in current limit mode, is lower than normal operation frequency.

In general, the output current is represented by:

$$I_{OUT} = i_{L(AVG)} = i_{L(VALLEY)} + \Delta I_{PK\_PK}/2$$

Where ΔI_{PK_PK} is the peak to peak inductor current ripple which is given by:

$$\Delta I_{PK\_PK} = i_{L(PK)} - i_{L(VALLEY)} = (V_{IN} - V_{OUT}) \times t_{ON}/L$$

Figure 15 shows that the operation frequency of the buck converter decreases as output current goes up during current limit mode. The on time of high side MOSFET is controlled by the output voltage loop so that the voltage at Fb pin, still equals the reference voltage, $V_{FB}=V_{REF}$. The output voltage is regulated to the desired voltage.

As a result:

$$t_{ON} = V_{O(NOM)}/V_{IN}/F_S$$

$$I_{OUT(Current\ Limit\ Mode)} = I_{SET} + \frac{(V_{IN} - V_{O(NOM)}) \times V_{O(NOM)}}{(2 \times L \times V_{IN} \times Fs)}$$

Where $V_{O(NOM)}$ is the nominal output voltage and it is determined by the feedback resistor and reference voltage as shown in Figure 14. The above equation indicates that the operation frequency is inversely proportional to the output current during the current limit mode. For practical application, the most important is setting up the over current limit threshold. From Figure 15, at the current limit threshold $I_{O(LIM)}$, the frequency is still equal to nominal operation frequency.

$F_S = F_{S(NOM)}$

Therefore, the output current limit threshhold is set by:

$$I_{OUT(LIM)} = I_{SET} + \frac{\Delta I_{PK\_PK(LIM)}}{2}$$

Where:

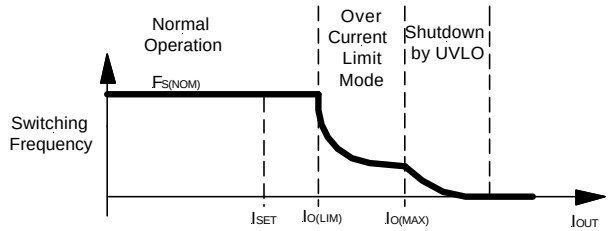
$$\Delta I_{PK\_PK(LIM)} = \frac{(V_{IN} - V_{O(NOM)}) \times V_{O(NOM)}}{(V_{IN} \times F_{S(NOM)} \times L)}$$

From equation (2), the over current limit set resistor can be calculated by:

$$R_{SET} = \frac{I_{SET} \times R_{DS(ON)}}{20\mu A}$$

$$R_{SET} = (I_{OUT(LIM)} - \Delta I_{PK\_PK(LIM)}/2) \times R_{DS(ON)}/20\mu A \quad ---(3)$$

Where $R_{DS(ON)}$ has to choose the maximum over the temperature for the selected MOSFET. Overall, the profile of current limit operation is shown in Figure 17.



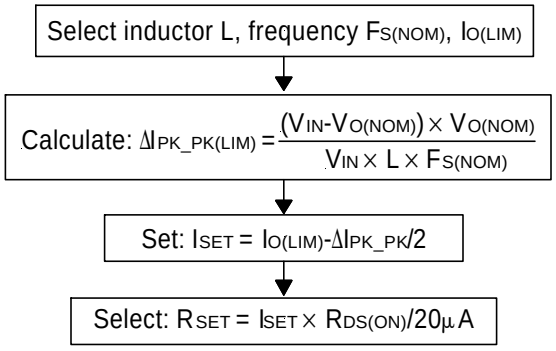
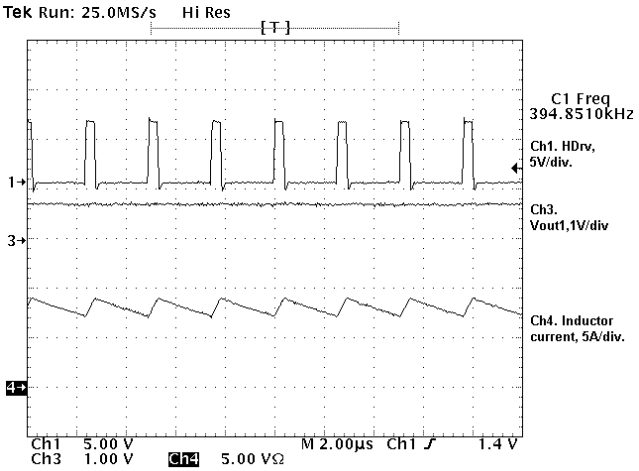
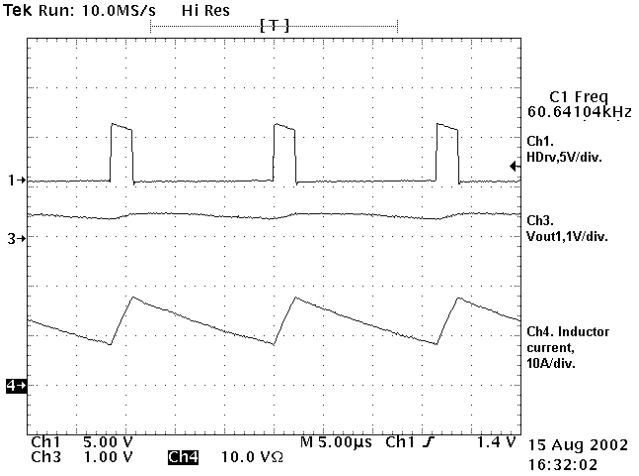


Figure 17 - Profile of operation switching frequency versus output current.



(a). Normal operation.



(b). Current limit mode.

Figure 18 - Operation waveforms during normal and current limit mode.

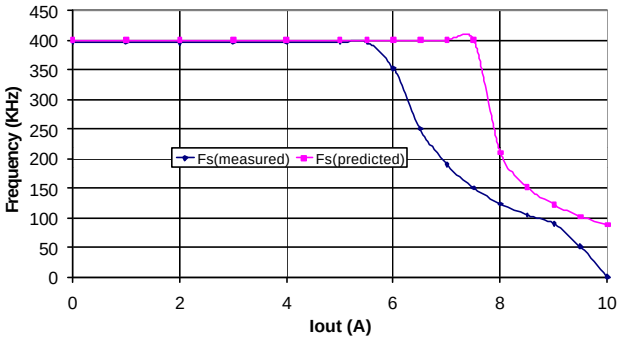


Figure 19 - Profile of switching frequency versus output current -predicted and measured.

Figure 18 (a) shows normal operation waveforms for a 12V input 1.6V output 400KHz buck regulator. During normal operation, the switching frequency is 400KHz. Figure 18 (b) shows the operation waveforms during current limit mode. The switching frequency is reduced and output ripple increases. Figure 19 shows the profile of switching frequency versus output current. When the output current goes up and hit the over current limit, the switching frequency starts to decreases. Due to the output voltage loop, the output voltage will keep the regulation except the ripple increases. As the output current keeps going up. The output voltage will start to decrease until the feedback voltage Fb is under 0.4V. The output voltage under lockout takes over and turns off both high side and low side MOSFET. The output voltage reduces to zero.

Output Feedback UVLO

Besides the cycle-by-cycle current limit, an output feedback UVLO is included in the IRU3072 for the output short protection. The diagram is shown in Figure 14. If the output is short or overload, once the voltage at the Fb1 pin is below 0.4V, the output feedback UVLO comparator will flip and turn off both high side and low side MOSFETs. The output of converter will decrease to zero. The operation when PWM output is in short circuit condition is shown in Figure 20. If either PWM or LDO output is in short condition, it will turn off all outputs. The operation waveforms are shown in Figures 21 and 22. Figure 23 shows a soft-start operation when the output is short. Because of current limit and output feedback UVLO, the output will be turned off and the system protected.

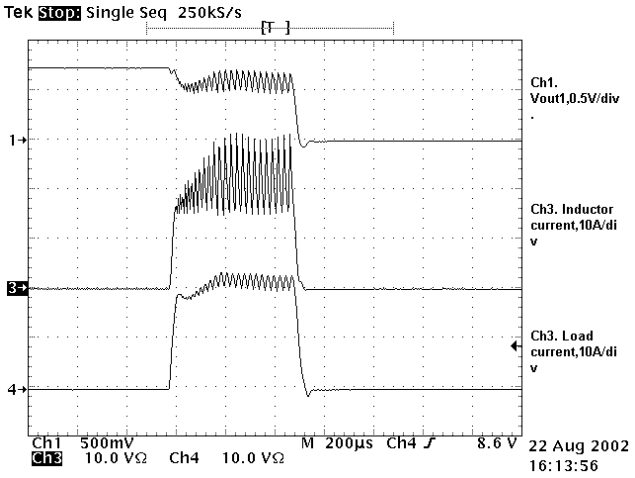


Figure 20 - Operation waveforms when output of buck converter is short to ground.

The output UVLO senses the four feedback pin voltages Fb1,Fb2,Fb3,Fb4. If any of the feedback voltages are below 0.4V, all four outputs will be shutdown.

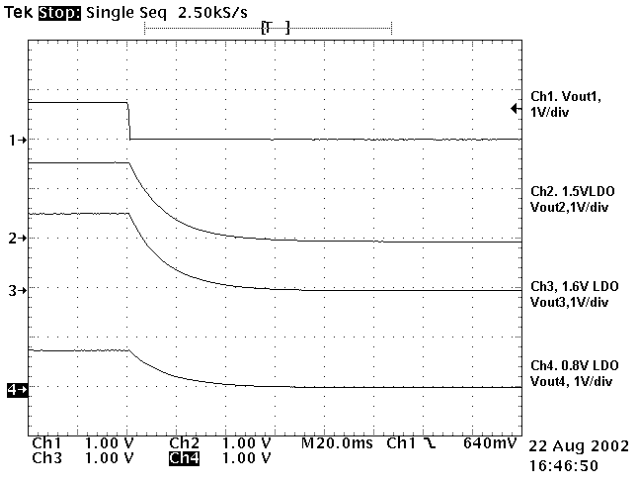


Figure 21 - Operation of PWM output and LDO when PWM output is short to ground.

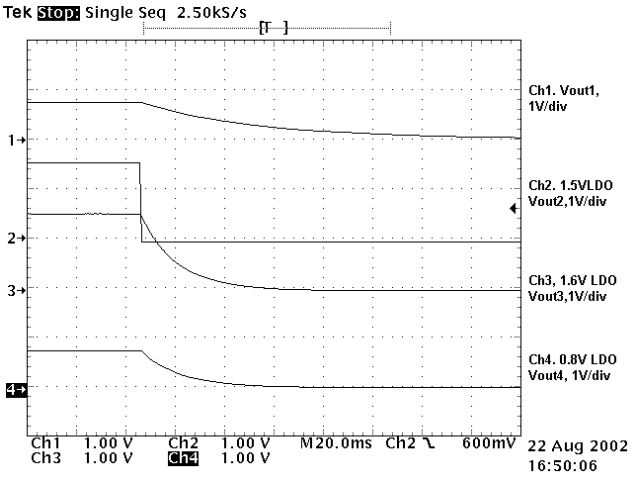


Figure 22 - Operation of PWM output and LDO when LDO V_{OUT2} is short.

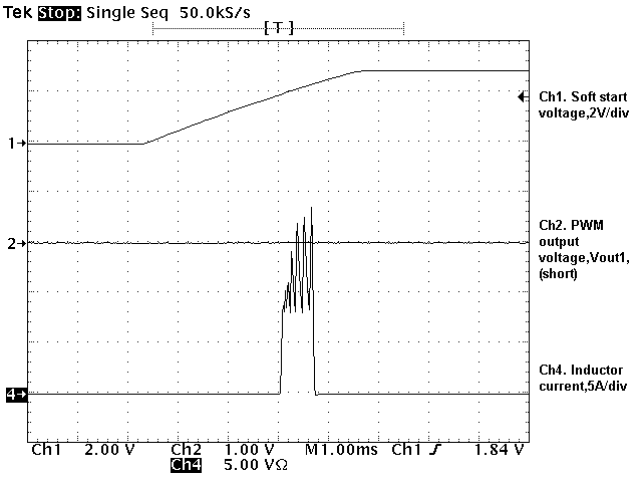


Figure 23 - Soft-start with output is short to ground.

Switching frequency

The switching frequency of IRU3072 can be selected by the following figure.

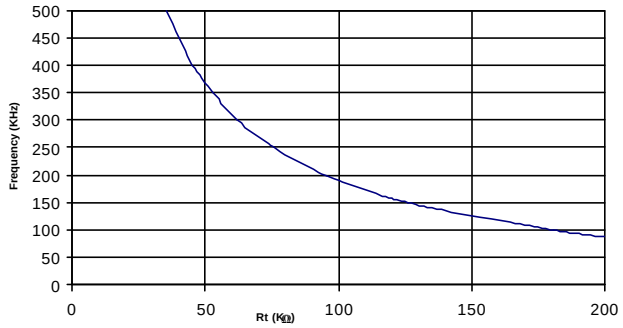


Figure 24 - Switching frequency versus resistor Rt.

Design Example

Input voltage for buck converter: V_{IN}=12V
Output voltage for buck converter: V_{OUT}=1.2V
Nominal output current from switching regulator: I_{OUT}=8A
Output current limit is 10A.
Switching frequency: F_S=400KHz
The maximum dynamic output voltage droop at 8A step load is 150mV.

LDO specification

LDO input voltage: $V_{IN(LDO)}$=3.3V
LDO output1: V_{OUT2}=2.5V @ 2A
LDO output2: V_{OUT3}=1.8V @ 2A
LDO output3: V_{OUT4}=1.5V @ 2A

Output inductor selection

The inductor is selected based on the inductor current ripple, operation frequency and efficiency consideration. In general, a large inductor results in a small output ripple and higher efficiency but large size. A small value inductor causes large current ripple and poor efficiency but small size. Generally, the inductor is selected based on the output current ripple. The optimum point is usually found between 20% and 50% ripple of output inductor current.

Suppose the ripple is selected as 40% of the total output current.

$$\Delta I_{PK\_PK}/I_{OUT} = 40\%$$

The current ripple is calculated as:

$$\Delta I_{PK\_PK} = (V_{IN}-V_{OUT}) \times V_{OUT}/(L \times F_S \times V_{IN})$$

Combining of above two equations, the inductance can be selected by:

$$L > V_{OUT} \times (V_{IN}-V_{OUT})/(F_S \times V_{IN} \times 40\% \times I_{OUT})$$

In this example,

$$L > 1.2V \times (12 - 1.2)/(400KHz \times 12V \times 0.4 \times 8A)$$
$$L > 0.8\mu H$$

Select inductor from Panasonic so that L=1μH. The ripple current is calculated as:

$$\Delta I_{PK\_PK} = (12 - 1.2) \times 1.2/(1\mu H \times 400KHz \times 12)$$
$$\Delta I_{PK\_PK} \cong 2.7A$$

Output capacitor selection

The voltage rating of the output capacitor is the same as the output voltage. Typical available capacitors on the market are electrolytic, tantalum and ceramic. If electrolytic or tantalum capacitors are employed, the criteria is normally based on the value of Effective Series Resistance (ESR) of total output capacitor. In most cases, the ESR of the output capacitor is calculated based on the following relationship:

$$ESR < \Delta V_{RIPPLE(SPEC)}/\Delta I_{PK\_PK}$$

or

$$ESR < \Delta V_{STEPLOAD(SPEC)}/\Delta I_{STEPLOAD(MAX)}$$

Depending on which one is the requirement.

Where:

$\Delta V_{RIPPLE(SPEC)}$ is the maximum allowed voltage ripple.

ΔI_{PK_PK} is the current ripple.

$\Delta V_{STEPLOAD(SPEC)}$ is the maximum allowed voltage droop during the transient or step load.

$\Delta I_{STEPLOAD(MAX)}$ is the maximum step load current.

In this example:

$$\Delta V_{STEPLOAD(SPEC)} = 150mV$$
$$\Delta I_{STEPLOAD(MAX)} = 8A$$

The required ESR is calculated as:

$$ESR < 150mV/8A = 18.75m\Omega$$

Select three Sanyo POSCAP 6TPB330M with 6.3V 330µF and 40mΩ ESR will give about 13mΩ, which will meet the specification.

Input capacitor Selection

Input capacitor is dertermined by the voltage rating and input RMS current. For this application, the input RMS current is given as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1-D)}$$
$$D = V_{OUT}/V_{IN} = 1.2V/12V \cong 0.1$$

The input RMS current is estimated as:

$$I_{IN(RMS)} = 8A \times \sqrt{0.1 \times (1-0.1)} \cong 2.4A$$

Select two Sanyo POSCAP -16TPB47M with 16V, 47µF and 1.4A ripple current. A 1µH, 1A small input inductor is enough for the input filer.

Power MOSFET Selection

In general, the MOSFET selection criteria depends on the maximum drain-source voltage, RMS current and ON resistance ($R_{DS(ON)}$). For both high side and low side MOSFETs, a drain-source voltage rating higher than maximum input voltage is necessary. In the demo-board, 20V rating should be satisfied. The gate drive requirement for each MOSFET is almost the same. If logic-level or 3V driver MOSFET is used, some caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through circuit.

If output inductor current ripple is neglected, the RMS current of high side switch is given by:

$$D = V_{OUT}/V_{IN} = 0.1$$
$$I_{RMS(HI)} = \sqrt{D} \times I_{OUT} = \sqrt{0.1} \times 8A = 2.53A$$

The RMS current of low side switch is given as:

$$I_{RMS(HI)} = \sqrt{1-D} \times I_{OUT} = \sqrt{1-0.1} \times 8A = 7.6A$$

For low side MOSFET, if it is driven by 5V, a logic gate driver MOSFET is preferred. For $R_{DS(ON)}$ of the MOSFET, it should be as small as possible in order to get highest efficiency. A logic driver MOSFET such as IRF7460 from International Rectifier in a SOIC 8-pin package, $R_{DS(ON)}$=10mΩ, 20V drain source voltage rating and 12A I_{DS} is selected for high side and low side MOSFET.

Power Dissipation for MOSFETs

The power dissipation for MOSFETS typically includes conduction loss and switching losses. For high side switch, the conduction loss is estimated as:

$$P_{COND(HI)} = D \times I_{OUT} \times I_{OUT} \times R_{DS(ON)MAX}$$

The $R_{DS(ON)}$ has to consider the worst case. In the datasheet of IRF7460:

$$R_{DS(ON)MAX} = 14m\Omega \text{ @ } Vgs = 4.5V$$
$$P_{COND(HI)} = 0.1 \times 8A \times 8A \times 14m\Omega \cong 0.09W$$

The switching loss is more difficult to calculate because of the parasitic parameters. In general, the switching loss can be estimated by the following:

$$P_{SW} = 0.5 \times V_{DS} \times I_{OUT} \times (tr+tf) \times F_S$$

tr is the rising time and tf is the falling time. From IRU3072 datasheet: tr=50ns and tf=50ns

$$P_{SW(HI)} = 0.5 \times 12V \times 8A \times (50ns+50ns) \times 400KHz$$
$$P_{SW(HI)} \cong 1.92W$$

The total disspation for the high side switch is:

$$P_{D(HI)} = P_{SW(HI)} + P_{COND(HI)} \cong 2W$$

For low side switch, most of the loss are conduction loss. The low side switch power dissipation is:

$$P_{D(LO)} \cong P_{COND(LO)} = (1-D) \times I_{OUT} \times I_{OUT} \times R_{DS(ON)MAX}$$
$$P_{D(LO)} \cong P_{COND(LO)} = (1-0.1) \times 8A \times 8A \times 14m\Omega$$
$$P_{D(LO)} \cong P_{COND(LO)} = 0.81W$$

Estimated Temperature Rise for MOSFET

The estimated junction temperature of the MOSFET is given by:

$$T_J = T_A + P_D \times R_{\theta JA}$$

Where:
T_J is the junction temperature.
T_A is the ambient temperature.
P_D is the power dissipation.
$R_{\theta JA}$ is the junction-to-ambient thermal resistance with MOSFET on 1" square PCB board and is from the data sheet.

For MOSFET IRF7460 with SOIC 8-pin package, $R_{\theta JA}$=50°C/W. Assume ambient temperature is T_A=35°C. For high side MOSFET, the junction temperature is given as:

$$T_J = T_A + P_D \times R_{\theta JA} = 35 + 2 \times 50 = 135°C < 150°C$$

For low side MOSFET IRF7460, the maximum junction temperature can be calculated as:

$$T_J = T_A + P_D \times R_{\theta JA} = 35 + 0.81 \times 50 = 76°C < 150°C$$

The maximum junction temperature of both MOSFETs is below the maximum rating of 150°C.

Controller Parameter Calculation

(1) Frequency Selection
From Figure 23, the frequency setting resistor can be chosen to be Rt=47KΩ, which gives us approximately 400KHz frequency.

(2) Soft-Start Capacitor
Soft-start capacitor for PWM secton is selected from equation (1). Select start up time t_{START}=5ms:

$$C_{SS} = 20\mu A \times t_{START} = 20\mu A \times 5ms = 0.1\mu F$$

Select C11=C_{SS}=0.1μF

(3) Over Current Limit Setting
The over current limit resistor can be calculated based on Figure 17. The output current limit is set by:

$$I_{O(LIM)} = 10A$$

The current ripple during nomral operation (400KHz) is given by:

$$\Delta I_{PK\_PK} = (12-1.2) \times 1.2/(1\mu H \times 400KHz \times 12)$$
$$\Delta I_{PK\_PK} \cong 2.7A$$

The over current setting I_{SET} is:

$$I_{SET} = I_{O(LIM)} - \Delta I_{PK\_PK}/2 = 10A - 2.7A/2 \cong 8.7A$$

The over current setting resistor:

$$R_{SET} = I_{SET} \times R_{DS(ON)}/20\mu A$$

For low side MOSFET IRF7460, with 4.5V gate voltage and maximum $R_{DS(ON)}$ of 14mΩ, then:

$$R_{SET} = 8.7A \times 14m\Omega/20\mu A = 6.09K\Omega$$

Select R7=R_{SET}=6.8KΩ

(4) Compensation Design

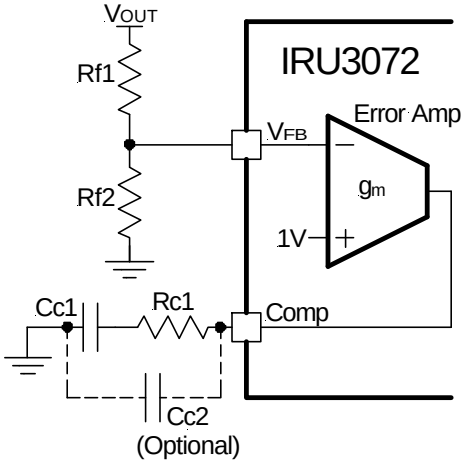


Figure 25 - Type II compensator.

For electrolytic capacitor, the frequency caused by ESR is typically at a few KHz range. A type II compensator is a good option. The detailed description is shown in application note AN-1043 from:

http://www.irf.com/technical-info/appnotes.htm

Select the zero crossover frequency to be 1/10 of switching frequency that is 40KHz:

$$F_O = 40KHz$$

The compensation resistor can be calculated as:

$$Rc1 = \frac{2\pi \times F_O \times L \times V_{OSC} \times V_{OUT}}{(ESR \times V_{IN} \times g_m \times V_{REF})}$$

Where V_{OSC} is the oscillator peak to peak voltage and gm is the transconductance of the error amplifier. From the datasheet we get V_{OSC}=1.25V and g_m=1000μmho. The calculated compensation resistor is:

$$Rc1 = 2\pi \times 40 \times 1 \times 1.25 \times 1.2/(13 \times 12 \times 1000 \times 0.8)$$
Rc1=2.98K
Select R8=Rc1=3.3K

The compensator capacitor is given as:

$$Cc1 = \sqrt{(L \times C_{OUT})}/0.75/Rc1$$
$$Cc1 = \sqrt{(1\mu H \times 450\mu F)}/0.75/3.3K = 10nF$$
Select C9=Cc1=15nF

(Optional) an additional capacitor Cc2 can be adopted, where:

$$Cc2 \cong 1/(\pi \times Rc1 \times F_S) \cong 220pF$$

(5) Feedback resistor

The output of PWM is determined by:

$$V_{OUT} = V_{REF} \times (R_T + R_B)/R_B$$

or

$$R_T = (V_{OUT}/V_{REF} - 1) \times R_B$$

Where V_{REF}=0.8V

R_T is the top feedback resistor and R_B is bottom feedback resistor.For 1.2V output, R_T=499Ω, R_B=1K.

LDO Regulator Component Selection and LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulator is to select its maximum $R_{DS(ON)}$ based on the input to output dropout voltage and maximum load current.

For V_{OUT2}=2.5V, $V_{IN(LDO)}$=3.3V and I_{OUT2}=2A:

$$R_{DS(ON)MAX} = (V_{IN(LDO)} - V_{OUT2})/I_{OUT2}$$
$$R_{DS(ON)MAX} = (3.3V - 2.5V)/2.0A = 0.4\Omega$$

Note that the MOSFET's $R_{DS(ON)}$ increases with temperature, the calculated $R_{DS(ON)}$ has to be divided by the $R_{DS(ON)}$ temperature coefficienct (about 1.5) in order to get typical $R_{DS(ON)}$.

IRLR2703s from Internation Rectifier with D2 package, 30V, V_{DS} logic drive and 65mΩ is good enough to meet the requirement.

To select the heat sink for the LDO MOSFET, the first step is to calculate the maximum power dissipation of the device:

$$P_D = (V_{IN(LDO)} - V_{OUT}) \times I_{OUT}$$
$$P_D = (3.3V - 2.5V) \times 2A = 1.4W$$

The junction temperature of MOSFET can be estimated by the following formula:

$$T_J = T_A + P_D \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$$

T_J should be < $T_{J(MAX)}$ @ 150°C

Where:

T_J = the estimated junction temperature.

T_A = the ambient temperature.

P_D = the power disspation.

$R_{\theta JC}$ = the thermal resistance from junction to case.

$R_{\theta CS}$ = the thermal resistance from case to heat sink.

$R_{\theta SA}$ = the thermal resistance from heat sink to ambient.

The required thermal resistance of heat sink should be

$$R_{\theta SA} < (T_J - T_A)/P_D - R_{\theta JC} - R_{\theta CS}$$

In this example, the MOSFET is mounted in the copper area more than 1 square inch. The estimated junction temperaure is:

$$T_J = T_A + P_D \times R_{\theta JA}$$

Where $R_{\theta JA}$ is the thermal resistance from junction to ambient with PCB mounted.

For IRLR2703s, $R_{\theta JA}$=50°C/W, Assume:

$$T_A = 35°C$$
$$T_J = 35 + 1.5W \times 50°C/W = 110°C < 150°C$$

The thermal managment can meet the requirement.

VccLDO Selection

For LDO, the LDO controller supply voltage has to satisfy the following:

$$V_{CC(LDO)} > V_{LDO(OUT)MAX} + V_{GS(TH)MIN} + 2V_{BE}$$

Where:

$V_{LDO(OUT)MAX}$ is the maximum output voltage

$V_{GS(TH)MIN}$ is the minimum LDO MOSFET gate threshold voltage

V_{BE} is the diode drop, approximately 0.6V

For this example, $V_{GS(TH)MIN}$ of MOSFET IRLR2703s, is 1V. Then:

$$V_{CC(LDO)} > 2.5V + 1V + 2 \times 0.6V = 4.7V$$

Select V_{CCLDO}=12V for proper power sequence

LDO Feedback Resistor Selection

The output of LDO is determined by:

$$V_{OUT} = V_{REF} \times (R_T + R_B)/R_B$$

Where:

V_{REF}=0.8V

R_T is the top feedback resistor and R_B is bottom feedback resistor.

For 2.5V output, if R_B=1K then:

$$R_T = (V_{OUT}/V_{REF} - 1) \times R_B = (2.5/0.8 - 1) \times 1K = 2.12K$$

Select Rt=2.15K

LDO Soft-Start Capacitor

The soft-start capacitor can be estimated from equation (1). Select start up time as 2ms:

$$C_{SS(LDO)} = 20\mu A \times t_{START} = 20\mu A \times 2ms = 0.04\mu F$$

Select C12=$C_{SS(LDO)}$=33nF

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

APPLICATION EXPERIMENTAL WAVEFORMS

for Application Circuit in Figures 1 and 3

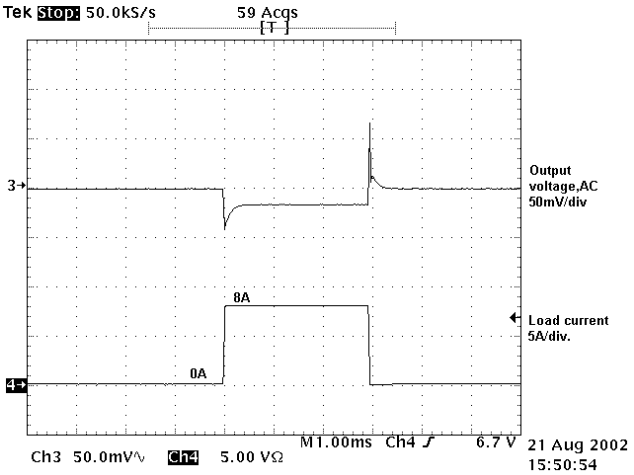


Figure 26 - Transient response with 8A load.

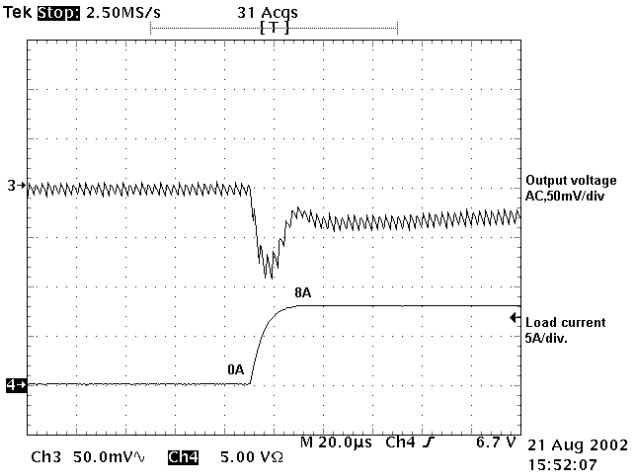


Figure 27 - Transient response (zoomed).

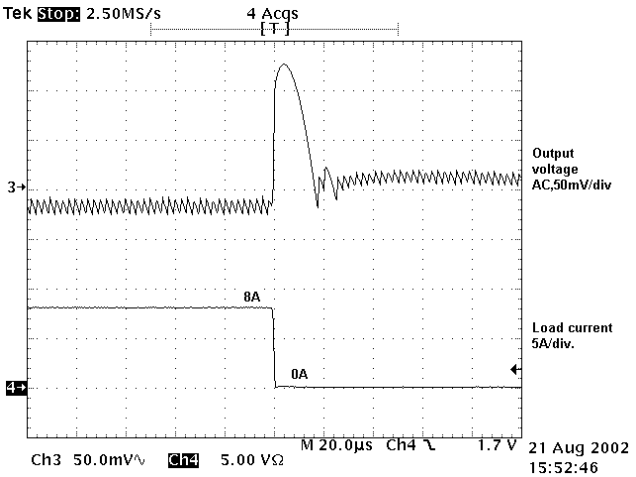


Figure 28 - Transient response (zoomed).

TYPICAL APPLICATIONS

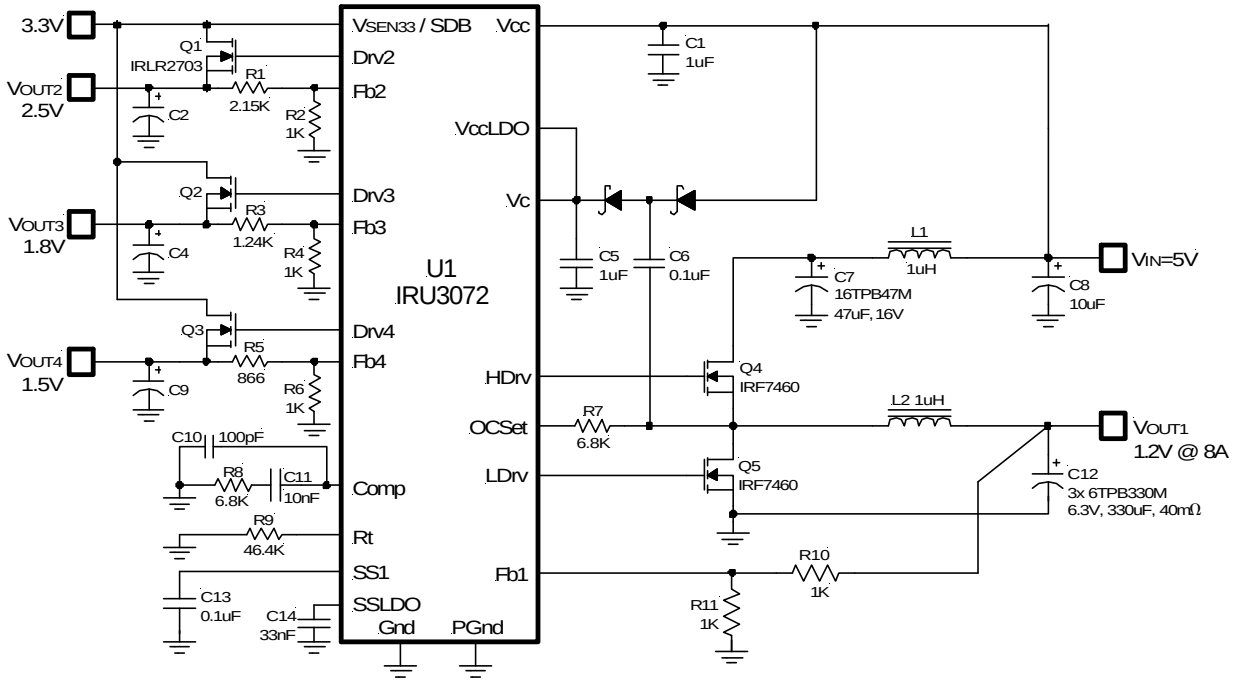


Figure 29 - IRU3072 typical application with one bus input voltage V_{CC}=V_{BUS}=5V and 3.3V for LDO.

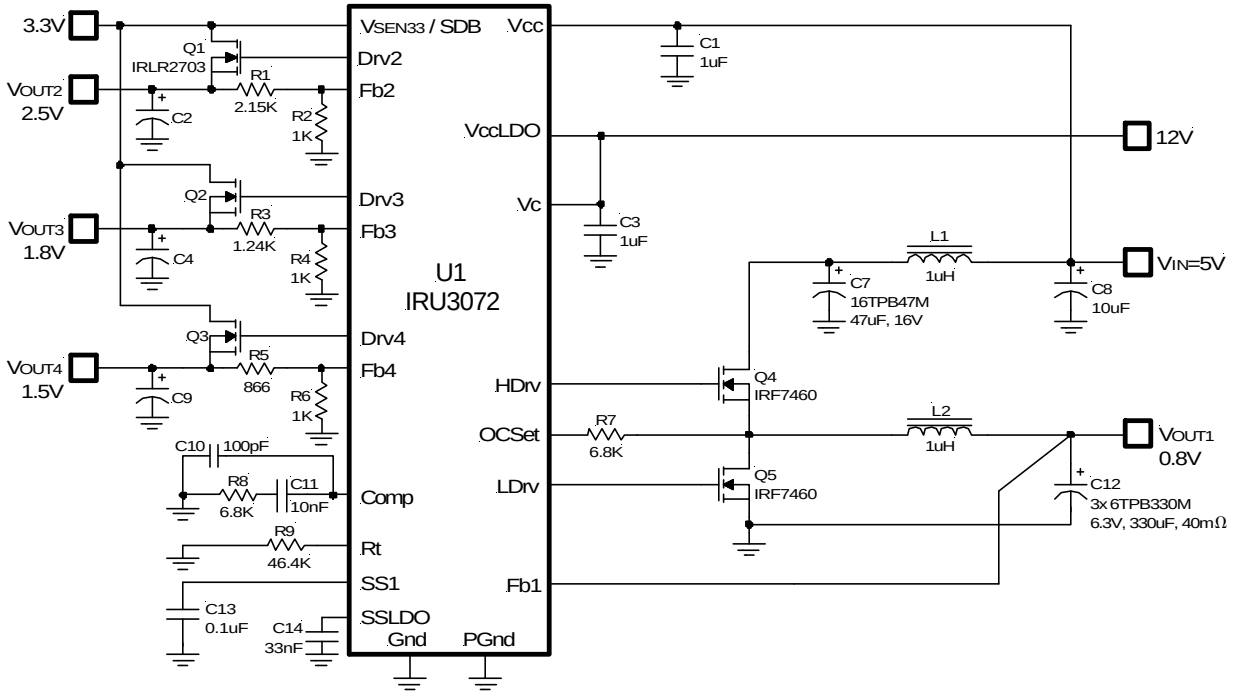


Figure 30 - IRU3072 Typical application with 5V_{BUS} input and 12V for the driver (charge pump is saved).

TYPICAL APPLICATIONS

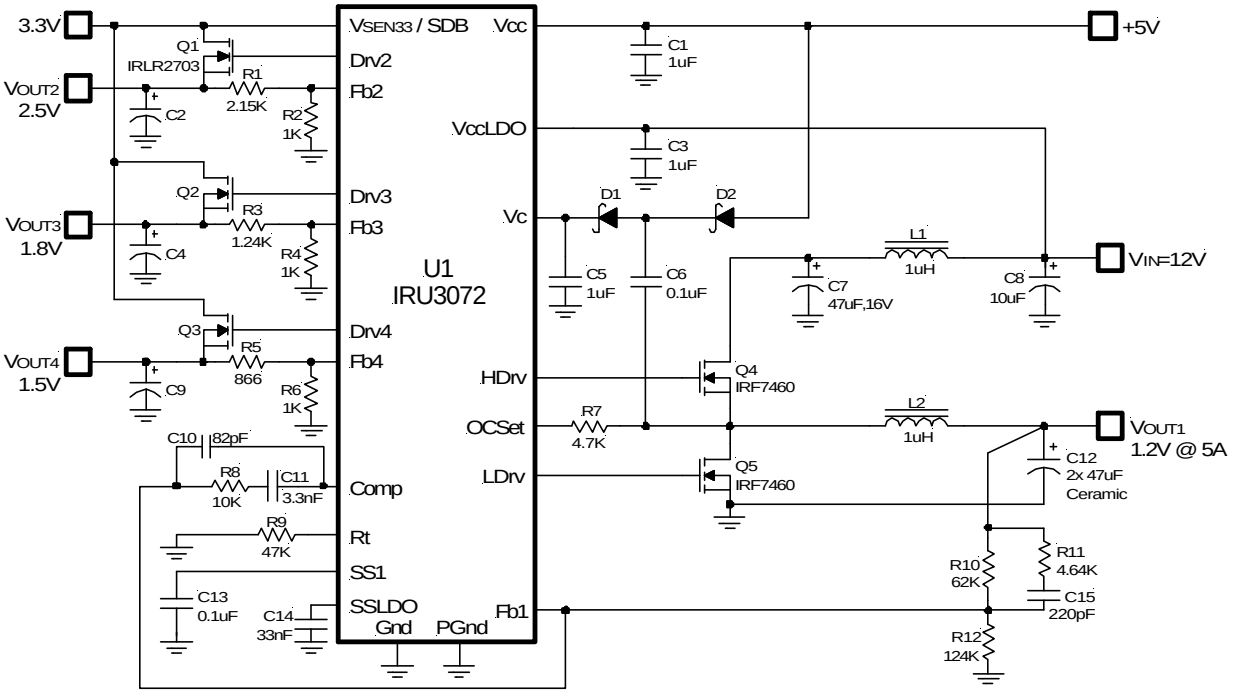


Figure 31 - IRU3072 typical application with ceramic capacitor output.

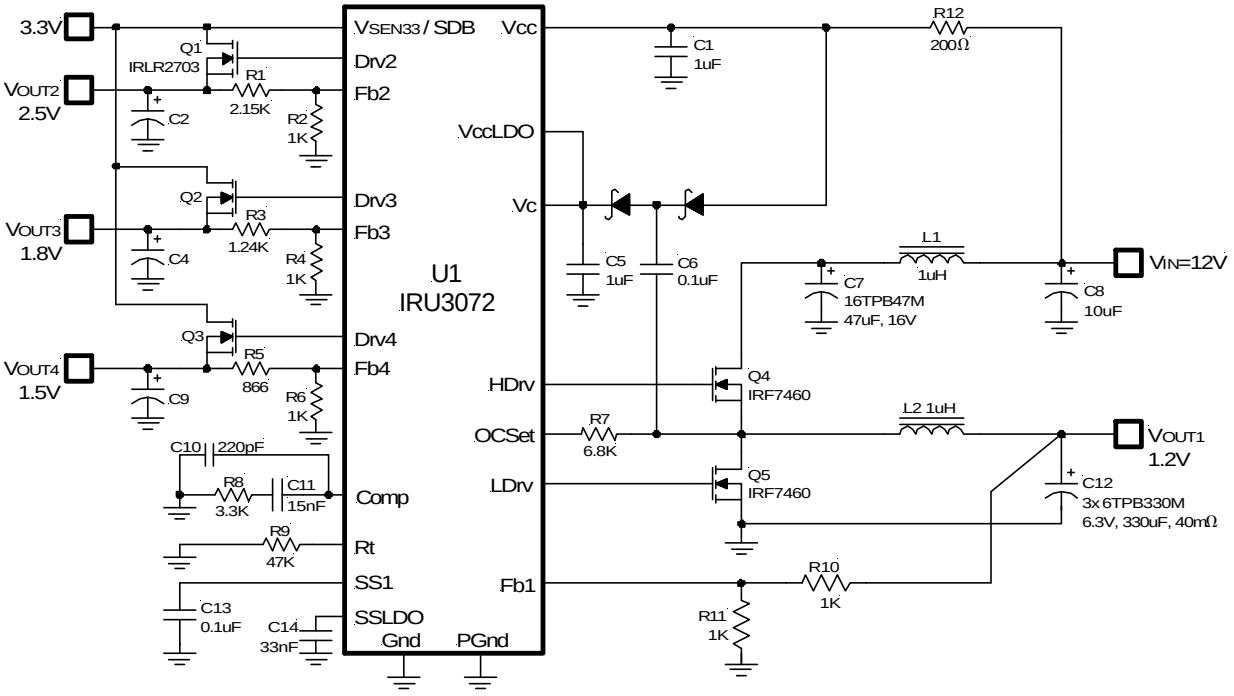


Figure 32 - IRU3072 typical application with one bus input voltage V_{CC}=V_{BUS}=12V and 3.3V for LDO.

TYPICAL APPLICATION

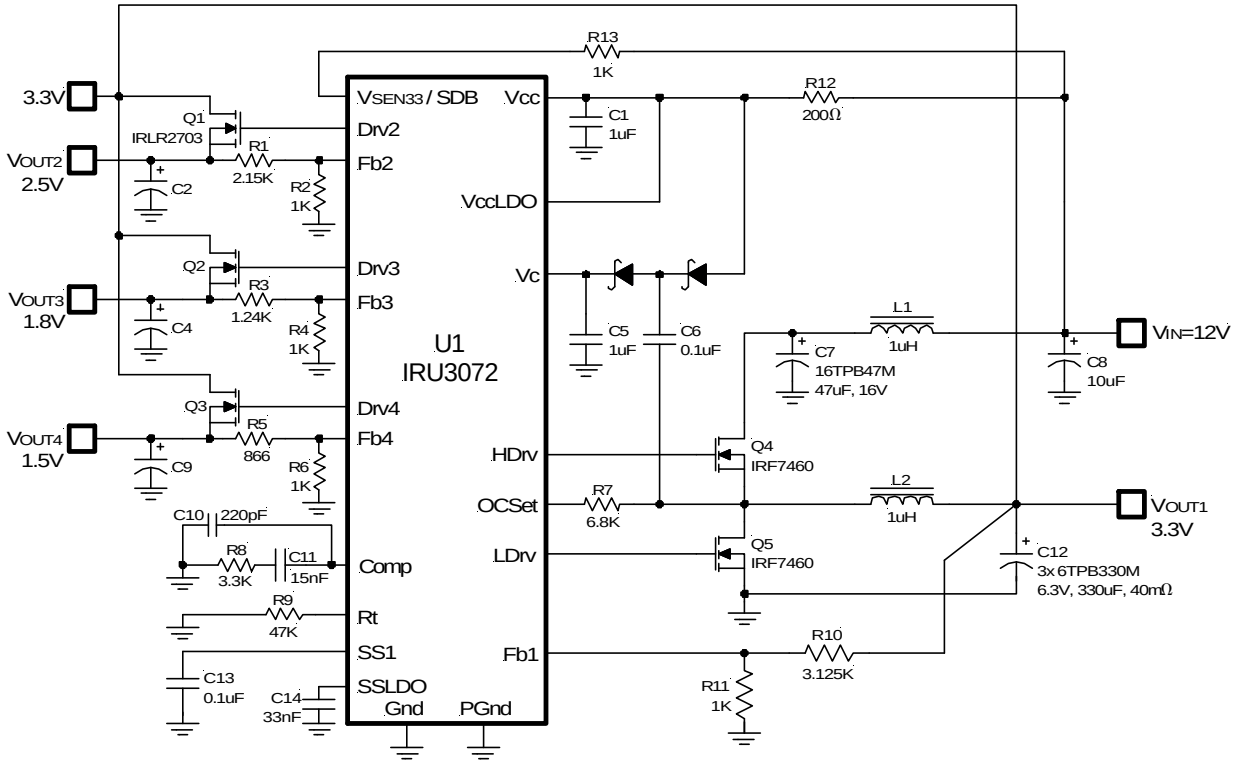
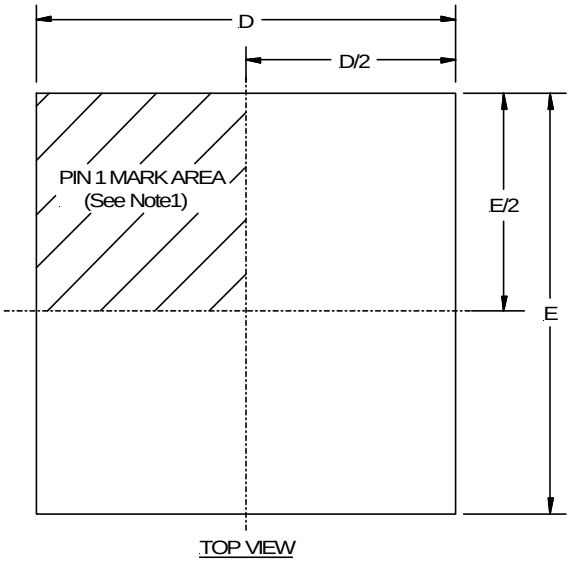
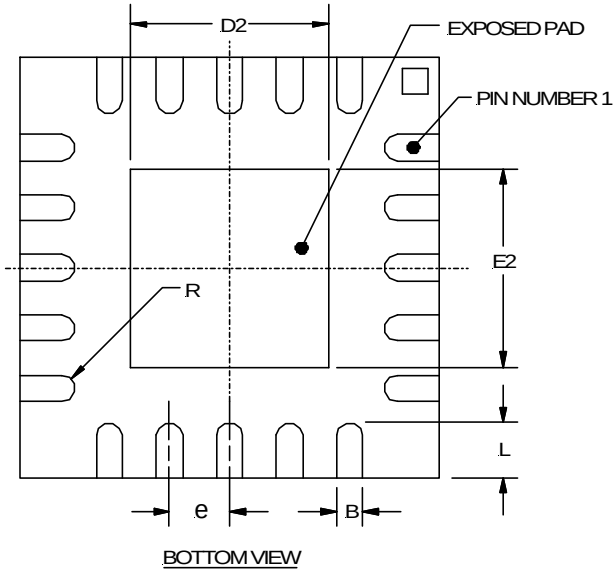
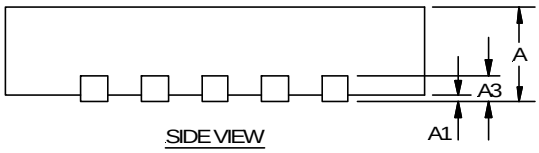


Figure 33 - IRU3072 typical application with one bus input voltage $V_{CC}=V_{BUS}=12V$ to generate all LDO output.

(H) MLPQ Package
20-Pin







Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL DESIG	20-PIN 4x4		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		4.00 BSC	
D2	2.00	2.15	2.25
E		4.00 BSC	
E2	2.00	2.15	2.25
e		0.50 BSC	
L	0.45	0.55	0.65
R	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
H	MLPQ 4x4	20	TBD	TBD	Fig A

Feed Direction
Figure A

This product has been designed and qualified for the industrial market.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information
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