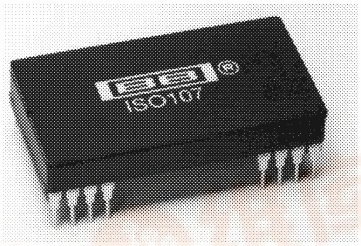
BURR - BROWN®



ISO107

High-Voltage, Internally Powered ISOLATION AMPLIFIER

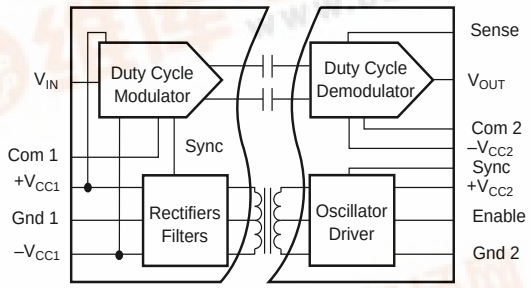
FEATURES

- SIGNAL AND POWER IN ONE TRIPLE-WIDE PACKAGE
- 8000Vpk TEST VOLTAGE
- 2500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- BIOMEDICAL INSTRUMENTATION
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION

ISO107 BLOCK DIAGRAM



DESCRIPTION

The ISO107 isolation amplifier provides both signal and power across an isolation barrier. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 2500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL544 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO107 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-898C Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage (1)					
AC, 60Hz	T_{MIN} to T_{MAX}	2500			Vrms
DC	T_{MIN} to T_{MAX}	3500			VDC
Test Breakdown, AC, 60Hz	10s	8000			Vpk
Isolation-Mode Rejection	2500Vrms, 60Hz		100		dB
	2121VDC		160		dB
Barrier Impedance			10^{12} || 13		Ω || pF
Leakage Current	240Vrms, 60Hz		1.2	2	µA
GAIN					
Nominal			1		V/V
Initial Error			±0.1	±0.25	% FSR
Gain vs Temperature			±50	±120	ppm/°C
Nonlinearity			±0.01	±0.025	% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±20	±50	mV
vs Temperature			±150	±400	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		±2		mV/V
INPUT					
Voltage Range	Output Voltage in Range	±10	±15		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±15		mA
Ripple Voltage, 800kHz Carrier (See Figure 4)			20		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		µV/√Hz
FREQUENCY RESPONSE					
Small Signal Bandwidth			20		kHz
Slew Rate			1.5		V/µs
Settling Time	0.1%, –10/10V		75		µs
POWER SUPPLIES					
Rated Voltage, V_{CC2}			±15		V
Voltage Range		±10		±18	V
Input Current	I_O = ±15mA(2)		+75/–4.5		mA
Ripple Current	No Filter		10		mAp-p
	C_{IN} = 1µF		3		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	V
Output Current	Balanced Load		±15	±50	mA
	Single		30	100	mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.18		V/V
Output Voltage vs Temperature			10		mV/°C
Voltage Balance Error, $\pm V_{CC1}$			0.05		%
Voltage Ripple	No External Capacitors		10		mVp-p
Output Capacitive Load (See Figure 1)				1	µF
Sync Frequency	Sync-Pin Grounded(3)		1.6		MHz
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–25		+125	°C

NOTES: (1) Conforms to UL544 test methods. 100% tested at 2500Vrms for 1 minute. (2) For other conditions, see Performance Curve, Input Current ($+V_{CC2}$) vs Output Current. Input Current ($-V_{CC2}$) is constant at –4.5mA (typ) for all output currents. (3) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	2500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature, (soldering, 10s)	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO107	32-Pin Side-Braze Ceramic	210

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

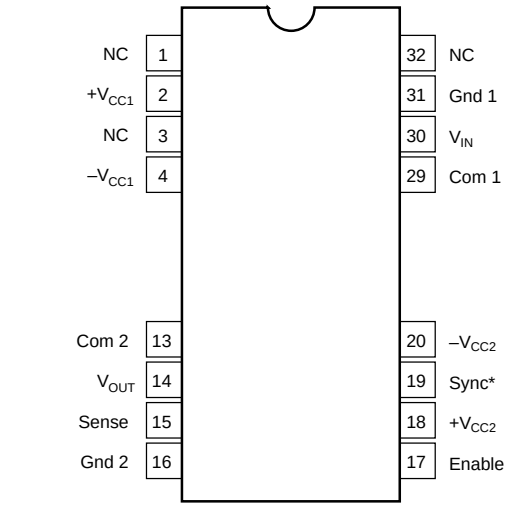
ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View **DIP**

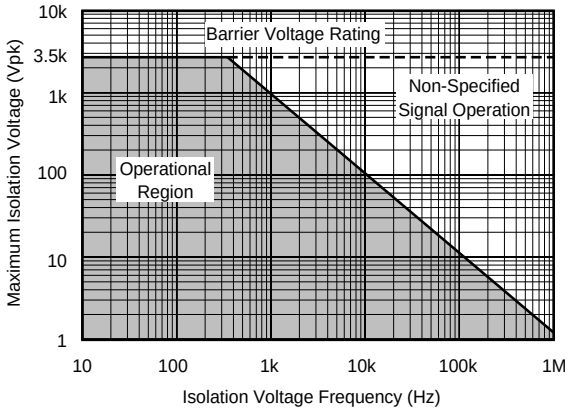


*Operation requires that this pin be grounded or driven with TTL levels.

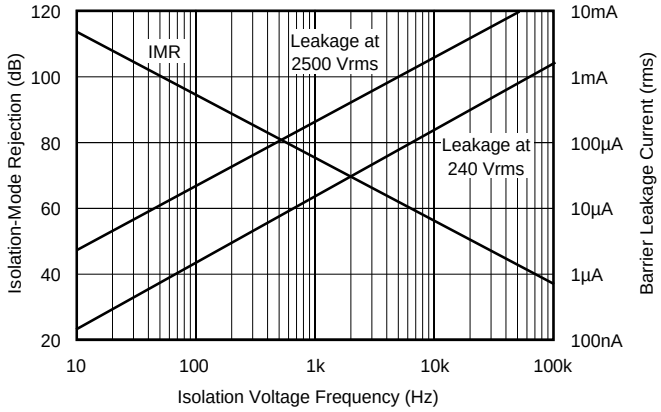
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

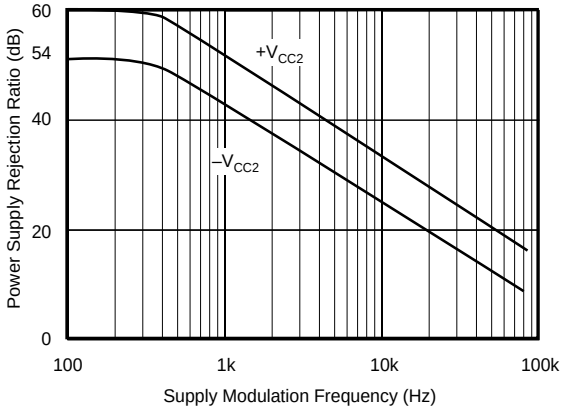
RECOMMENDED RANGE OF ISOLATION VOLTAGE



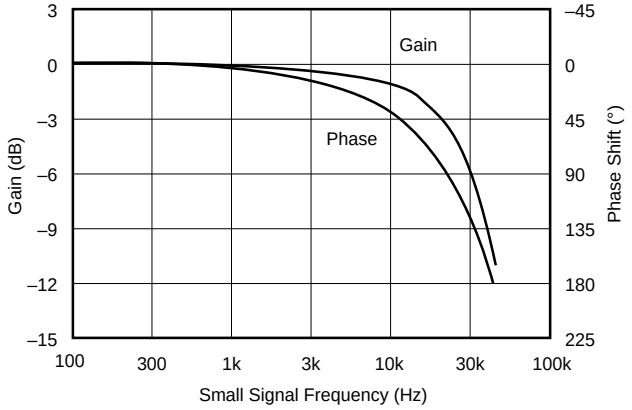
IMR/LEAKAGE vs FREQUENCY



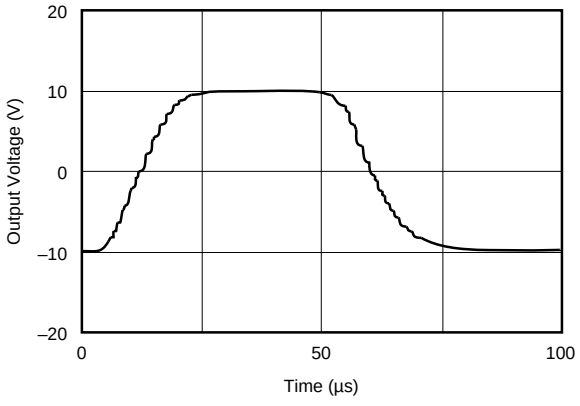
PSRR vs FREQUENCY



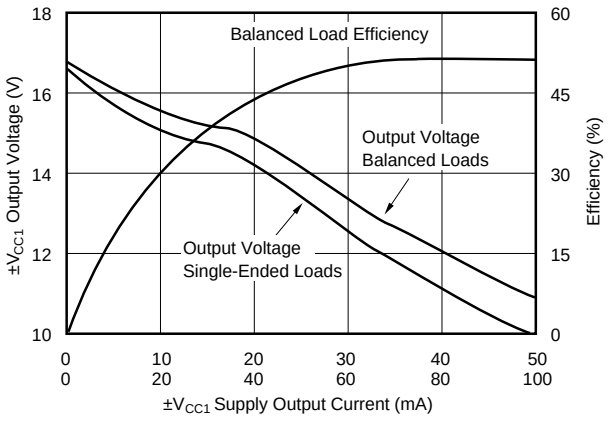
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



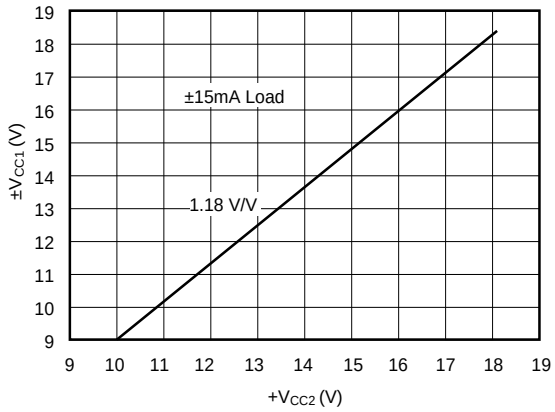
ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



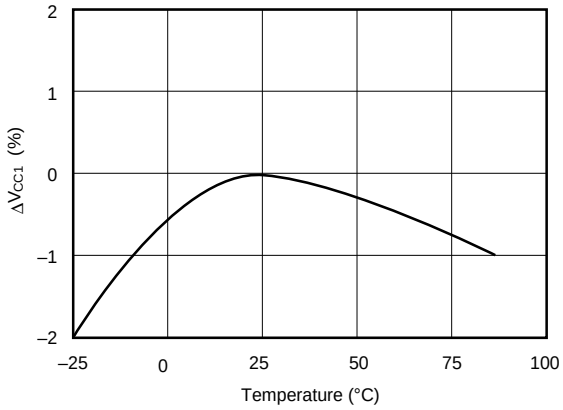
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

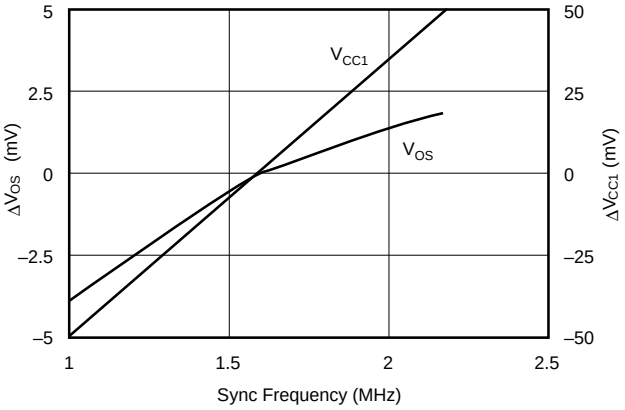
ISOLATED POWER SUPPLY LINE REGULATION



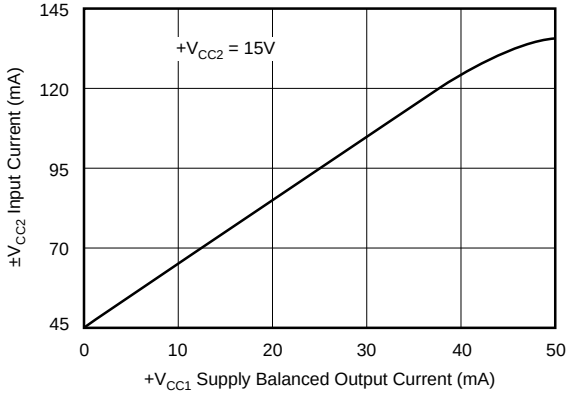
ISOLATED POWER SUPPLY VOLTAGE
vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS}
vs SYNC FREQUENCY



ISOLATED POWER SUPPLY
INPUT CURRENT vs OUTPUT CURRENT



THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminates beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$ an option recommended if more than ±15mA are drawn from the isolated supply. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO107 socket. The enable pin may be left open if the ISO107 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R1 and R1. Every 2kΩ increase in R1 will give an additional 1% adjustment range, with R2 ≥ R1. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R1 and R2 may be reserved.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in in-

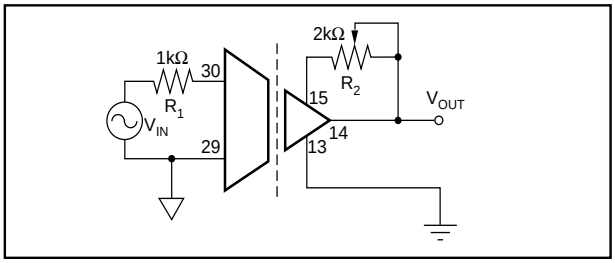


FIGURE 2a. Gain Adjust.

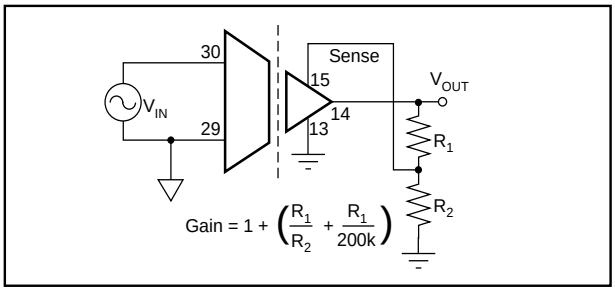


FIGURE 2b. Gain Setting.

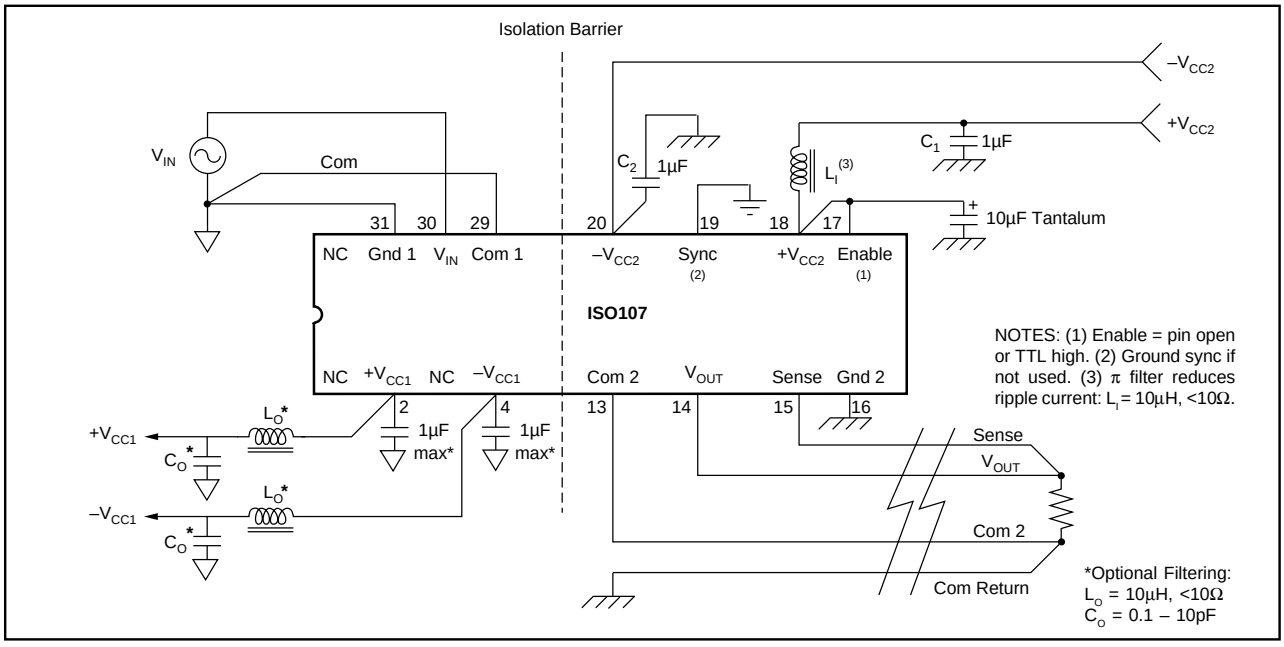


FIGURE 1. Signal and Power Connections.

verse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO107. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

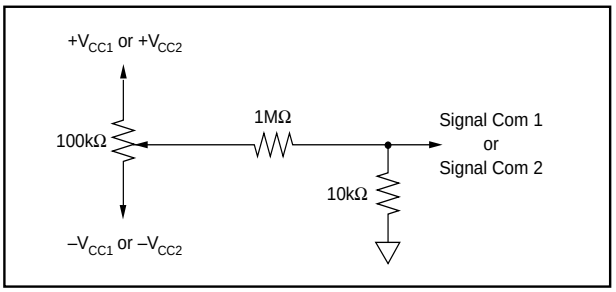


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <3mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

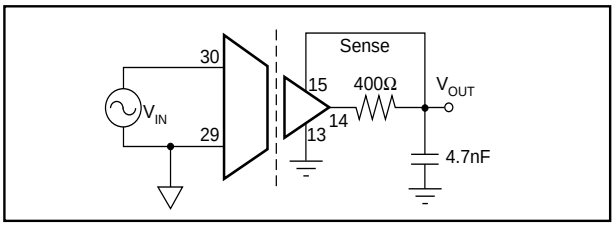


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO107s can be accomplished by connecting pin 19 of each device to an external TTL level oscillator, as shown in Figure 6. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO107 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 6. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.2MHz and 2MHz, and the duty cycle is greater than 25%.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO107 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO107 was designed to reliably operate with 2500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 8000V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 2500Vrms, 60Hz potential is applied for one minute to conform to UL544. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

APPLICATIONS

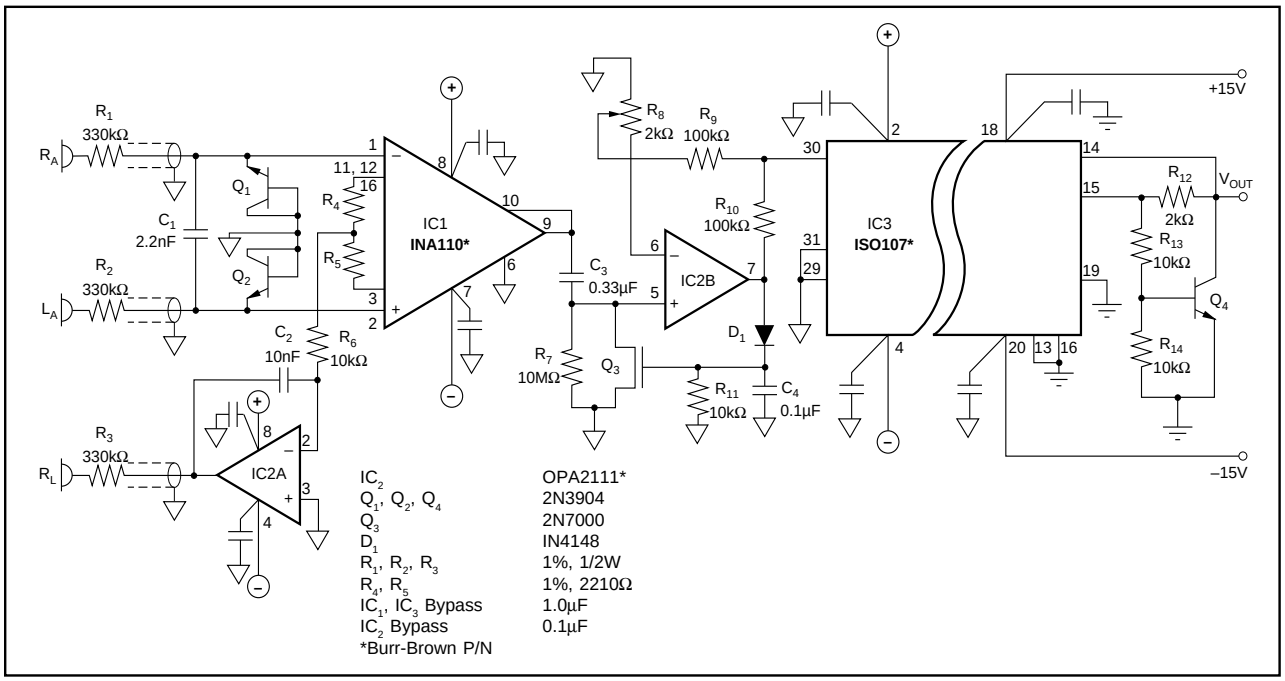


FIGURE 5. ECG Amplifier with Right Leg Drive, Defibrillator Protection, and E.S.U. Blanking.

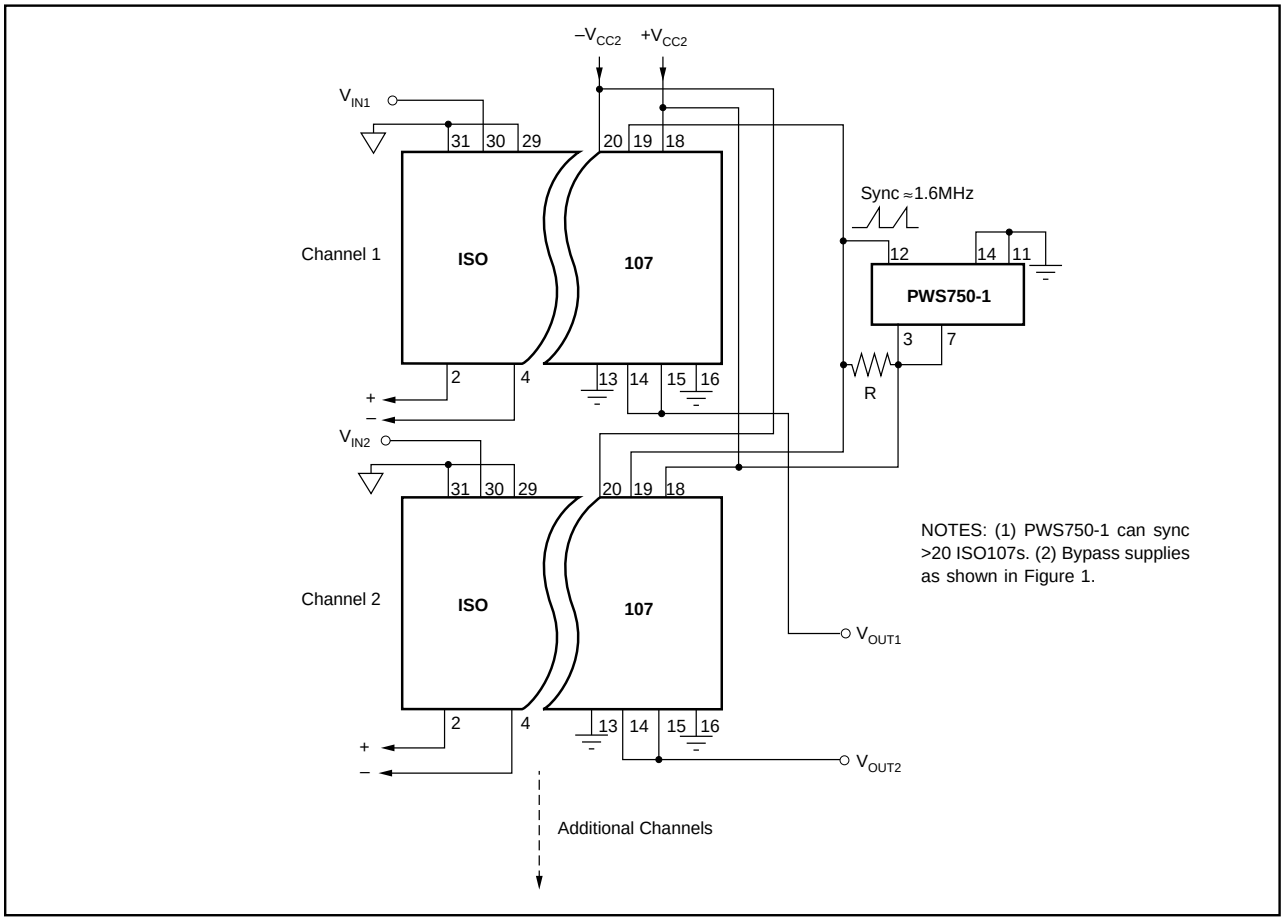


FIGURE 6. Synchronized-Multichannel Isolation.