



## ISOLATED 5-V FULL AND HALF-DUPLEX RS-485 TRANSCEIVERS

### FEATURES

- **4000-V<sub>PEAK</sub> Isolation, 560-V<sub>peak</sub> V<sub>IORM</sub>**
  - UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2), IEC 61010-1, IEC 60950-1 and CSA Approved
- **Bus-Pin ESD Protection**
  - 16 kV HBM Between Bus Pins and GND2
  - 6 kV HBM Between Bus Pins and GND1
- **1/8 Unit Load – Up to 256 Nodes on a Bus**
- **Meets or Exceeds TIA/EIA RS-485 Requirements**
- **Signaling Rates up to 20 Mbps**
- **Thermal Shutdown Protection**
- **Low Bus Capacitance – 16 pF (Typ)**
- **50 kV/μs Typical Transient Immunity**
- **Fail-safe Receiver for Bus Open, Short, Idle**
- **3.3-V Inputs are 5-V Tolerant**

### APPLICATIONS

- **Security Systems**
- **Chemical Production**
- **Factory Automation**
- **Motor/Motion Control**
- **HVAC and Building Automation Networks**
- **Networked Security Stations**

ISO3080	Full-Duplex	200 kbps
ISO3086	Full-Duplex	20 Mbps
ISO3082	Half-Duplex	200 kbps
ISO3088	Half-Duplex	20 Mbps

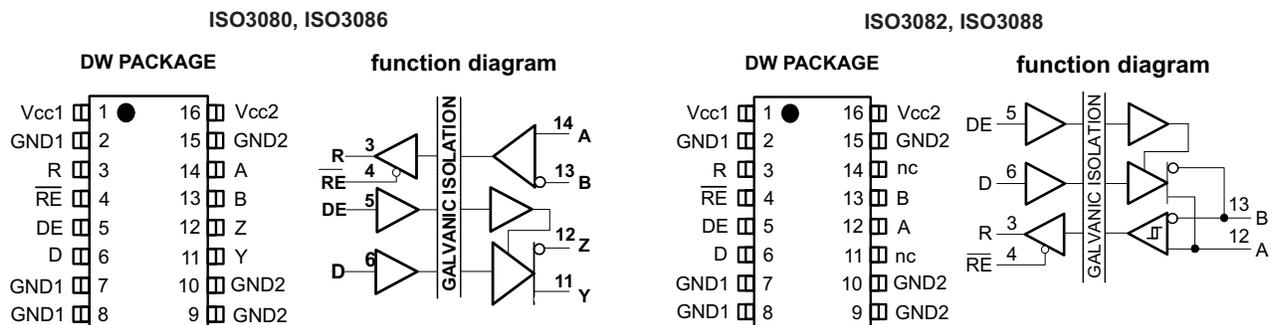
### DESCRIPTION

The ISO3080, and ISO3086 are isolated full-duplex differential line drivers and receivers while the ISO3082, and ISO3088 are isolated half-duplex differential line transceivers for TIA/EIA 485/422 applications.

These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500 V<sub>rms</sub> of isolation for 60s between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

The ISO3080, SO3082, ISO3086 and ISO3088 are qualified for use from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

				VALUE	UNIT	
$V_{CC}$	Input supply voltage, <sup>(2)</sup> $V_{CC1}$ , $V_{CC2}$			-0.3 to 6	V	
$V_O$	Voltage at any bus I/O terminal			-9 to 14	V	
$V_{IT}$	Voltage input, transient pulse, A, B, Y, and Z (through 100 $\Omega$ , see <a href="#">Figure 11</a> )			-50 to 50	V	
$V_I$	Voltage input at any D, DE or $\overline{RE}$ terminal			-0.5 to 7	V	
$I_O$	Receiver output current			$\pm 10$	mA	
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus pins and GND1	$\pm 6$	kV
				Bus pins and GND2	$\pm 16$	
		All pins	$\pm 4$			
		Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	$\pm 1$	kV
Machine Model	ANSI/ESDS5.2-1996				$\pm 200$	V
$T_J$	Maximum junction temperature			150	$^{\circ}\text{C}$	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values

## RECOMMENDED OPERATING CONDITIONS

				MIN	TYP	MAX	UNIT
$V_{CC1}$	Logic-side supply voltage <sup>(1)</sup>			3.15		5.5	V
$V_{CC2}$	Bus-side supply voltage <sup>(1)</sup>			4.5	5	5.5	V
$V_{OC}$	Voltage at either bus I/O terminal		A, B	-7		12	V
$V_{IH}$	High-level input voltage		D, DE, $\overline{RE}$	2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage			0		0.8	
$V_{ID}$	Differential input voltage		A with respect to B	-12		12	V
$R_L$	Differential input resistance			54	60		$\Omega$
$I_O$	Output current	Driver		-60		60	mA
		Receiver		-8		8	
$T_J$	Operating junction temperature			-40		85	$^{\circ}\text{C}$

- (1) For 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For 3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6V.

## SUPPLY CURRENT

over recommended operating condition (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC1}$	Logic-side supply current	$\overline{RE}$ at 0 V or $V_{CC}$ , DE at 0 V or $V_{CC1}$	3.3-V $V_{CC1}$		8	mA
		$\overline{RE}$ at 0 V or $V_{CC}$ , DE at 0 V or $V_{CC1}$	5-V $V_{CC1}$		10	
$I_{CC2}$	Bus-side supply current	$\overline{RE}$ at 0 V or $V_{CC}$ , DE at 0 V, No load			15	mA

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Differential output voltage magnitude	I <sub>O</sub> = 0 mA, no load		3	4.3	V <sub>CC</sub>	V
		R <sub>L</sub> = 54 Ω, See <a href="#">Figure 1</a>		1.5	2.3		
		R <sub>L</sub> = 100 Ω (RS-422), See <a href="#">Figure 1</a>		2	2.3		
		V <sub>test</sub> from -7 V to +12 V, See <a href="#">Figure 2</a>		1.5			
Δ V <sub>OD</sub>	Change in magnitude of the differential output voltage	See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>		-0.2	0	0.2	V
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	See <a href="#">Figure 3</a>		1	2.6	3	V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage			-0.1		0.1	
V <sub>OC(pp)</sub>	Peak-to-peak common-mode output voltage	See <a href="#">Figure 3</a>			0.5		V
I <sub>I</sub>	Input current	D, DE, V <sub>I</sub> at 0 V or V <sub>CC1</sub>		-10		10	μA
I <sub>OZ</sub>	High-impedance state output current	ISO3082 ISO3088	See receiver input current				μA
		ISO3080 ISO3086	V <sub>Y</sub> or V <sub>Z</sub> = 12 V, V <sub>CC</sub> = 0 V or 5 V, DE = 0 V	Other input at 0 V			
V <sub>Y</sub> or V <sub>Z</sub> = -7 V, V <sub>CC</sub> = 0 V or 5 V, DE = 0 V			-1				
I <sub>OS</sub>	Short-circuit output current	V <sub>A</sub> or V <sub>B</sub> at -7 V		-200		200	mA
		V <sub>A</sub> or V <sub>B</sub> at 12 V					
CMTI	Common-mode transient immunity	V <sub>I</sub> = V <sub>CC1</sub> or 0 V, See <a href="#">Figure 12</a>		25	50		kV/μs

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	ISO3080/82			0.7	1.3	ns	
		ISO3086/88			25	45		
PWD <sup>(1)</sup>	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	ISO3080/82		See <a href="#">Figure 4</a>	20	200	ns	
		ISO3086/88			3	7.5		
t <sub>r</sub> , t <sub>f</sub>	Differential output signal rise and fall time	ISO3080/82			0.5	0.9	1.5	μs
		ISO3086/88			7	15		ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Propagation delay, high-impedance-to-high-level output Propagation delay, high-impedance-to-low-level output	ISO3080/82	50% V <sub>O</sub>	See <a href="#">Figure 5</a> and <a href="#">Figure 6</a> , DE at 0 V	2.5	7	μs	
		ISO3086/88	90% V <sub>O</sub>		1.8			
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Propagation delay, high-level-to-high-impedance output Propagation delay, low-level to high-impedance output	ISO3080/82			95	225	ns	
		ISO3086/88			25	55		

(1) Also known as pulse skew

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$		-85	-10	mV
$V_{IT(-)}$	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-200	-115		mV
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			30		mV
$V_{OH}$	High-level output voltage	$V_{ID} = 200 \text{ mV}$ , $I_O = -8 \text{ mA}$ , See Figure 7	3.3-V $V_{CC1}$	$V_{CC1} - 0.4$	3.1	V
			5-V $V_{CC1}$	4	4.8	
$V_{OL}$	Low-level output voltage	$V_{ID} = -200 \text{ mV}$ , $I_O = 8 \text{ mA}$ , See Figure 7	3.3-V $V_{CC1}$	0.15	0.4	V
			5-V $V_{CC1}$	0.15	0.4	
$I_{O(Z)}$	High-impedance state output current	$V_I = -7 \text{ to } 12 \text{ V}$ , Other input = 0 V	-1		1	$\mu\text{A}$
$I_I$	Bus input current	Other input at 0 V	$V_A \text{ or } V_B = 12 \text{ V}$	0.04	0.1	mA
			$V_A \text{ or } V_B = 12 \text{ V}$ , $V_{CC} = 0$	0.06	0.13	
			$V_A \text{ or } V_B = -7 \text{ V}$	-0.1	-0.04	
			$V_A \text{ or } V_B = -7 \text{ V}$ , $V_{CC} = 0$	-0.05	-0.03	
$I_{IH}$	High-level input current, $\overline{RE}$	$V_{IH} = 2 \text{ V}$	-10		10	$\mu\text{A}$
$I_{IL}$	Low-level input current, $\overline{RE}$	$V_{IL} = 0.8 \text{ V}$	-10		10	$\mu\text{A}$
$R_{ID}$	Differential input resistance	A, B	48			k $\Omega$
$C_D$	Differential input capacitance	Test input signal is a 1.5 MHz sine wave with 1Vpp amplitude. CD is measured across A and B.		7		pF

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay	See Figure 8		90	125	ns
PWD <sup>(1)</sup>	Pulse width distortion [ $t_{PHL} - t_{PLH}$ ]		4	12		
$t_r$ , $t_f$	Output signal rise and fall time		1			
$t_{PZH}$ , $t_{PZL}$	Propagation delay, high-level-to-high-impedance output Propagation delay, high-impedance-to-high-level output	See Figure 9, DE at 0 V			22	ns
$t_{PHZ}$ , $t_{PLZ}$	Propagation delay, high-impedance-to-low-level output Propagation delay, low-level-to-high-impedance output	See Figure 10, DE at 0 V			22	ns

(1) Iso known as pulse skew.

## PARAMETER MEASUREMENT INFORMATION

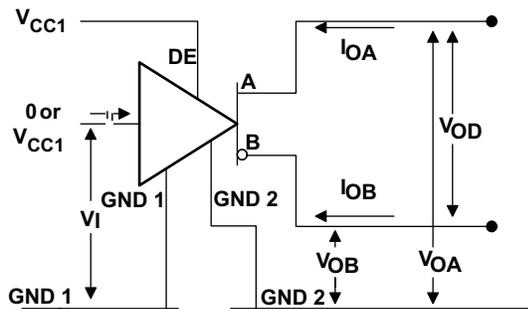


Figure 1. Driver  $V_{OD}$  Test and Current Definitions

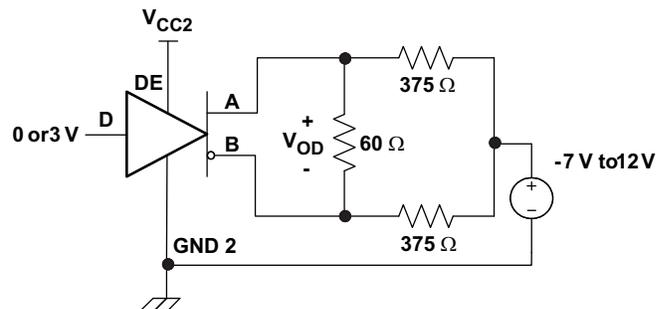


Figure 2. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

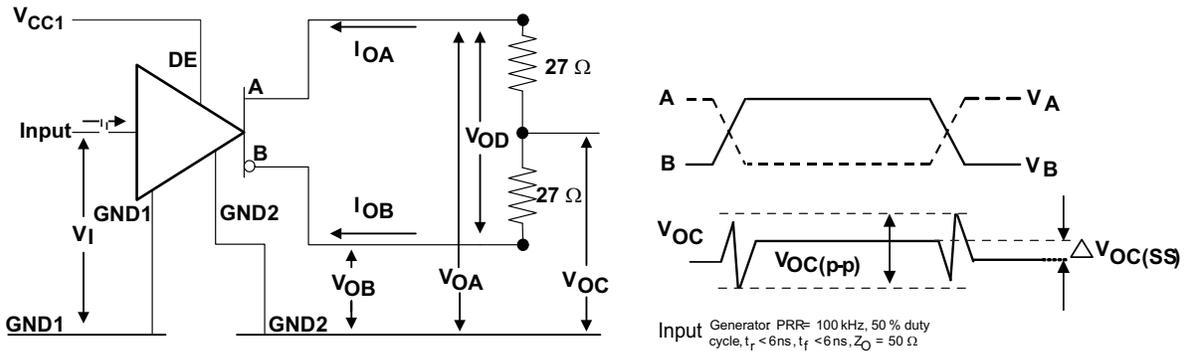


Figure 3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

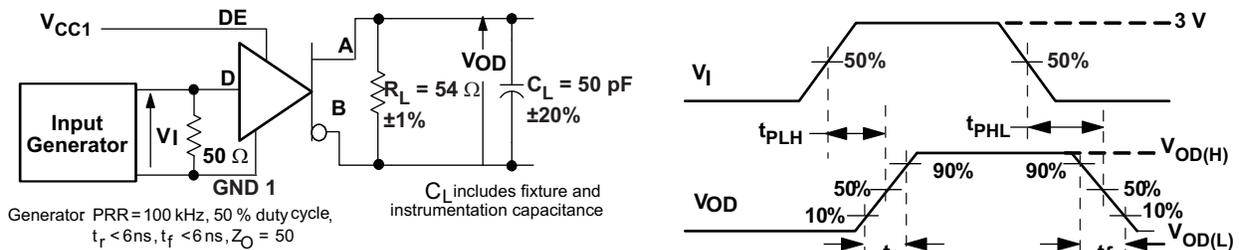


Figure 4. Driver Switching Test Circuit and Voltage Waveforms

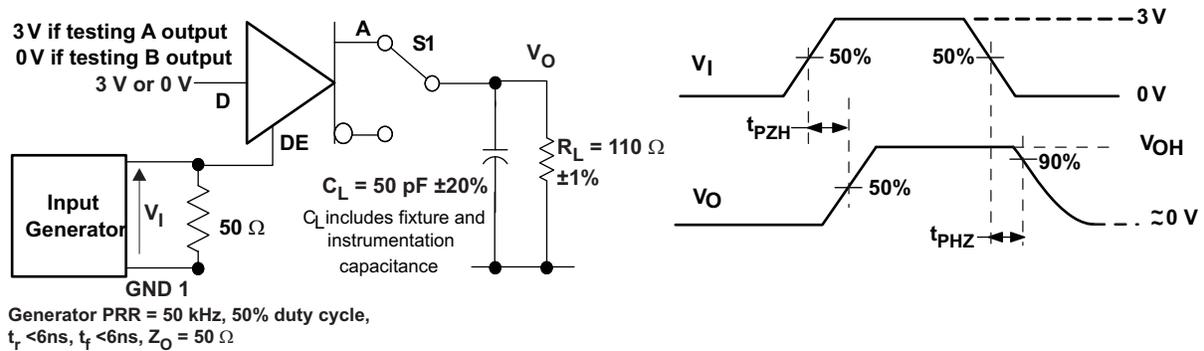


Figure 5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

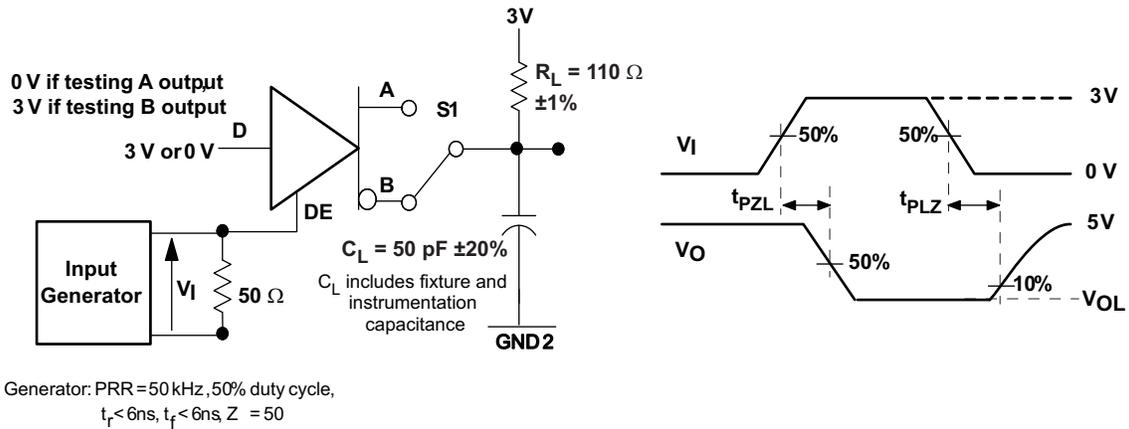


Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

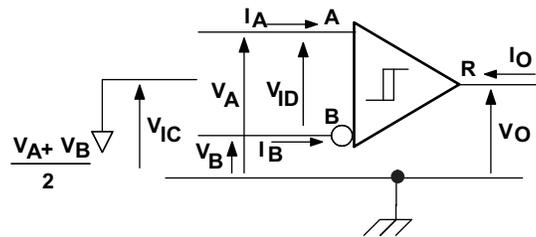


Figure 7. Receiver Voltage and Current Definitions

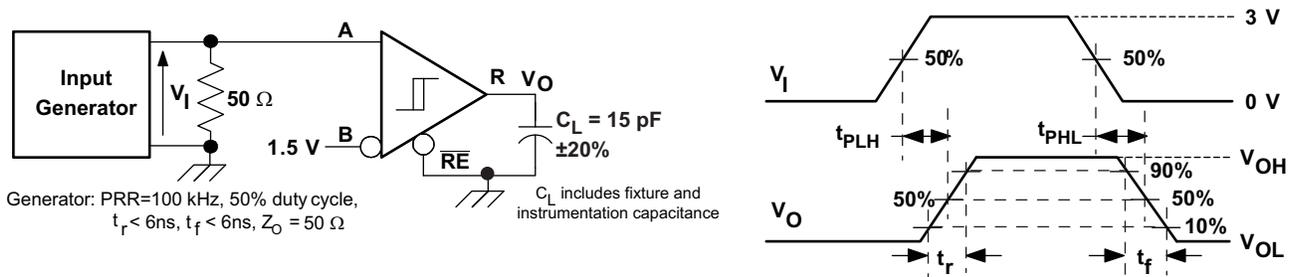


Figure 8. Receiver Switching Test Circuit and Waveforms

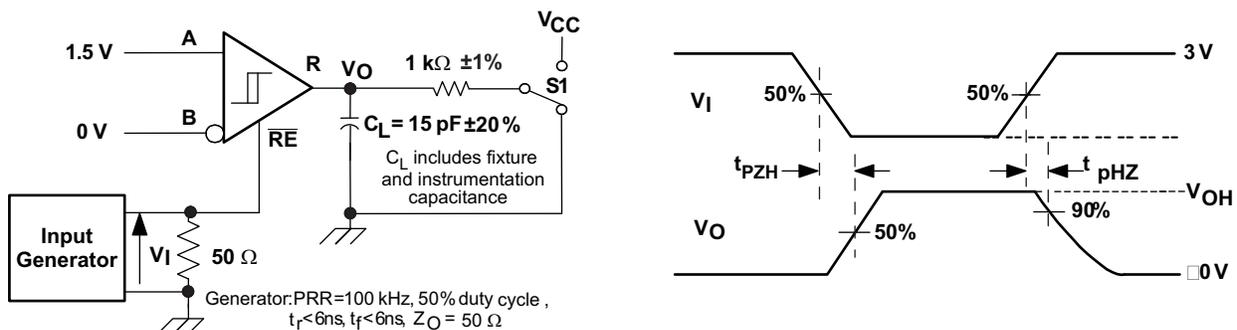


Figure 9. Receiver Enable Test Circuit and Waveforms, Data Output High

PARAMETER MEASUREMENT INFORMATION (continued)

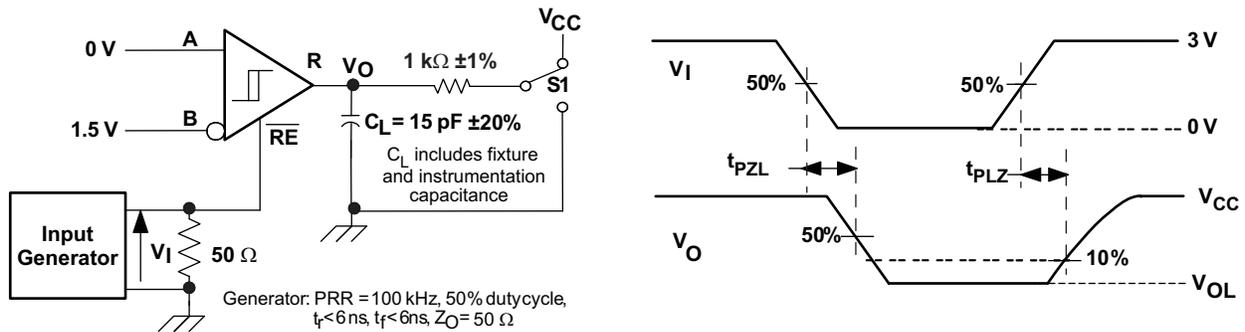
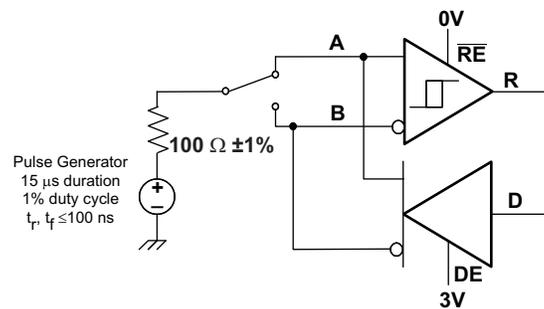


Figure 10. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only.  
Data stability at the R output is not specified.

Figure 11. Transient Over-Voltage Test Circuit

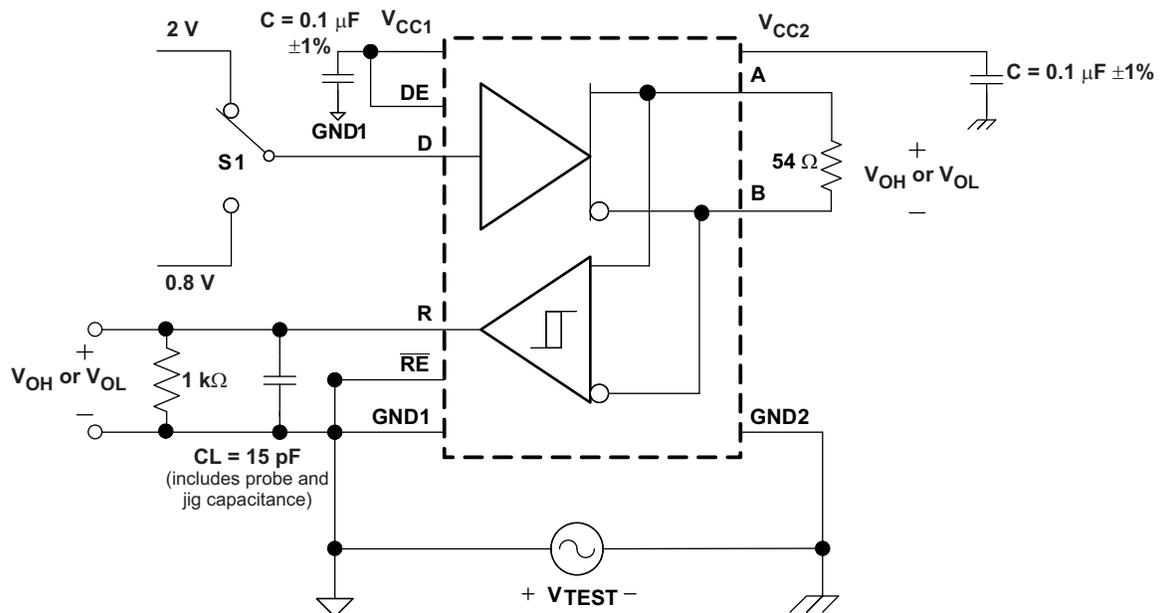


Figure 12. Half-Duplex Common-Mode Transient Immunity Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

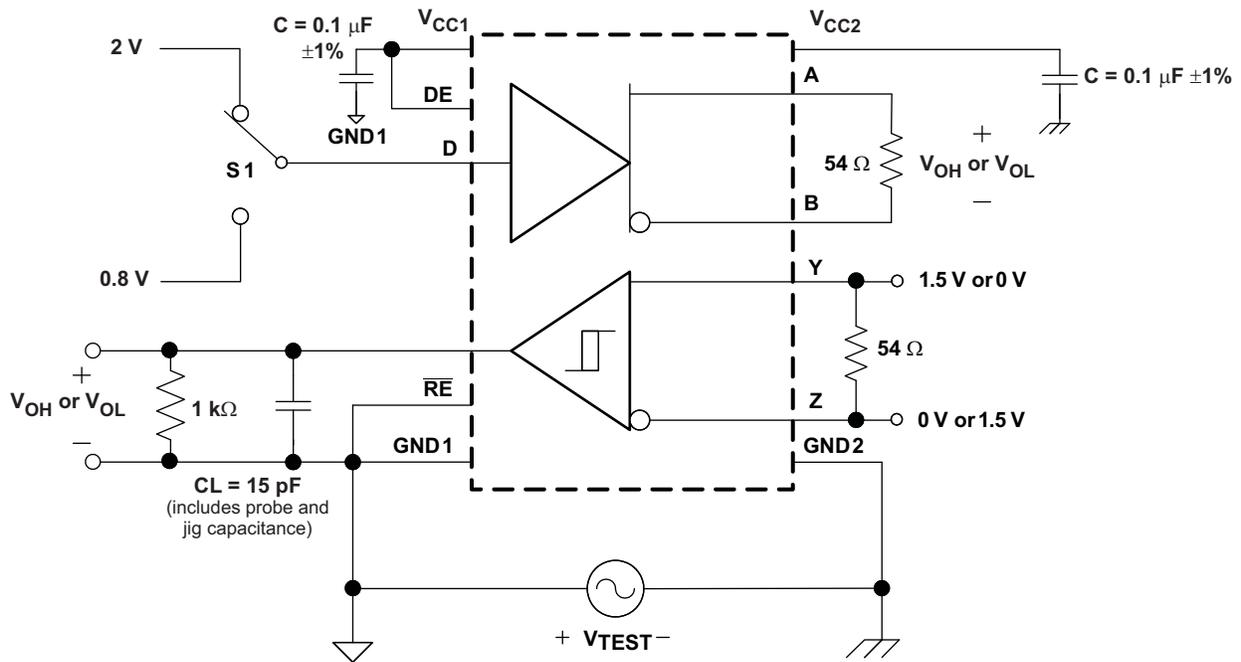


Figure 13. Full-Duplex Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

Table 1. Driver Function Table

V <sub>CC1</sub>	V <sub>CC2</sub>	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS	
				Y	Z
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

Table 2. Receiver Function Table

V <sub>CC1</sub>	V <sub>CC2</sub>	DIFFERENTIAL INPUT V <sub>ID</sub> = (V <sub>A</sub> - V <sub>B</sub> )	ENABLE (RE)	OUTPUT (R)
PU	PU	-0.01 V ≤ V <sub>ID</sub>	L	H
PU	PU	-0.2 V < V <sub>ID</sub> < -0.01 V	L	?
PU	PU	V <sub>ID</sub> ≤ -0.2 V	L	L
PU	PU	X	H	Z
PU	PU	X	OPEN	Z
PU	PU	Open circuit	L	H

**Table 2. Receiver Function Table (continued)**

V <sub>CC1</sub>	V <sub>CC2</sub>	DIFFERENTIAL INPUT V <sub>ID</sub> = (V <sub>A</sub> – V <sub>B</sub> )	ENABLE ( $\overline{RE}$ )	OUTPUT (R)
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Z
PU	PD	X	L	H

## PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER <sup>(1)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R <sub>IO</sub>	Isolation resistance	Input to output, V <sub>IO</sub> = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		>10 <sup>12</sup>		Ω
C <sub>IO</sub>	Barrier capacitance Input to output	V <sub>I</sub> = 0.4 sin (4E6πt)		2		pF
C <sub>I</sub>	Input capacitance to ground	V <sub>I</sub> = 0.4 sin (4E6πt)		2		pF

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

## IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV
	Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-III
	Rated mains voltage ≤ 400 V <sub>RMS</sub>	I-II

## IEC 60747-5-2 INSULATION CHARACTERISTICS<sup>(1)</sup>

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V <sub>IOORM</sub>	Maximum working insulation voltage		560	V
V <sub>PR</sub>	Input to output test voltage	Method b1, V <sub>PR</sub> = V <sub>IOORM</sub> × 1.875, 100% Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V <sub>IO TM</sub>	Transient overvoltage	t = 60 s	4000	V
R <sub>S</sub>	Insulation resistance	V <sub>IO</sub> = 500 V at T <sub>S</sub>	>10 <sup>9</sup>	Ω
	Pollution degree		2	

- (1) Climatic Classification 40/125/21

## REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program <sup>(1)</sup>
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested  $\geq 3000$  VRMS for 1 second in accordance with UL 1577.

## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER			MIN	TYP	MAX	UNIT
$I_S$	Safety input, output, or supply current	DW-16	$\theta_{JA} = 212^\circ\text{C/W}$ , $V_I = 5.5\text{ V}$ , $T_J = 170^\circ\text{C}$ , $T_A = 25^\circ\text{C}$		210	mA
$T_S$	Maximum case temperature	DW-16			150	$^\circ\text{C}$

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Junction-to-Air	Low-K Thermal Resistance <sup>(1)</sup>	168			$^\circ\text{C/W}$
		High-K Thermal Resistance	96.1			
$\theta_{JB}$	Junction-to-Board Thermal Resistance		61			$^\circ\text{C/W}$
$\theta_{JC}$	Junction-to-Case Thermal Resistance		48			$^\circ\text{C/W}$
$P_D$	Device Power Dissipation	$V_{CC1} = V_{CC2} = 5.25\text{ V}$ , $T_J = 150^\circ\text{C}$ , $C_L = 15\text{ pF}$ , Input a 20 MHz 50% duty cycle square wave	220			mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

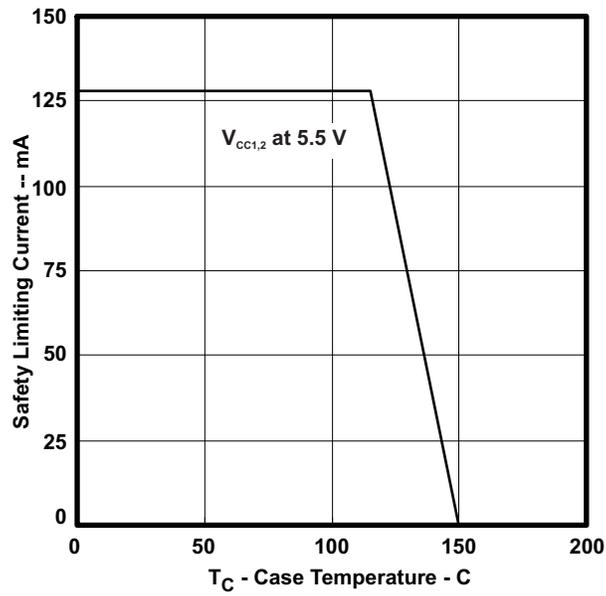
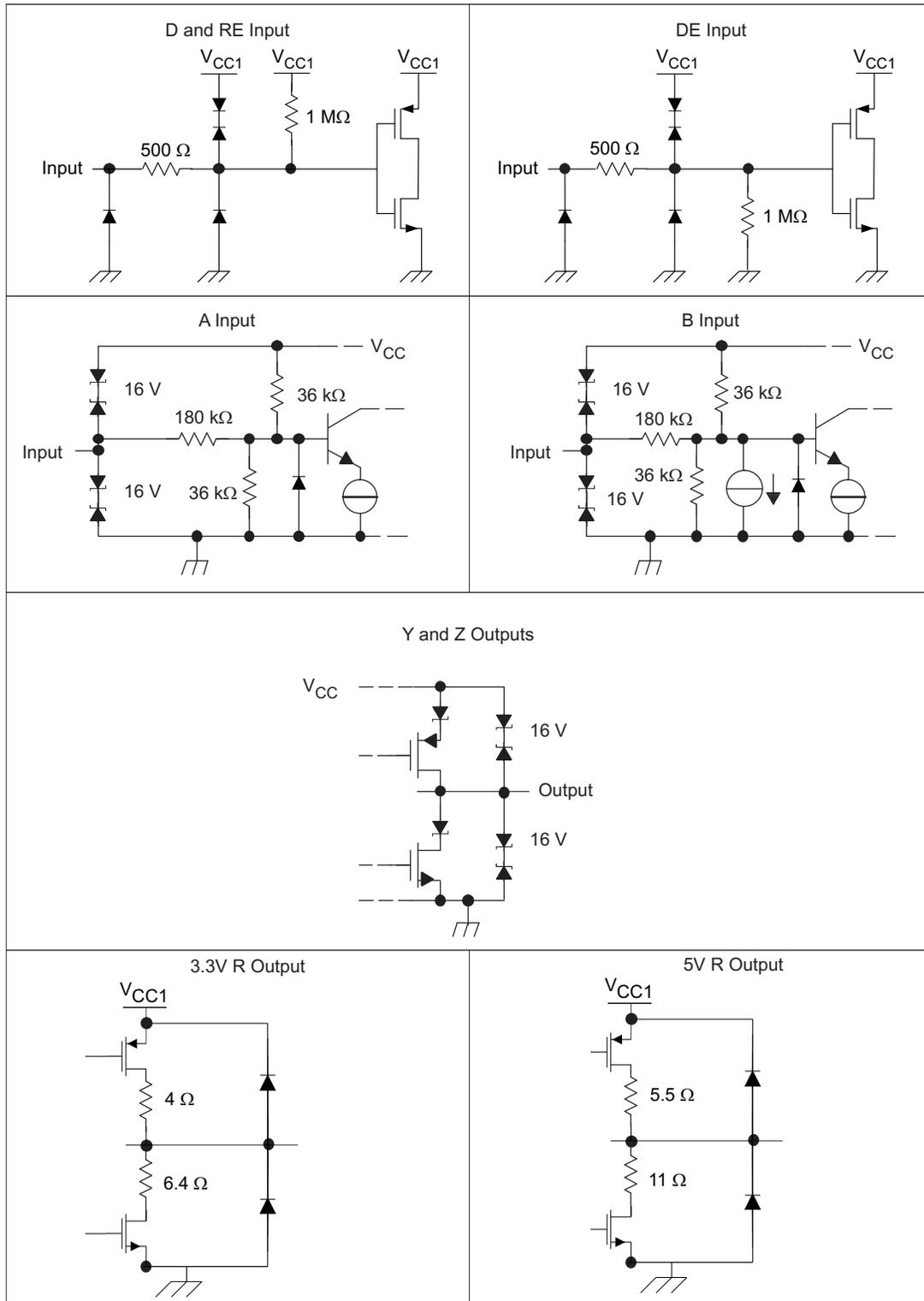


Figure 14. DW-16  $\theta_{JC}$  Thermal Derating Curve per IEC 60747-5-2

EQUIVALENT CIRCUIT SCHEMATICS



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ISO3080DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3080DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3080DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3080DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3082DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3082DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3082DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3082DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3086DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3086DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3086DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3086DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3088DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3088DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3088DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO3088DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

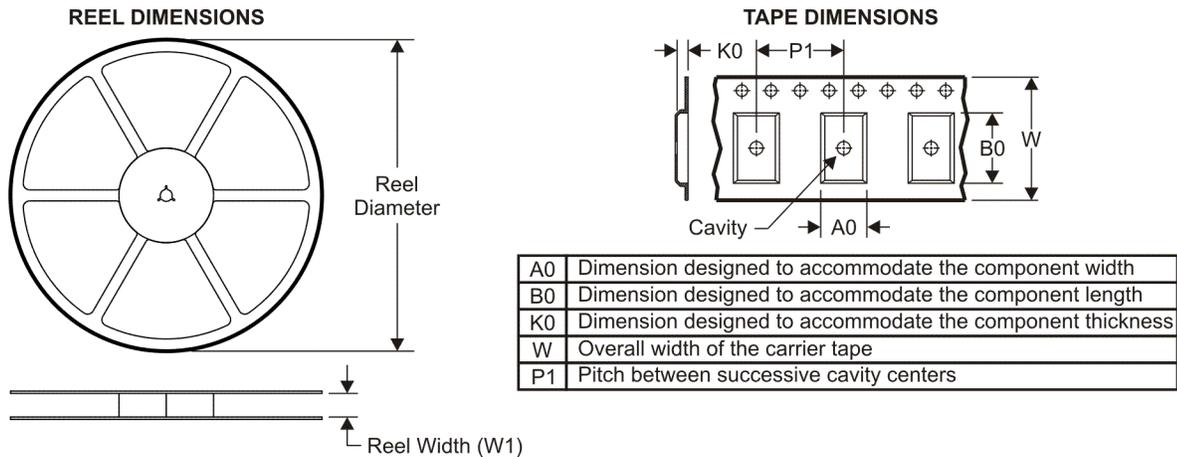
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

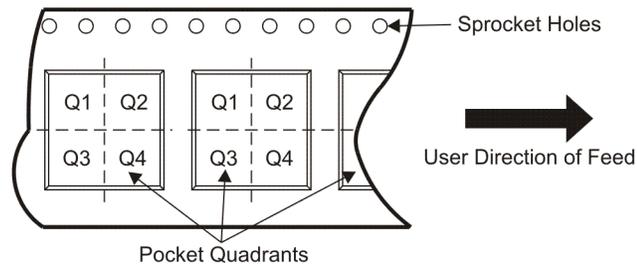
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## TAPE AND REEL INFORMATION



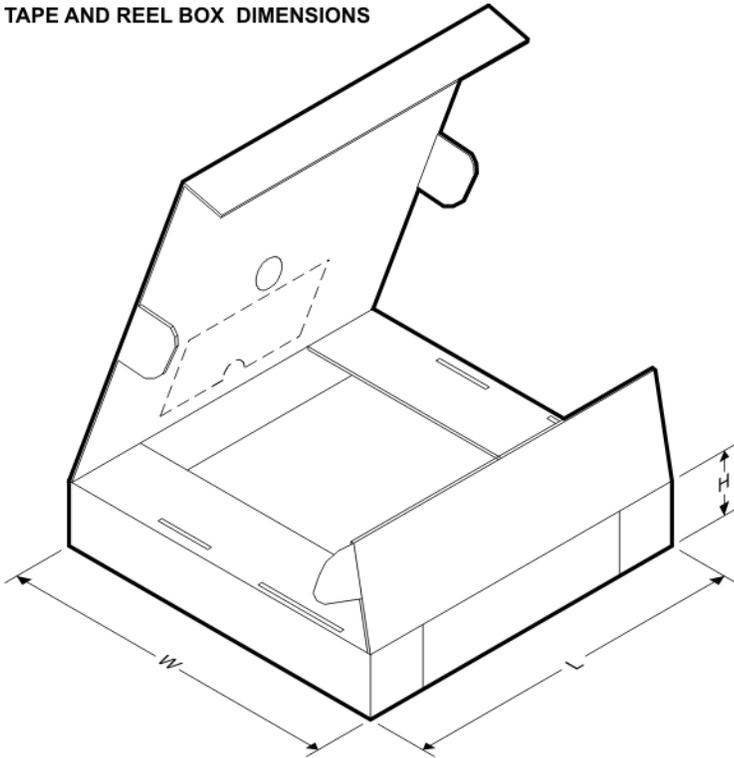
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO3080DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3082DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3086DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3088DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

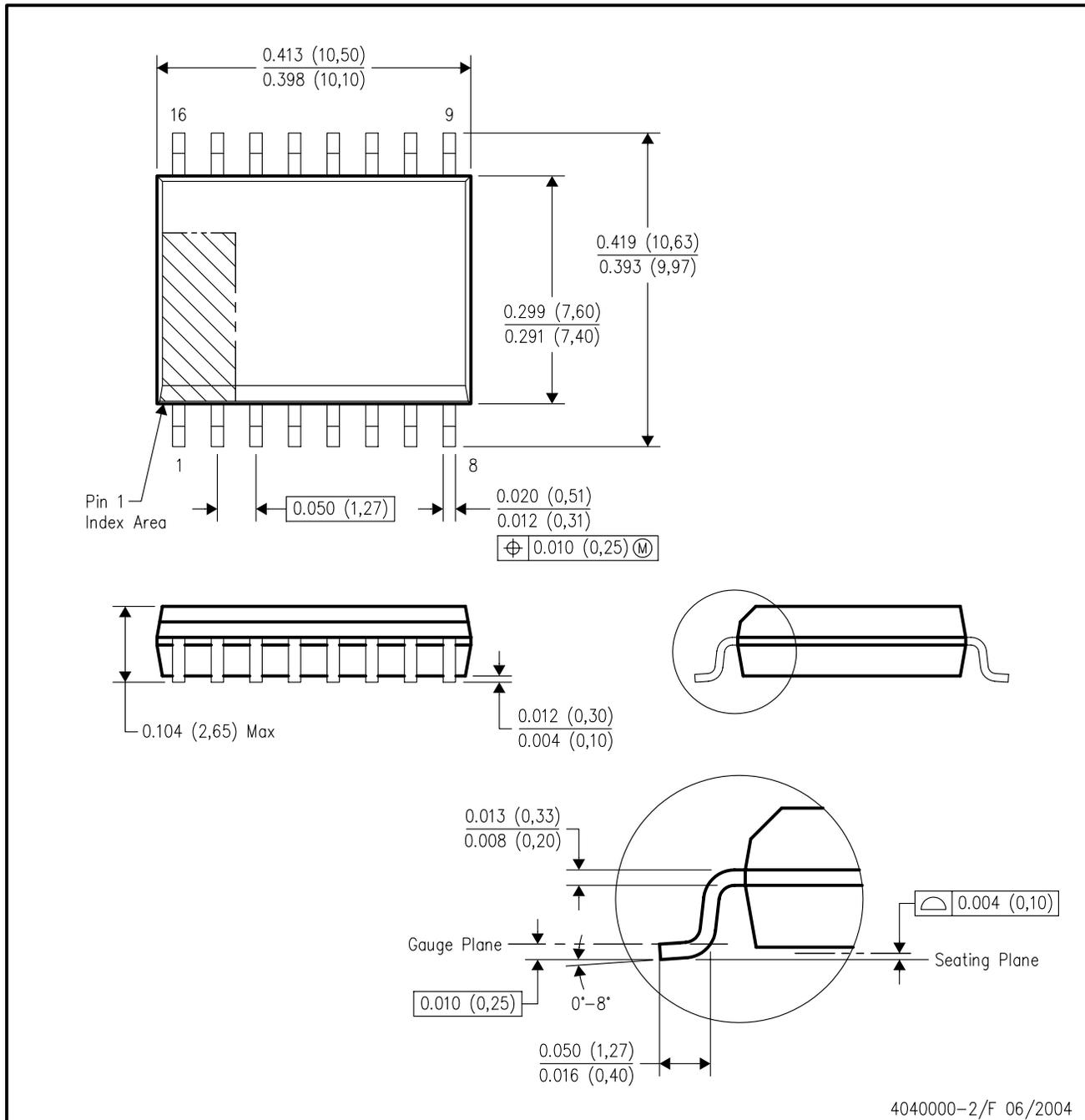


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO3080DWR	SOIC	DW	16	2000	358.0	335.0	35.0
ISO3082DWR	SOIC	DW	16	2000	358.0	335.0	35.0
ISO3086DWR	SOIC	DW	16	2000	358.0	335.0	35.0
ISO3088DWR	SOIC	DW	16	2000	358.0	335.0	35.0

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

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