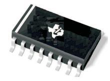


TRIPLE DIGITAL ISOLATORS

FEATURES

- **1, 25, and 150-Mbps Signaling Rate Options**
  - **Low Channel-to-Channel Output Skew; 1 ns max**
  - **Low Pulse-Width Distortion (PWD); 2 ns max**
  - **Low Jitter Content; 1 ns Typ at 150 Mbps**
- **Typical 25-Year Life at Rated Working Voltage (see application note SLLA197 and Figure 14)**
- **4000-V_{peak} Isolation, 560-V_{peak} Working Voltage**
- **UL 1577 Certified**
- **4 kV ESD Protection**
- **Operate With 3.3-V or 5-V Supplies**
- **High Electromagnetic Immunity (see application note SLLA181)**
- **–40°C to 125°C Operating Range**

APPLICATIONS

- **Industrial Fieldbus**
- **Computer Peripheral Interface**
- **Servo Control Interface**
- **Data Acquisition**

DESCRIPTION

The ISO7230 and ISO7231 are triple-channel digital isolators each with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

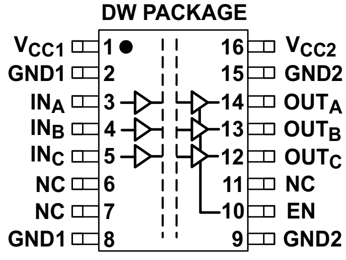
The ISO7230 triple-channel device has all three channels in the same direction while the ISO7231 has two channels in one direction and one channel in opposition. These devices have an active-high output enable that when driven to a low level, places the output in a high-impedance state and turns off internal bias circuitry to conserve power.

The ISO7230A, ISO7230C, ISO7231A, and ISO7231C have TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device, while the ISO7230M and ISO7231M have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter or the additional propagation delay.

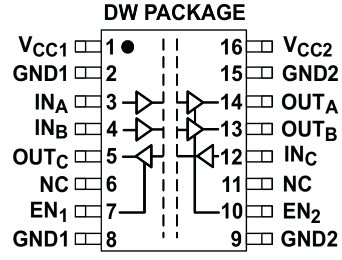
In each device a periodic update pulse is sent across the isolation barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS. These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

ISO7230
DW PACKAGE



ISO7231
DW PACKAGE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

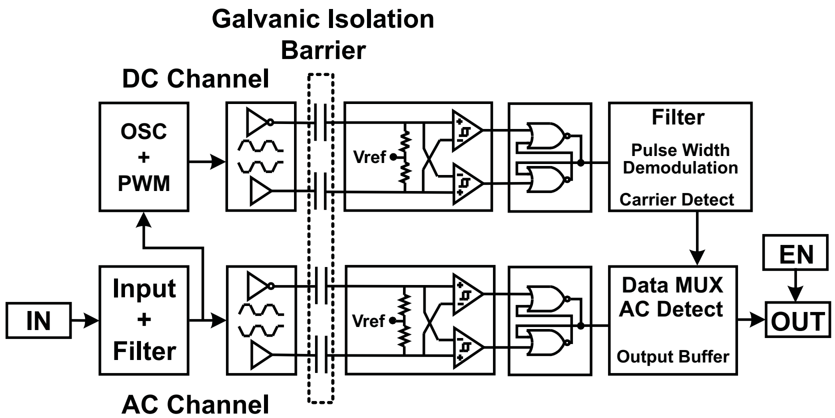


Table 1. Device Function Table ISO723x (1)

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER (1)
ISO7230ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	3/0	ISO7230A	ISO7230ADW (rail)
					ISO7230ADWR (reel)
ISO7230CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7230C	ISO7230CDW (rail)
					ISO7230CDWR (reel)
ISO7230MDW	150 Mbps	Vcc/2 (CMOS)		ISO7230M	ISO7230MDW (rail)
					ISO7230MDWR (reel)
ISO7231ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	2/1	ISO7231A	ISO7231ADW (rail)
					ISO7231ADWR (reel)
ISO7231CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7231C	ISO7231CDW (rail)
					ISO7231CDWR (reel)
ISO7231MDW	150 Mbps	Vcc/2 (CMOS)		ISO7231M	ISO7231MDW (rail)
					ISO7231MDWR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

					VALUE	UNIT
V_{CC}	Supply voltage[2], V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT, EN				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage, V_{CC1}, V_{CC2}		4.5		5.5	V
			3.15		3.6	
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		–4			mA
t_{ui}	Input pulse width	ISO723xA	1			µs
		ISO723xC	40			ns
		ISO723xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO723xA	0	1500[1]	1000	kbps
		ISO723xC	0	30[1]	25	Mbps
		ISO723xM	0	200[1]	150	
V_{IH}	High-level input voltage (IN)	ISO723xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 V_{CC}	
V_{IH}	High-level input voltage (IN) (EN on all devices)	ISO723xA, ISO723xC	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)		0		0.8	
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) Typical sigalling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA
	ISO7230A	1 Mbps			1	3	
	ISO7230C/M	25 Mbps			7	9.5	
	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
	ISO7231A	1 Mbps			6.5	11	
	ISO7231C/M	25 Mbps			11	17	
I_{CC2}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
	ISO7230A	1 Mbps			16	22	
	ISO7230C/M	25 Mbps			17	24	
	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
	ISO7231A	1 Mbps			13	20	
	ISO7231C/M	25 Mbps			17.5	27	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at VCC, Single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xA	See Figure 1	40		95	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xA	See Figure 1			10	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 1	18		42	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xC	See Figure 1			2.5	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM	See Figure 1	10		23	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xM	See Figure 1		1	2	ns
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xA/C			0	2	ns
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xM			0	1	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 2		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 2		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		12		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity inputon all channels, See Figure 5		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5-V, V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			1	3	mA
	ISO7230A	1 Mbps				1	3	
	ISO7230C/M	25 Mbps				7	9.5	
	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
	ISO7231A	1 Mbps				6.5	11	
	ISO7231C/M	25 Mbps				11	17	
I_{CC2}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			9	15	mA
	ISO7230A	1 Mbps				9.5	15	
	ISO7230C/M	25 Mbps				10	17	
	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	12	mA
	ISO7231A	1 Mbps				8	12	
	ISO7231C/M	25 Mbps				10.5	16	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at VCC, Single channel			0		μA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	ISO7230	V_{CC} – 0.4			V
				ISO7231 (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 μA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1				0.4	V
			I_{OL} = 20 μA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	μA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4		25	50		kV/μs

SWITCHING CHARACTERISTICS

V_{CC1} at 5-V, V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xA	See Figure 1	40		100	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xA	See Figure 1			11	ns
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xC	See Figure 1	20		50	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xC	See Figure 1			3	ns
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xM	See Figure 1	12		29	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xM	See Figure 1		1	2	ns
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xA/C			0	2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISSO723xM			0	1	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 2		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 2		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		18		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3-V, V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			0.5	1	mA
I_{CC1}	ISO7230A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			1	2	mA
I_{CC1}	ISO7230C/M	25 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			3	5	mA
I_{CC1}	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4.5	7	mA
I_{CC1}	ISO7231A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4.5	7	mA
I_{CC1}	ISO7231C/M	25 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
I_{CC2}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			15	22	mA
I_{CC2}	ISO7230A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			16	22	mA
I_{CC2}	ISO7230C/M	25 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			17	24	mA
I_{CC2}	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
I_{CC2}	ISO7231A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
I_{CC2}	ISO7231C/M	25 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			17.5	27	mA
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at VCC, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	ISO7230	V_{CC} – 0.4			V
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	ISO7231 (5-V side)	V_{CC} – 0.8			V
V_{OH}	High-level output voltage		I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1				0.4	V
V_{OL}	Low-level output voltage		I_{OL} = 20 µA, See Figure 1				0.1	V
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current		IN from 0 V to V_{CC}		–10			µA
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin(4E6\pi t)$			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3-V and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xA	See Figure 1	40		100	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} – t_{PLH} \rvert$					11	
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC		22		51	
PWD	Pulse-width distortion(1) $\lvert t_{PHL} – t_{PLH} \rvert$					3	
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM		12		30	
PWD	Pulse-width distortion(1) $\lvert t_{PHL} – t_{PLH} \rvert$				1	2	
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xA/C			0	2.5	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		12		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		0.5	1	mA
	ISO7230A	1 Mbps			1	2	
	ISO7230C/M	25 Mbps			3	5	
	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4.5	7	mA
	ISO7231A	1 Mbps			4.5	7	
	ISO7231C/M	25 Mbps			6.5	11	
I_{CC2}	ISO7230A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		9	15	mA
	ISO7230A	1 Mbps			9.5	15	
	ISO7230C/M	25 Mbps			10	17	
	ISO7231A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	12	mA
	ISO7231A	1 Mbps			8	12	
	ISO7231C/M	25 Mbps			10.5	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at V_{CC}, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/µs

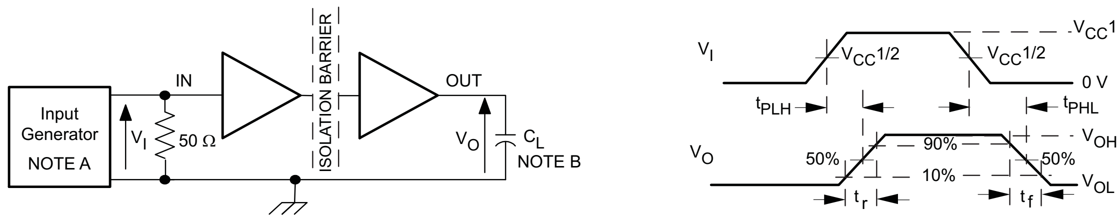
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xA	See Figure 1	45		110	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xA	See Figure 1			12	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 1	25		56	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO723xC	See Figure 1			4	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xM	See Figure 1	12		34	ns
PWD	Pulse-width distortion (1) $\|t_{PHL} – t_{PLH}\|$	ISO722xM	See Figure 1		1	2	ns
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xA/C			0	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xM			0	1	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 2		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 2		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		18		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 5		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

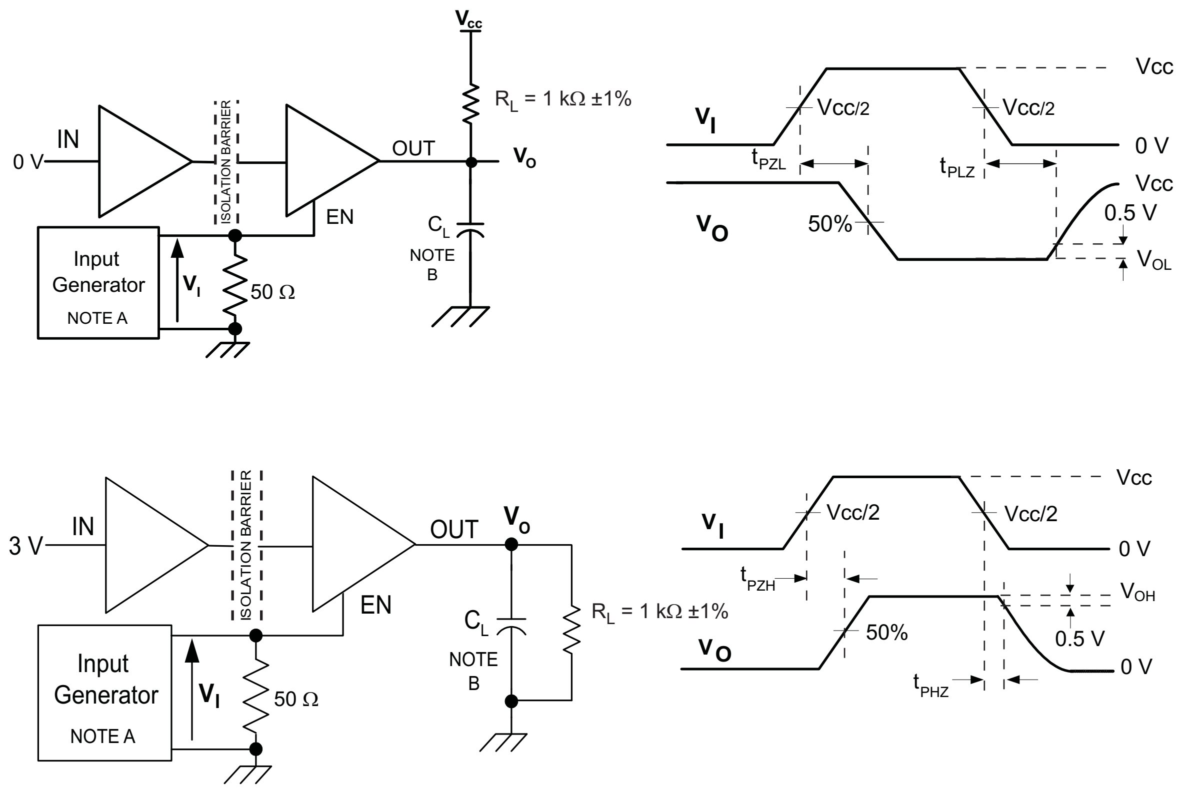
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

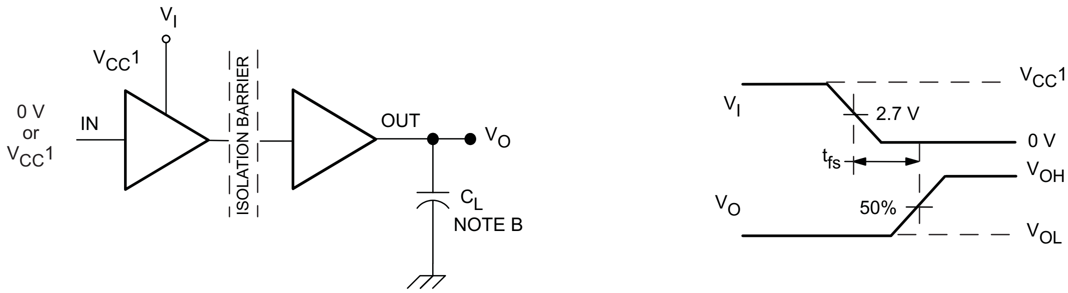


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

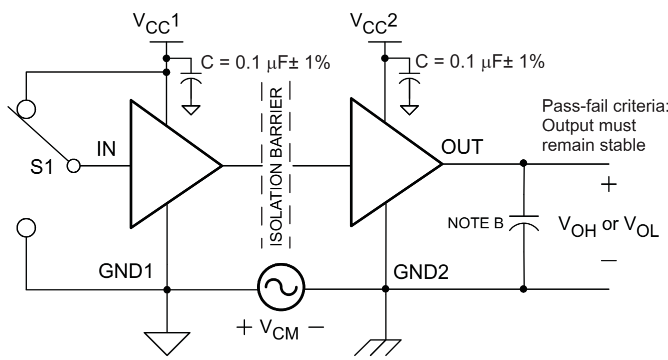
PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \le 3$ ns, $t_f \le 3$ ns, $Z_O = 50\Omega$.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

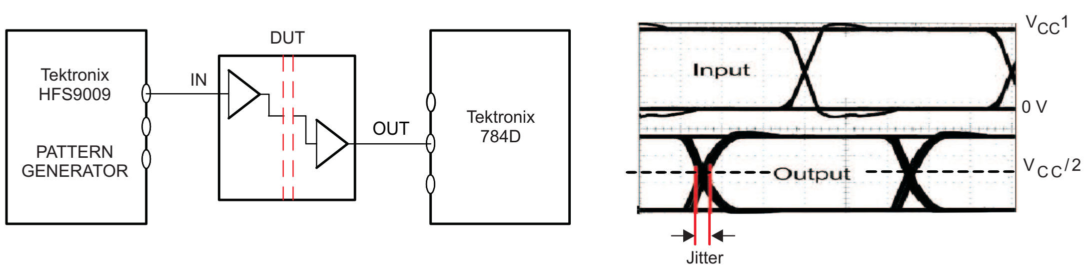
Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \le 3$ ns, $t_f \le 3$ ns, $Z_O = 50\Omega$.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 5. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

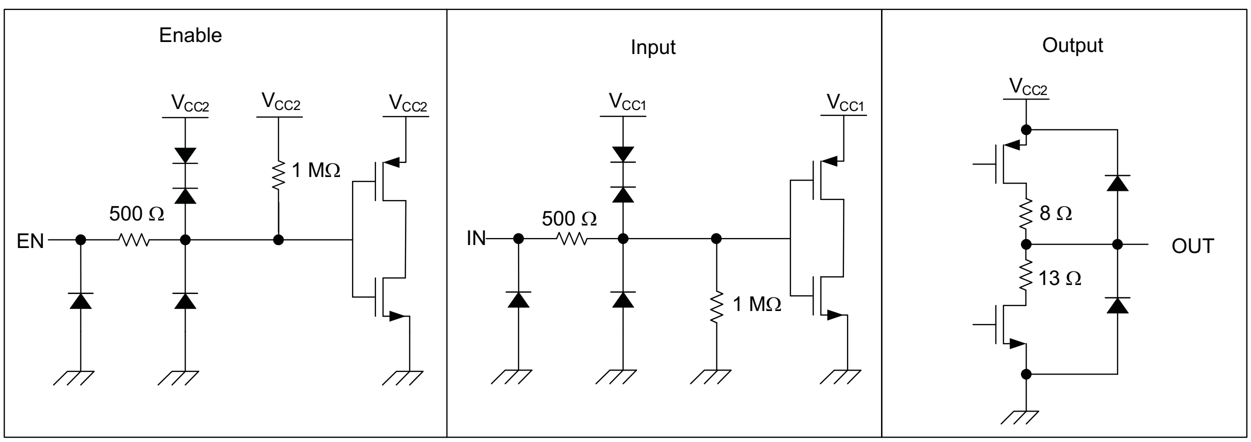
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	7.7			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program (1)
File Number: Pending	File Number: Pending	File Number: E181974

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance (1)		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	$V_{CC1} = V_{CC2}$ = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

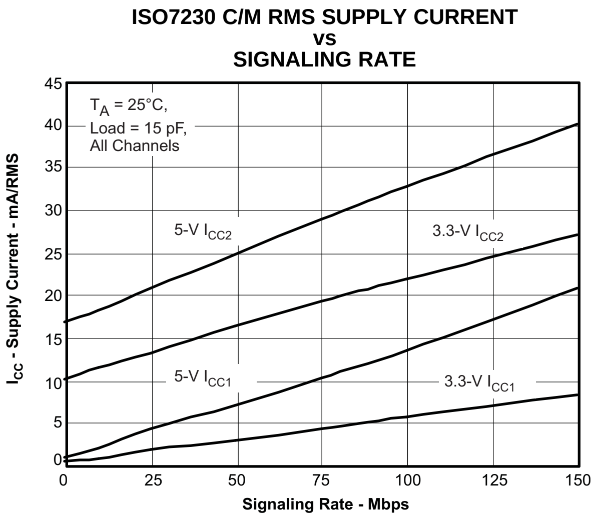


Figure 6.

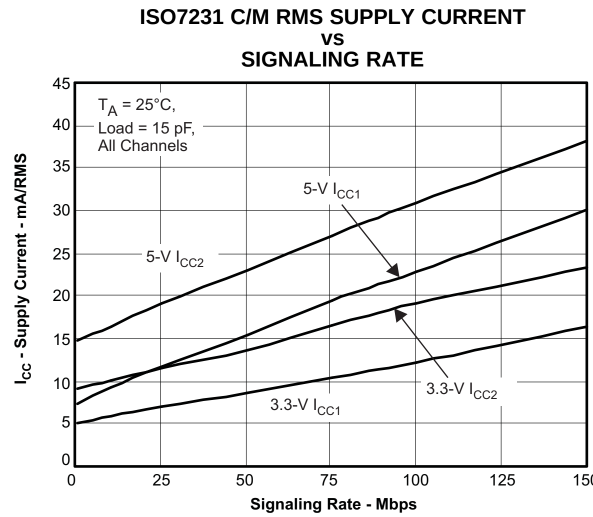


Figure 7.

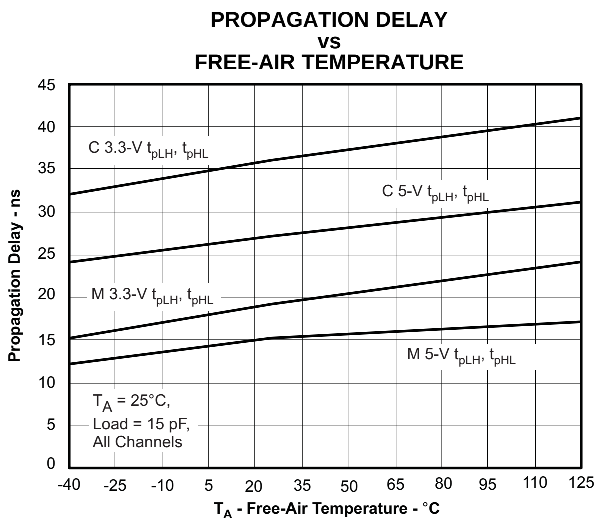


Figure 8.

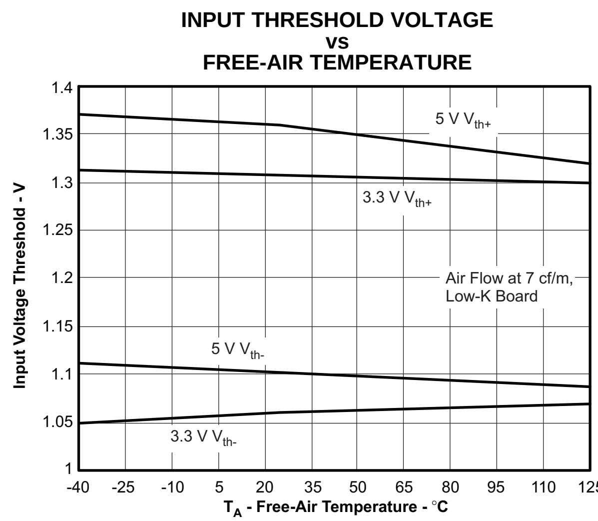


Figure 9.

TYPICAL CHARACTERISTIC CURVES (continued)

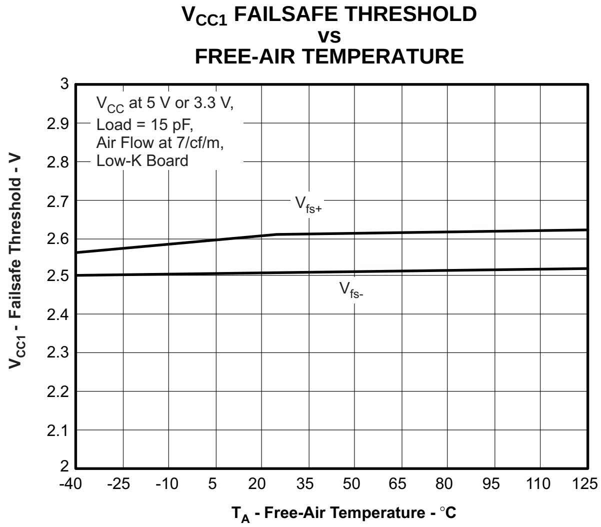


Figure 10.

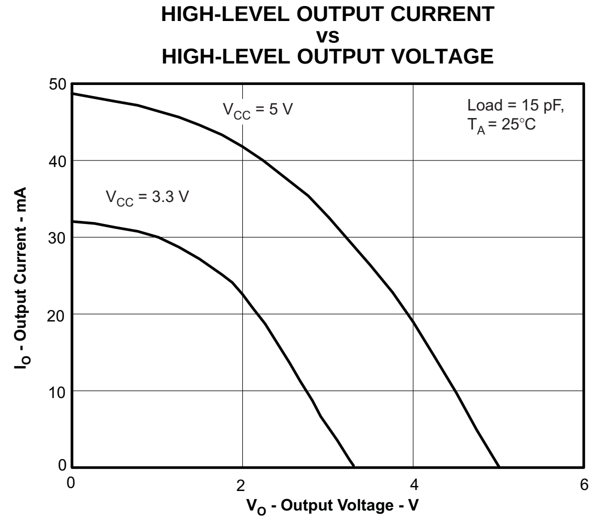


Figure 11.

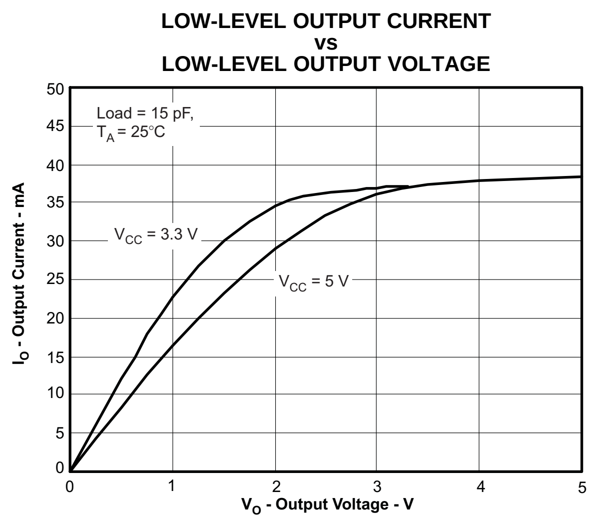


Figure 12.

APPLICATION INFORMATION

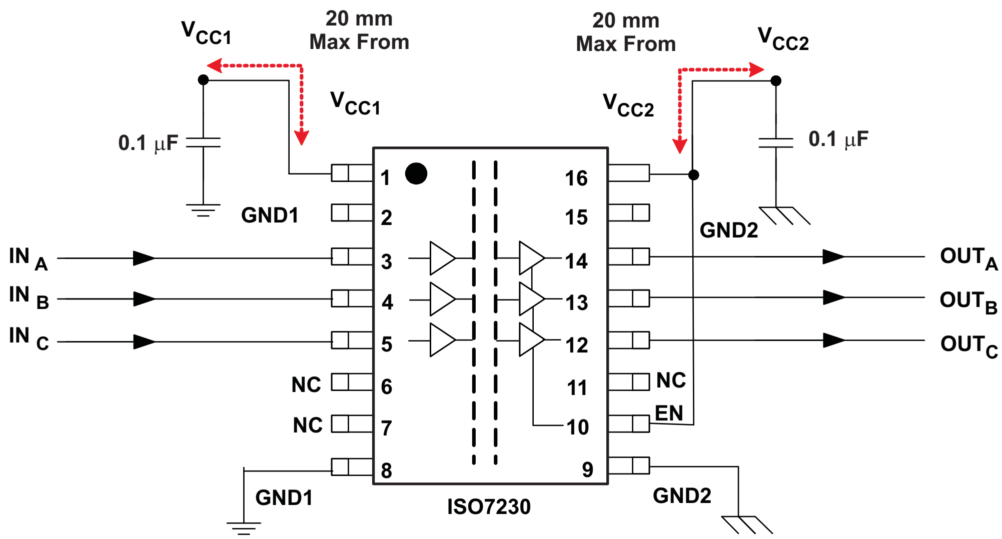


Figure 13. Typical ISO723x Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE

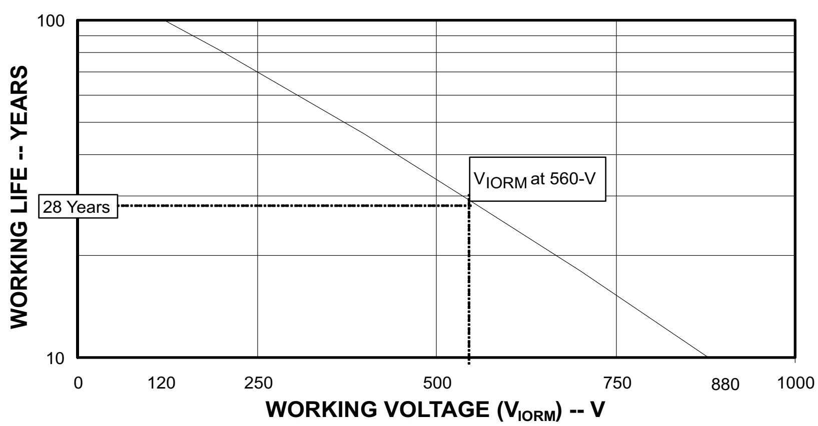


Figure 14. Time Dependant Dielectric Breakdown Testing Results

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
ISO7230ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230ADWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[(1)] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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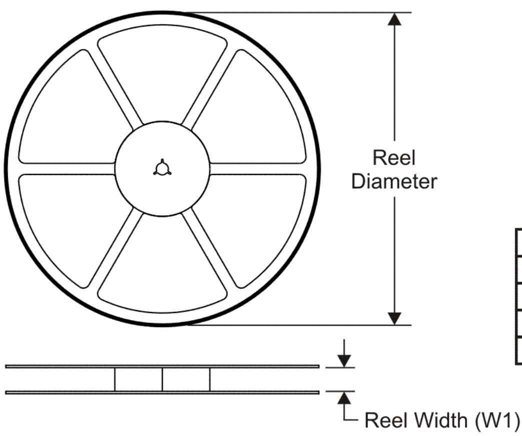
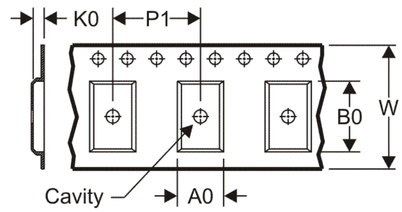
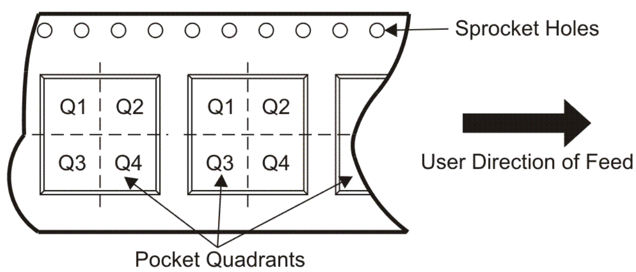
TAPE AND REEL INFORMATION





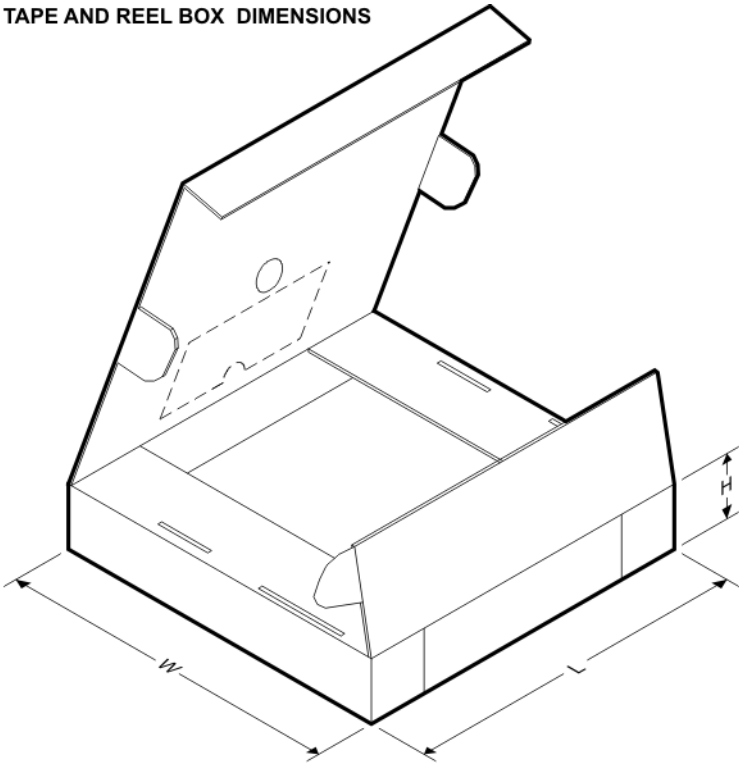
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230ADWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7230CDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7230MDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7231ADWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7231CDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7231MDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1

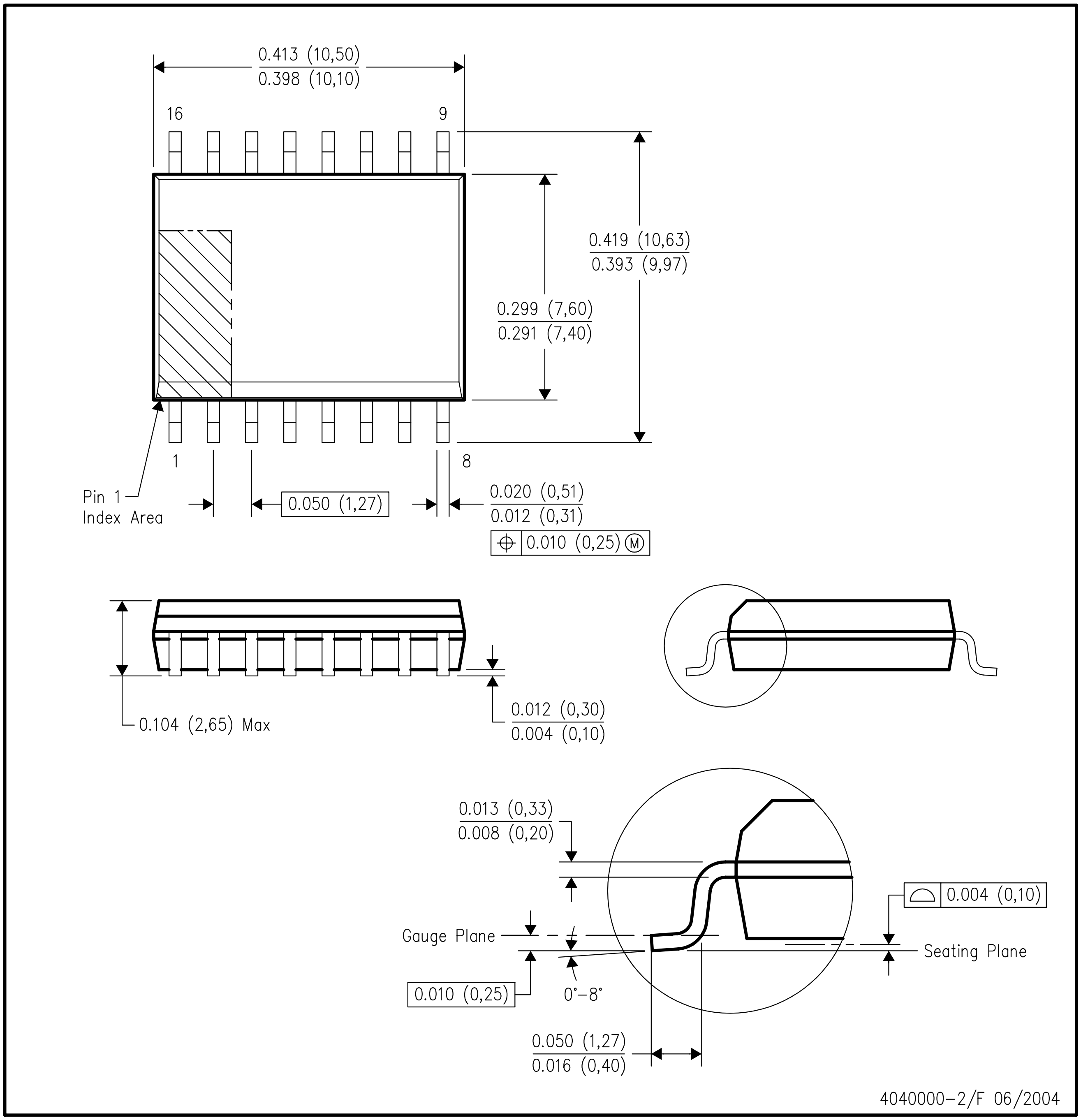
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7230ADWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7230CDWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7230MDWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7231ADWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7231CDWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7231MDWR	SOIC	DW	16	2000	406.0	348.0	63.0

DW (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.

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