



# ISP1301

Universal Serial Bus On-The-Go transceiver

Rev. 01 — 14 April 2004

Product data

## 1. General description

The ISP1301 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device that is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB Specification Rev. 1.0a*. The ISP1301 can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates.

It is ideal for use in portable electronics devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) and any system chip set (with the USB host or device function built-in but without the USB physical layer) to interface to the physical layer of the USB.

The ISP1301 can interface to devices with digital I/O voltages in the range of 1.65 V to 3.6 V.

The ISP1301 is available in HVQFN24 package.

## 2. Features

- Fully complies with:
  - ◆ *Universal Serial Bus Specification Rev. 2.0*
  - ◆ *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a*
  - ◆ *On-The-Go Transceiver Specification (CEA-2011) Rev. 1.0*
- Can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates
- Ideal for system ASICs or chip sets with built-in USB OTG dual-role core
- Supports mini USB analog car kit interface
- Supports various serial data interface protocols; transparent general-purpose buffer mode allows you to control the direction of data transfer
- Supports data line and  $V_{BUS}$  pulsing session request
- Contains Host Negotiation Protocol (HNP) command and status registers
- Supports serial I<sup>2</sup>C-bus™ interface for OTG status and command controls
- 2.7 V to 4.5 V power supply input range for the ISP1301
- Built-in charge pump regulator outputs 5 V at current greater than 8 mA
- Supports external charge pump
- Supports wide range interfacing I/O voltage ( $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ) for digital control logics



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- 8 kV built-in electrostatic discharge (ESD) protection on the DP, DM, V<sub>BUS</sub> and ID lines
- Full industrial grade operation from –40 °C to +85 °C
- Available in a small HVQFN24 (4 × 4 mm<sup>2</sup>) halogen-free and lead-free package.

### 3. Applications

- Mobile phone
- Digital camera
- Personal digital assistant
- Digital video recorder.

### 4. Abbreviations

**ASIC** — Application-Specific Integrated Circuit  
**ATX** — Analog USB transceiver  
**HNP** — Host Negotiation Protocol  
**ESD** — ElectroStatic Discharge  
**I<sup>2</sup>C-bus** — Inter IC-bus  
**IC** — Integrated Circuit  
**OTG** — On-The-Go  
**PDA** — Personal Digital Assistant  
**SE0** — Single-Ended zero  
**SOF** — Start-of-Frame  
**SRP** — Session Request Protocol  
**USB** — Universal Serial Bus  
**USB-IF** — USB Implementers Forum.

### 5. Ordering information

**Table 1: Ordering information**

Type number	Package		
	Name	Description	Version
ISP1301BS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

6. Block diagram

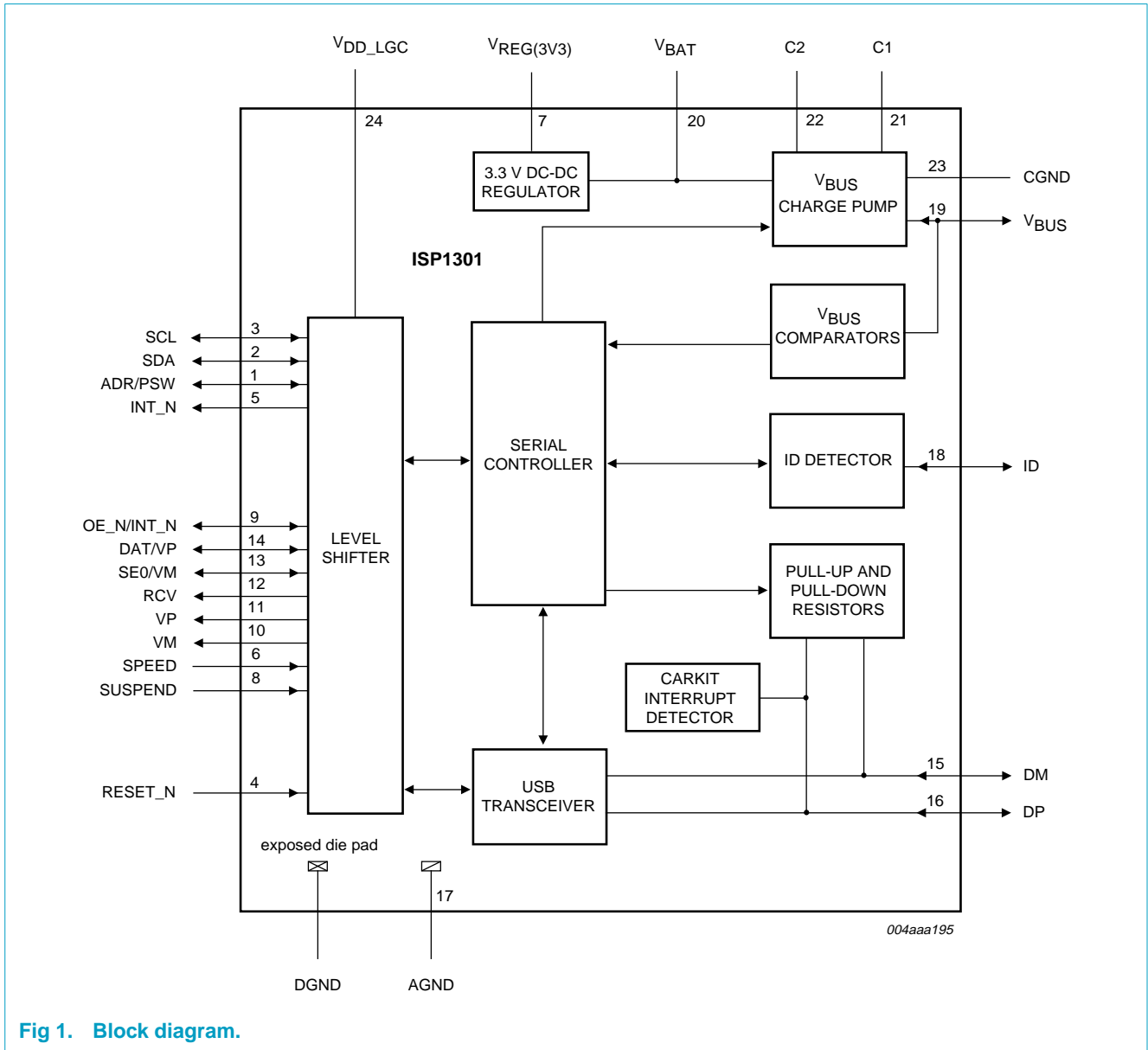
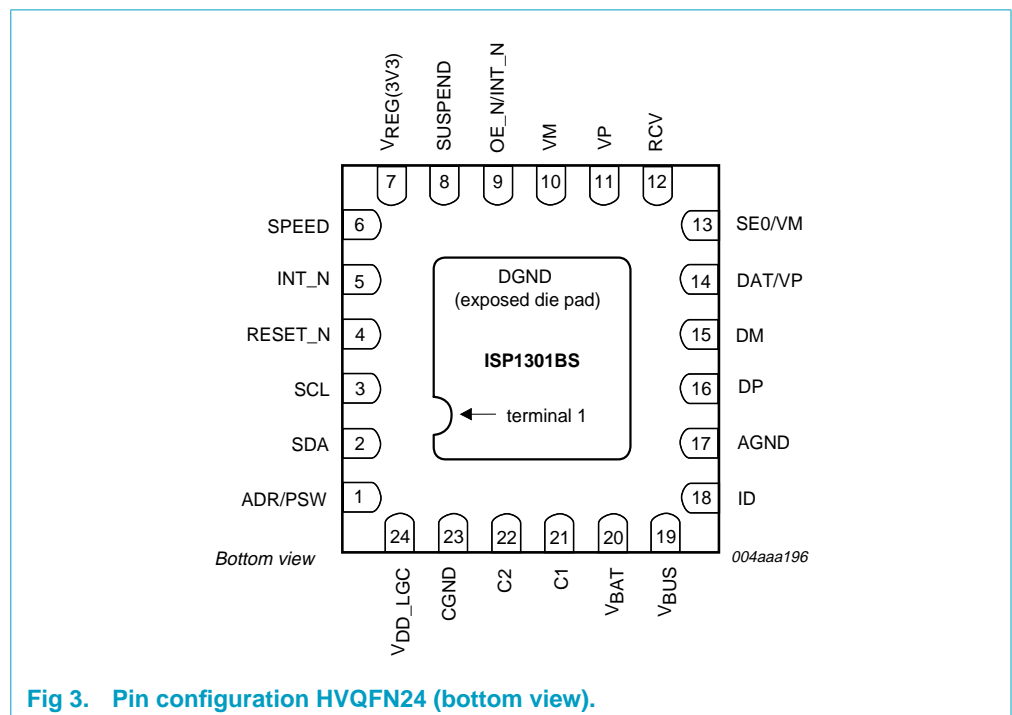
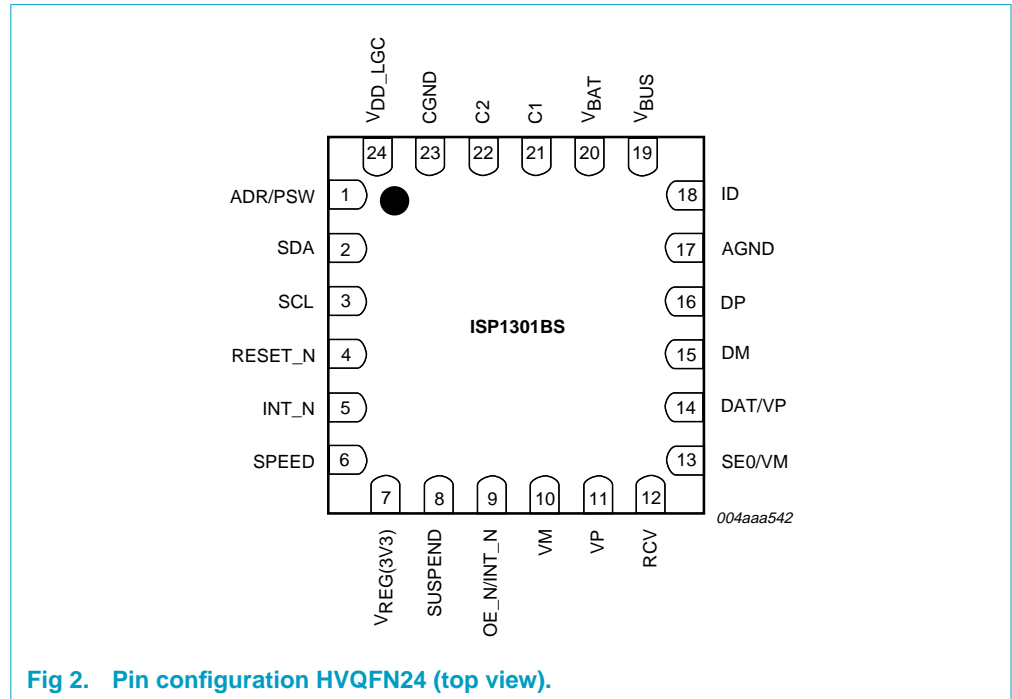


Fig 1. Block diagram.

## 7. Pinning information

### 7.1 Pinning



## 7.2 Pin description

Table 2: Pin description<sup>[1]</sup>

Symbol <sup>[2]</sup>	Pin	Type <sup>[3]</sup>	Reset value	Description
ADR/PSW	1	I/O	high-Z	<p><b>ADR input</b> — sets the least-significant I<sup>2</sup>C-bus address bit of the ISP1301; latched-on reset (including power-on reset)</p> <p><b>PSW output</b> — enables or disables the external charge pump after reset</p> <p>bidirectional; push-pull input; three-state output</p>
SDA	2	I/OD	high-Z	<p>serial I<sup>2</sup>C-bus data input and output</p> <p>bidirectional; push-pull input; open-drain output</p>
SCL	3	I/OD	high-Z	<p>serial I<sup>2</sup>C-bus clock input and output</p> <p>bidirectional; push-pull input; open-drain output</p>
RESET_N	4	I	-	<p>asynchronous reset; active LOW</p> <p>push-pull input</p>
INT_N	5	OD	high-Z	<p>interrupt output; active LOW</p> <p>open-drain output</p>
SPEED	6	I	-	<p>speed selection input for the ATX; effective when bit SPD_SUSP_CTRL = 0:</p> <ul style="list-style-type: none"> <li>• LOW: low-speed</li> <li>• HIGH: full-speed.</li> </ul> <p>push-pull input</p>
V <sub>REG(3V3)</sub>	7	P	-	<p>output of the internal voltage regulator; an external decoupling capacitor of 0.1 μF is required</p>
SUSPEND	8	I	-	<p>suspend selection input for ATX; effective when bit SPD_SUSP_CTRL = 0:</p> <ul style="list-style-type: none"> <li>• LOW: normal operating</li> <li>• HIGH: suspend.</li> </ul> <p>push-pull input</p>
OE_N/ INT_N	9	I/O	high-Z	<p><b>OE_N input</b> — enable driving DP and DM when in the USB mode</p> <p><b>INT_N output</b> — interrupt (push pull) when suspended and bit OE_INT_EN = 1</p> <p>bidirectional; push-pull input; three-state output</p>
VM	10	O	-	<p>single-ended DM receiver output</p> <p>push-pull output</p>
VP	11	O	-	<p>single-ended DP receiver output</p> <p>push-pull output</p>
RCV	12	O	0	<p>differential receiver output; reflects the differential value of DP and DM</p> <p>push-pull output</p>

Table 2: Pin description<sup>[1]</sup>...continued

Symbol <sup>[2]</sup>	Pin	Type <sup>[3]</sup>	Reset value	Description
SE0/VM	13	I/O	- <sup>[4]</sup>	<b>SE0 (input and output)</b> — SE0 function in DAT_SE0 USB mode <b>VM (input and output)</b> — VM function in VP_VM USB mode bidirectional; push-pull input; three-state output
DAT/VP	14	I/O	- <sup>[4]</sup>	<b>DAT (input and output)</b> — DAT function in DAT_SE0 USB mode <b>VP (input and output)</b> — VP function in VP_VM USB mode bidirectional; push-pull input; three-state output
DM	15	A/O	-	USB data minus pin (D-)
DP	16	A/O	-	USB data plus pin (D+)
AGND	17	P	-	analog ground
ID	18	A/O	-	identification detector input and output; connected to the ID pin of the USB mini receptacle
V <sub>BUS</sub>	19	A/O	-	V <sub>BUS</sub> line input and output of the USB interface; place an external decoupling capacitor of 0.1 μF close to this pin
V <sub>BAT</sub>	20	P	-	supply voltage (2.7 V to 4.5 V)
C1	21	A/O	-	charge pump capacitor pin 1; typically use a 100 nF capacitor between pins C1 and C2
C2	22	A/O	-	charge pump capacitor pin 2; typically use a 100 nF capacitor between pins C1 and C2
CGND	23	P	-	ground for the charge pump
V <sub>DD_LGC</sub>	24	P	-	supply voltage for the interface logic signals (1.65 V to 3.6 V)
DGND	exposed die pad	P	-	digital ground

- [1] A detailed description of these pins can be found in [Section 8.9](#).
- [2] Symbol names ending with underscore N (for example, NAME\_N) indicate active LOW signals.
- [3] I = input; O = output; I/O = digital input/output; OD = open-drain output; A/O = analog input/output; P = power or ground pin.
- [4] High-Z when pin OE\_N/INT\_N is LOW. Driven LOW when pin OE\_N/INT\_N is HIGH.

## 8. Functional description

### 8.1 Serial controller

The serial controller includes the following functions:

- I<sup>2</sup>C-bus slave interface
- Interrupt generator
- Mode Control registers
- OTG registers
- Interrupt related registers
- Device identification registers.

The serial controller acts as an I<sup>2</sup>C-bus slave, and uses the SCL and SDA pins to communicate with the OTG controller.

For more details on serial controller, see [Section 11](#).

### 8.2 V<sub>BUS</sub> charge pump

The charge pump supplies current to the V<sub>BUS</sub> line. It can operate in any of the following modes:

- Output 5 V at current greater than 8 mA
- Pull-up V<sub>BUS</sub> to 3.3 V through a resistor (R<sub>VBUS(PU)</sub>) for initiating V<sub>BUS</sub> pulsing SRP
- Pull-down V<sub>BUS</sub> to ground through a resistor (R<sub>VBUS(PD)</sub>) for discharging V<sub>BUS</sub> before initiating SRP.

### 8.3 V<sub>BUS</sub> comparators

V<sub>BUS</sub> comparators provide indications regarding the voltage level on V<sub>BUS</sub>.

#### 8.3.1 V<sub>BUS</sub> valid comparator

This comparator is used by an A-device to determine whether or not the voltage on V<sub>BUS</sub> is at a valid level for operation. The minimum threshold for the V<sub>BUS</sub> valid comparator is 4.4 V. Any voltage on V<sub>BUS</sub> below this threshold is considered to be a fault. During power up, it is expected that the comparator output will be ignored.

#### 8.3.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V<sub>BUS</sub> is high enough for a session to start. Both the A-device and the B-device use this comparator to detect when a session is being started. The A-device also uses this comparator to indicate when a session is completed. The session valid threshold of the ISP1301 is between 0.8 V and 2.0 V.

#### 8.3.3 Session end comparator

The session end comparator determines when V<sub>BUS</sub> is below the B-device session end threshold of 0.2 V to 0.8 V.

## 8.4 ID detector

In either the active or suspended power mode, the ID detector senses the condition of the ID line and differentiates between the following three conditions:

- Pin ID is floating; bit ID\_FLOAT = 1
- Pin ID is shorted to ground; bit ID\_GND = 1
- Pin ID is connected to ground through resistor R<sub>ACC\_ID</sub>; bit ID\_FLOAT = 0 and bit ID\_GND = 0.

The ID detector also has a switch that can be used to ground pin ID. This switch is controlled by bit ID\_PULLDOWN in the serial controller.

## 8.5 Pull-up and pull-down resistors

The pull-up and pull-down resistors include the following switchable resistors:

- Pin DP pull-up
- Pin DP pull-down
- Pin DM pull-up
- Pin DM pull-down.

The pull-up resistor is a context variable as described in the *ECN\_27%\_Resistor* document. The variable pull-up resistor hardware is implemented to meet the USB ECN\_27% specification.

## 8.6 USB transceiver (ATX)

The behavior of the USB transceiver depends on the operation mode of the ISP1301:

- In the USB mode, the USB transceiver block performs USB full-speed or low-speed transceiver functions. This includes differential driver, differential receiver and single-ended receivers.
- In the transparent general purpose buffer mode or the UART mode, the USB transceiver block functions as a level shifter between the pins DAT/VP and SE0/VM and the pins DP and DM.

## 8.7 3.3 V DC-DC regulator

The built-in 3.3 V DC-DC regulator conditions the supply voltage ( $V_{BAT}$ ) for use in the ISP1301:

- $V_{BAT} = 3.6 \text{ V to } 4.5 \text{ V}$ : the regulator will output  $3.3 \text{ V} \pm 10 \%$
- $V_{BAT} < 3.6 \text{ V}$ : the regulator will be bypassed.

The output of the regulator can be monitored on the  $V_{REG(3V3)}$  pin.

## 8.8 Car kit interrupt detector

The car kit interrupt detector is a comparator that detects when the DP line is below the car kit interrupt threshold  $V_{PH\_CR\_INT}$  (0.4 V to 0.6 V). The car kit interrupt detector is enabled in the audio mode only (bit AUDIO\_EN = 1).



## 8.9 Detailed description of pins

### 8.9.1 ADR/PSW

The ADR/PSW pin has two functions. On reset (including power-on reset), the level on this pin is latched as ADR\_REG, which represents the least significant bit (LSB) of the I<sup>2</sup>C address of the ISP1301. If bit ADR\_REG = 0, the I<sup>2</sup>C-bus address for the ISP1301 is 0101100 (0x2C); if bit ADR\_REG = 1, the I<sup>2</sup>C-bus address for the ISP1301 is 0101101 (0x2D).

After reset, the ADR/PSW pin can be programmed as an output. If in the Mode Control 2 register bit PSW\_OE = 1, then the ADR/PSW output will be enabled. The logic level will be determined by bit ADR\_REG. If bit ADR\_REG = 0, then the ADR/PSW pin will drive HIGH. If bit ADR\_REG = 1, then the ADR/PSW pin will drive LOW.

The ADR/PSW pin can be used to turn on or off the external charge pump. The ISP1301 built-in charge pump supports  $V_{BUS}$  current at 8 mA. If the application needs more current support (for example, 50 mA), an external charge pump may be needed. In this case, the ADR/PSW pin can act as a power switch for the external charge pump. Figure 4 shows an example of using external charge pump.

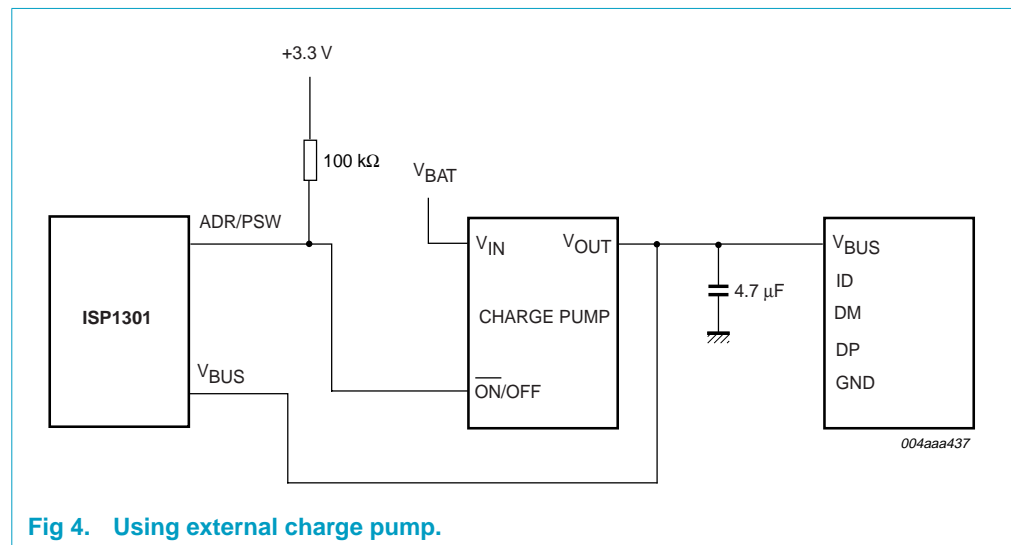


Fig 4. Using external charge pump.

### 8.9.2 SCL and SDA

The SCL (serial clock) and SDA (serial data) signals implement a two-wire serial I<sup>2</sup>C-bus.

### 8.9.3 RESET\_N

Active LOW asynchronous reset for all digital logic. Either connect this pin to  $V_{DD\_LGC}$  for power-on reset or apply a minimum of 10  $\mu$ s LOW pulse for hardware reset.

### 8.9.4 INT\_N

The INT\_N (interrupt) pin is asserted while an interrupt condition exists. It is deasserted when the Interrupt Latch register is cleared. The INT\_N pin is open-drain, and, therefore, can be connected using a wired-AND with other interrupt signals.

### 8.9.5 OE\_N/INT\_N

Pin OE\_N/INT\_N is normally an input to the ISP1301.

When bit TRANSP\_EN = 0 and bit UART\_EN = 0, the OE\_N/INT\_N pin controls the direction of DAT/VP, SE0/VM, DP and DM as indicated in [Table 4](#).

When suspended (either pin SUSPEND = HIGH or bit SUSPEND\_REG = 1) and bit OE\_INT\_EN = 1, pin OE\_N/INT\_N becomes a push-pull output (active LOW) to indicate the interrupt condition.

### 8.9.6 SE0/VM, DAT/VP, RCV, VM and VP

The ISP1301 transmits USB data on the USB line under the following conditions:

- Bit TRANSP\_EN = 0
- Bit UART\_EN = 0
- Pin OE\_N/INT\_N = LOW.

[Table 10](#) shows the operation of the SE0/VM and DAT/VP pins during the transmit operation. The RCV pin is not used during transmit.

The ISP1301 receives USB data from the USB line under the following conditions:

- Bit TRANSP\_EN = 0
- Bit UART\_EN = 0
- Pin OE\_N/INT\_N = HIGH.

[Table 12](#) shows the operation of the SE0/VM, DAT/VP and RCV pins during the receive operation.

The VP and VM pins are single-ended receiver outputs of the DP and DM pins, respectively.

### 8.9.7 DP and DM

The DP (data plus) and DM (data minus) pins implement the USB data signals. When in the transparent general-purpose buffer mode, the ISP1301 operates as a level shifter between the (DAT/VP, SE0/VM) and (DP, DM) pins.

### 8.9.8 ID

The ID (identification) pin is connected to the ID pin on the USB mini receptacle. An internal pull-up resistor (to  $V_{REG(3V3)}$ ) is connected to this pin. When bit ID\_PULLDOWN is set, the ID pin will be shorted to ground.

### 8.9.9 V<sub>BUS</sub>

This pin acts as an input to the V<sub>BUS</sub> comparator or an output from the charge pump.

When the VBUS\_DRV bit of the OTG Control register is asserted, the ISP1301 tries to drive V<sub>BUS</sub> to a voltage of 4.4 V to 5.25 V with an output current capability of at least 8 mA.

**8.9.10 V<sub>BAT</sub>**

This pin is an input and supplies power to the ISP1301. The ISP1301 operates when V<sub>BAT</sub> is between 2.7 V and 4.5 V.

**8.9.11 C1 and C2**

The C1 and C2 pins are for connecting the flying capacitor of the charge pump. The output current capacity of the charge pump depends on the value of the capacitor. For maximum efficiency, place capacitors as close as possible to the pins.

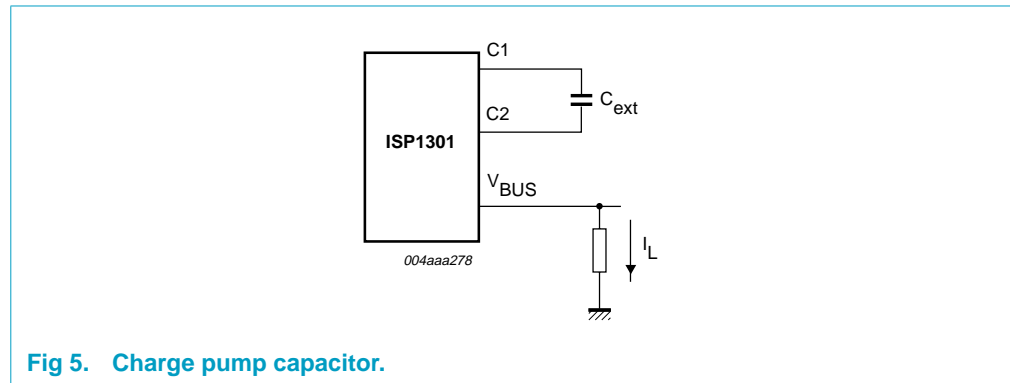


Fig 5. Charge pump capacitor.

Table 3: Recommended charge pump capacitor value

C <sub>ext</sub>	I <sub>L</sub> (max) <sup>[1]</sup>
47 nF	8 mA
100 nF	18 mA <sup>[2]</sup>

[1] For output voltage V<sub>BUS</sub> > 4.7 V (bit VBUS\_VLD = 1).

[2] For V<sub>BAT</sub> = 3.0 V to 4.5 V.

**8.9.12 V<sub>DD\_LGC</sub>**

This pin is an input and sets logic thresholds. It also powers the pads of the following logic pins:

- ADR/PSW
- DAT/VP, SE0/VM and RCV
- VM and VP
- INT\_N
- OE\_N/INT\_N
- RESET\_N
- SPEED
- SUSPEND
- SCL and SDA.

**8.9.13 AGND, CGND and DGND**

AGND, CGND and DGND are ground pins for analog, charge pump and digital circuits, respectively. These pins can be connected separately or together depending on the system performance requirements.

## 9. Modes of operation

There are four types of modes in the ISP1301:

- Power modes
- Direct I<sup>2</sup>C-bus mode
- USB modes
- Transparent modes.

### 9.1 Power modes

The power modes of the ISP1301 are as follows:

- Active power mode: power is on.
- USB suspend mode: to reduce power consumption, the USB differential receiver is powered down.
- Global power-down mode: set bit GLOBAL\_PWR\_DN = 1 of the Mode Control 2 register; the differential transmitter and receiver, clock generator, charge pump, and all biasing circuits are turned off to reduce power consumption to the minimum possible; for details on waking up the clock, see [Section 12](#).

### 9.2 Direct I<sup>2</sup>C-bus mode

In the direct I<sup>2</sup>C-bus mode, an external I<sup>2</sup>C-bus master (OTG controller) directly communicates with the serial controller through the SCL and SDA lines. The serial controller has a built-in I<sup>2</sup>C-bus slave function.

In this mode, an external I<sup>2</sup>C-bus master can access the internal registers of the device (Status, Control, Interrupt, and so on) through the I<sup>2</sup>C-bus interface.

The supported I<sup>2</sup>C-bus bit rate is 100 kbit/s (maximum).

The ISP1301 is in the direct I<sup>2</sup>C-bus mode when either bit TRANSP\_EN bit = 0 or pin OE\_N/INT\_N is deasserted.

### 9.3 USB modes

The four USB modes of the ISP1301 are:

- VP\_VM unidirectional mode
- VP\_VM bidirectional mode
- DAT\_SE0 unidirectional mode
- DAT\_SE0 bidirectional mode.

In the VP\_VM USB mode, the DAT/VP pin is used for the VP function, the SE0/VM pin is used for the VM function, and the RCV pin is used for the RCV function.

In the DAT\_SE0 USB mode, the DAT/VP pin is used for the DAT function, the SE0/VM pin is used for the SE0 function, and the RCV pin is not used.

In the unidirectional mode, the DAT/VP and SE0/VM pins are always inputs. In the bidirectional mode, the direction of these signals depends on the OE\_N/INT\_N input.

Table 6 specifies the functionality of the device during the four USB modes.

The ISP1301 is in the USB mode when both the TRANSP\_EN and UART\_EN bits are cleared.

## 9.4 Transparent modes

### 9.4.1 Transparent general-purpose buffer mode

In the transparent general-purpose buffer mode, the DAT/VP and SE0/VM pins are connected to the DP and DM pins, respectively. Using bits TRANSP\_BDIR1 and TRANSP\_BDIR0 of the Mode Control 2 register as specified in Table 8, you can control the direction of data transfer. The ISP1301 is in the transparent general-purpose buffer mode if bit TRANSP\_EN = 1 and bit DAT\_SE0 = 1.

### 9.4.2 Transparent UART mode

When in the transparent UART mode, the ATX behaves as two logic level translator between the following pins:

- For TxD signal: from SE0/VM ( $V_{DD\_LGC}$  level) to DM (+3.3 V level)
- For RxD signal: from DP (+3.3 V level) to DAT/VP ( $V_{DD\_LGC}$  level).

In the UART mode, the OTG controller is allowed to connect a UART to the DAT/VP and SE0/VM pins of the ISP1301.

The UART mode is entered by setting the UART\_EN bit in the Mode Control 1 register. The UART mode is equivalent to one of the transparent general purpose buffer mode (bit TRANSP\_BDIR1 = 1, bit TRANSP\_BDIR0 = 0).

### 9.4.3 Summary tables

Table 4: Device operating modes

Mode	USB suspend condition <sup>[1]</sup>	Bit DAT_SE0	Pin OE_N/INT_N	Bit TRANSP_EN	Bit UART_EN	Description
<b>Direct I<sup>2</sup>C-bus mode</b>						
Direct I <sup>2</sup> C-bus mode	X	X	X	0	X	
	X	X	HIGH	1	X	
	X	1	X	1	X	
<b>USB modes</b>						
USB suspend mode	1	X	X	0	0	see Table 5 and Table 7
USB functional mode	0	X	X	0	0	ATX is fully functional; see Table 6
<b>Transparent modes</b>						
Transparent general-purpose buffer mode	X	1	X	1	0	ATX is not functional; see Table 8
Transparent UART mode	X	X	X	X	1	DAT/VP <= DP (RxD signal of UART) SE0/VM => DM (TxD signal of UART); ATX is not functional

[1] Conditions:

- bit SPD\_SUSP\_CTRL = 0 and pin SUSPEND = HIGH, or
- bit SPD\_SUSP\_CTRL = 1 and bit SUSPEND\_REG = 0.

**Table 5: USB suspend mode: I/O**

Pin	Function
DP as output	can be driven if pin OE_N/INT_N is active LOW, otherwise high-Z <sup>[1]</sup>
DM as output	can be driven if pin OE_N/INT_N is active LOW, otherwise high-Z <sup>[1]</sup>
V <sub>BUS</sub>	can be driven depending on bit VBUS_DRV
SCL	connected to SCL I/O of the I <sup>2</sup> C-bus slave
SDA	connected to SDA I/O of the I <sup>2</sup> C-bus slave

[1] In the USB suspend mode, the ISP1301 can drive the DP and DM lines, if the OE\_N/INT\_N input (when the OE\_INT\_EN bit is not set) is LOW. In such a case, these outputs are driven as in the USB functional modes, but with the full-speed characteristics, irrespective of the value of the SPEED input pin or the SPEED\_REG bit.

**Table 6: USB functional modes: I/O values<sup>[1]</sup>**

USB mode		Bit		Pin					
		DAT_SE0	BI_DI	OE_N/INT_N	DAT/VP	SE0/VM	VP	VM	RCV
VP_VM	unidirectional	0	0	X	TxD <sup>[2]</sup>	TxD <sup>−[2]</sup>	RxD <sup>+[3]</sup>	RxD <sup>−[3]</sup>	RxD <sup>[3]</sup>
	bidirectional	0	1	LOW	TxD <sup>[2]</sup>	TxD <sup>−[2]</sup>			
		0	1	HIGH	RxD <sup>+[3]</sup>	RxD <sup>−[3]</sup>			
DAT_SE0	unidirectional	1	0	X	TxD <sup>[4]</sup>	FSE0 <sup>[5]</sup>			
	bidirectional	1	1	LOW	TxD <sup>[4]</sup>	FSE0 <sup>[5]</sup>			
		1	1	HIGH	RxD <sup>[6]</sup>	RSE0 <sup>[7]</sup>			

[1] Some of the modes and signals are provided to achieve backward compatibility with IP cores.

[2] TxD+ and TxD− are single-ended inputs for driving the DP and DM outputs, respectively, in the single-ended mode.

[3] RxD+ and RxD− are the outputs of the single-ended receivers connected to DP and DM, respectively.

[4] TxD is the input for driving DP and DM in the DAT\_SE0 mode.

[5] FSE0 is for forcing an SE0 on the DP and DM lines in the DAT\_SE0 mode.

[6] RxD is the output of the differential receiver.

[7] RSE0 is an output indicating that an SE0 has been received on the DP and DM lines.

**Table 7: USB suspend mode: I/O values**

USB suspend mode	Input pin		Output pin				
	DP	DM	DAT/VP	SE0/VM	VP	VM	RCV
DAT_SE0 (bit DAT_SE0 = 1)	LOW	LOW	LOW	HIGH	LOW	LOW	LOW
	HIGH	LOW	HIGH	LOW	HIGH	LOW	LOW
	LOW	HIGH	LOW	LOW	LOW	HIGH	LOW
	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LOW
VP_VM (bit DAT_SE0 = 0)	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	HIGH	LOW	HIGH	LOW	HIGH	LOW	LOW
	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW
	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW

**Table 8: Transparent general-purpose buffer mode**

Bit TRANSP_BDIR[1:0]	Direction of the data flow	
00	DAT/VP => DP	SE0/VM => DM
01	DAT/VP => DP	SE0/VM <= DM
10	DAT/VP <= DP	SE0/VM => DM
11	DAT/VP <= DP	SE0/VM <= DM

## 10. USB transceiver

### 10.1 Differential driver

The operation of the driver is described in [Table 9](#). The register bits and the pins used in the column heading are described in [Section 11.1](#) and [Section 8.9](#), respectively.

**Table 9: Transceiver driver operation setting**

Suspend <sup>[1]</sup>	Bit TRANSP_EN	Pin OE_N/ INT_N	Bit DAT_SE0	Differential driver
0	0	LOW	0	output value from DAT/VP to DP and SE0/VM to DM
0	0	LOW	1	output value from DAT/VP to DP and DM if SE0/VM is 0; otherwise, drive both DP and DM LOW
1	0	LOW	X	output value from DAT/VP to DP and DM
X	X	HIGH	X	high-Z
X	1	X	X	high-Z

[1] Can be controlled by using either the SUSPEND pin or the SUSPEND\_REG bit.

**Table 10: USB functional mode: transmit operation**

USB mode	Input pin		Output pin	
	DAT/VP	SE0/VM	DP	DM
DAT_SE0	LOW	LOW	LOW	HIGH
	HIGH	LOW	HIGH	LOW
	LOW	HIGH	LOW	LOW
	HIGH	HIGH	LOW	LOW
VP_VM	LOW	LOW	LOW	LOW
	HIGH	LOW	HIGH	LOW
	LOW	HIGH	LOW	HIGH
	HIGH	HIGH	HIGH	HIGH

### 10.2 Differential receiver

[Table 11](#) describes the operation of the differential receiver. The register bits and the pins used in the column heading are described in [Section 11.1](#) and [Section 8.9](#), respectively.

The detailed behavior of the receive transceiver operation is given in [Table 12](#).

**Table 11: Differential receiver operation settings**

Suspend <sup>[1]</sup>	Bit TRANSP_EN	Pin OE_N/INT_N	Bit DAT_SE0	Differential receiver
1	X	X	X	0
X	X	LOW	X	0
X	1	X	X	0
0	0	HIGH	1	output differential value from DP and DM to DAT/VP and RCV
0	0	HIGH	0	output differential value from DP and DM to RCV

[1] Can be controlled by using either the SUSPEND pin or the SUSPEND\_REG bit.

**Table 12: USB functional mode: receive operation**

USB mode	Suspend <sup>[1]</sup>	Input pin		Output pin		
		DP	DM	DAT/VP	SE0/VM	RCV
DAT_SE0	0	LOW	LOW	RCV	HIGH	last value of RCV
DAT_SE0	0	HIGH	LOW	HIGH	LOW	HIGH
DAT_SE0	0	LOW	HIGH	LOW	LOW	LOW
DAT_SE0	0	HIGH	HIGH	RCV	LOW	last value of RCV
DAT_SE0	1	LOW	LOW	LOW	HIGH	LOW
DAT_SE0	1	HIGH	LOW	HIGH	LOW	LOW
DAT_SE0	1	LOW	HIGH	LOW	LOW	LOW
DAT_SE0	1	HIGH	HIGH	HIGH	LOW	LOW
VP_VM	0	LOW	LOW	LOW	LOW	last value of RCV
VP_VM	0	HIGH	LOW	HIGH	LOW	HIGH
VP_VM	0	LOW	HIGH	LOW	HIGH	LOW
VP_VM	0	HIGH	HIGH	HIGH	HIGH	last value of RCV
VP_VM	1	LOW	LOW	LOW	LOW	LOW
VP_VM	1	HIGH	LOW	HIGH	LOW	LOW
VP_VM	1	LOW	HIGH	LOW	HIGH	LOW
VP_VM	1	HIGH	HIGH	HIGH	HIGH	LOW

[1] Can be controlled by using either the SUSPEND pin or the SUSPEND\_REG bit.



## 11. Serial controller

### 11.1 Register map

Table 13 provides an overview of the serial controller registers.

Table 13: Serial controller registers

Register	Width (bits)	Access <sup>[1]</sup>	Memory address	Functionality	Reference
Vendor ID	16	R	00–01H	device identification registers	Section 11.1.1 on page 17
Product ID	16	R	02–03H		
Version ID	16	R	14–15H		
Mode Control 1	8	R/S/C	<b>Set</b> — 04H <b>Clear</b> — 05H	mode control registers	Section 11.1.2 on page 18
Mode Control 2	8	R/S/C	<b>Set</b> — 12H <b>Clear</b> — 13H		
OTG Control	8	R/S/C	<b>Set</b> — 06H <b>Clear</b> — 07H	OTG registers	Section 11.1.3 on page 19
OTG Status	8	R	10H		
Interrupt Source	8	R	08H	interrupt related registers	Section 11.1.4 on page 20
Interrupt Latch	8	R/S/C	<b>Set</b> — 0AH <b>Clear</b> — 0BH		
Interrupt Enable Low	8	R/S/C	<b>Set</b> — 0CH <b>Clear</b> — 0DH		
Interrupt Enable High	8	R/S/C	<b>Set</b> — 0EH <b>Clear</b> — 0FH		

[1] The R/S/C access type represents a field that can be read, set or cleared (set to 0). A register can be read from either of the indicated addresses—set or clear. Writing logic 1 to the set address causes the associated bit to be set. Writing logic 1 to the clear address causes the associated bit to be cleared. Writing logic 0 to an address has no effect.

#### 11.1.1 Device identification registers

**Vendor ID register (Read: 00H–01H):** Table 14 provides the bit allocation of the Vendor ID register.

Table 14: Vendor ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	VENDORID [15:0]	R	04CCH	Philips Semiconductors' Vendor ID

**Product ID register (Read: 02H–03H):** The bit allocation of this register is given in Table 15.

Table 15: Product ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	PRODUCTID [15:0]	R	1301H	Product ID of the ISP1301

**Version ID register (Read: 14H–15H):** Table 16 shows the bit allocation of this register.

**Table 16: Version ID register: bit description**

Bit	Symbol	Access	Value	Description
15 to 0	VERSIONID [15:0]	R	0210H	Version number of the ISP1301

### 11.1.2 Mode control registers

**Mode Control 1 register (Set/Clear: 04H/05H):** The bit allocation of the Mode Control 1 register is given in Table 17.

**Table 17: Mode Control 1 register: bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	-	UART_EN	OE_INT_EN	BDIS_ACON_EN	TRANSP_EN	DAT_SE0	SUSPEND_REG	SPEED_REG
Reset	-	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

**Table 18: Mode Control 1 register: bit description**

Bit	Symbol	Description
7	-	reserved
6	UART_EN	When set, the ATX is in the transparent UART mode.
5	OE_INT_EN	When set and when in the suspend mode, pin OE_N/INT_N becomes an output and is asserted when an interrupt occurs.
4	BDIS_ACON_EN	Enables the A-device to connect if the B-device disconnect is detected; see Section 11.3
3	TRANSP_EN	When set, the ATX is in the transparent mode.
2	DAT_SE0	0 — VP_VM mode 1 — DAT_SE0 mode; see Table 6 and Table 7
1	SUSPEND_REG	Sets the ISP1301 in the suspend mode, if bit SPD_SUSP_CTRL = 1.  0 — active-power mode 1 — USB suspend mode
0	SPEED_REG	Sets the rise time and the fall time of the transmit driver in USB modes, if bit SPD_SUSP_CTRL = 1.  0 — USB low-speed mode 1 — USB full-speed mode

**Mode Control 2 register (Set/Clear: 12H/13H):** For the bit allocation of this register, see Table 19.

Table 19: Mode Control 2 register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	EN2V7	PSW_OE	AUDIO_EN	TRANSP_BDIR1	TRANSP_BDIR0	BI_DI	SPD_SUSP_CTRL	GLOBAL_PWR_DN
Reset	0	0	0	0	0	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 20: Mode Control 2 register: bit description

Bit	Symbol	Description
7	EN2V7	<b>0</b> — $V_{BAT} = 3.0\text{ V}$ to $4.5\text{ V}$ <b>1</b> — $V_{BAT} = 2.7\text{ V}$ to $4.5\text{ V}$
6	PSW_OE	<b>0</b> — ADR/PSW pin acts as an input <b>1</b> — ADR/PSW pin is driven
5	AUDIO_EN	<b>0</b> — SE receiver is enabled; cr_int detector is disabled <b>1</b> — SE receiver is turned off (pin VP = LOW, pin VM = LOW); cr_int detector is enabled
4 to 3	TRANSP_BDIR[1:0]	controls the direction of data transfer in the transparent general-purpose buffer mode; see <a href="#">Table 8</a>
2	BI_DI	<b>0</b> — direction of DAT/VP and SE0/VM are fixed (transmit only) <b>1</b> — direction of DAT/VP and SE0/VM are controlled by pin OE_N/INT_N; see <a href="#">Table 6</a>
1	SPD_SUSP_CTRL	control of speed and suspend in USB modes: <b>0</b> — controlled by pins SPEED and SUSPEND <b>1</b> — controlled by bit SPEED_REG and bit SUSPEND_REG of the Mode Control 1 register
0	GLOBAL_PWR_DN	<b>0</b> — normal operation <b>1</b> — sets the ISP1301 to the power down mode Activities on the I <sup>2</sup> C-bus or any OTG event can wake up the chip; see <a href="#">Section 12</a>

### 11.1.3 OTG registers

**OTG Control register (Set/Clear: 06H/07H):** [Table 21](#) provides the bit allocation of the OTG Control register.

Table 21: OTG Control register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VBUS_CHRG	VBUS_DISCHRG	VBUS_DRV	ID_PULL_DOWN	DM_PULL_DOWN	DP_PULL_DOWN	DM_PULL_UP	DP_PULL_UP
Reset	0	0	0	0	1	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 22: OTG Control register: bit description

Bit	Symbol	Description
7	VBUS_CHRG	charge $V_{BUS}$ through a resistor to 3.3 V
6	VBUS_DISCHRG	discharge $V_{BUS}$ through a resistor to ground
5	VBUS_DRV	drive $V_{BUS}$ to 5 V through the charge pump
4	ID_PULLDOWN	connect the ID pin to ground
3	DM_PULLDOWN	connect DM pull-down resistor to ground
2	DP_PULLDOWN	connect DP pull-down resistor to ground
1	DM_PULLUP	connect DM pull-up resistor to 3.3 V
0	DP_PULLUP	connect DP pull-up resistor to 3.3 V

**OTG Status register (Read: 10H):** Table 23 shows the bit allocation of the OTG Status register.

Table 23: OTG Status register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	B_SESS_VLD	B_SESS_END	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 24: OTG Status register: bit description

Bit	Symbol	Description
7	B_SESS_VLD	set when the $V_{BUS}$ voltage is above the B-device session valid threshold (2.0 V to 4.0 V)
6	B_SESS_END	set when the $V_{BUS}$ voltage is below the B-device session end threshold (0.2 V to 0.8 V)
5 to 0	-	reserved

#### 11.1.4 Interrupt related registers

**Interrupt Source register (Read: 08H):** This register indicates the current state of the signals that can generate an interrupt. The bit allocation of the Interrupt Source register is given in Table 25.

Table 25: Interrupt Source register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 26: Interrupt Source register: bit description**

Bit	Symbol	Description
7	CR_INT	DP pin is above the car kit interrupt threshold (0.4 V to 0.6 V)
6	BDIS_ACON	set when bit BDIS_ACON_EN is set, and the ISP1301 asserts bit DP_PULLUP after detecting the B-device disconnect
5	ID_FLOAT	ID pin is floating
4	DM_HI	DM pin is HIGH
3	ID_GND	ID pin is connected to ground
2	DP_HI	DP pin is HIGH
1	SESS_VLD	session valid comparator; threshold = 0.8 V to 2.0 V
0	VBUS_VLD	A-device V <sub>BUS</sub> valid comparator; threshold > 4.4 V

**Interrupt Latch register (Set/Clear: 0AH/0BH):** This register indicates the source that generated the interrupt. The bit allocation of the Interrupt Latch register is given in [Table 27](#).

**Table 27: Interrupt Latch register: bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

**Table 28: Interrupt Latch register: bit description**

Bit	Symbol	Description
7	CR_INT	interrupt for CR_INT status change
6	BDIS_ACON	interrupt for BDIS_ACON status change
5	ID_FLOAT	interrupt for ID_FLOAT status change
4	DM_HI	interrupt for DM_HI status change
3	ID_GND	interrupt for ID_GND status change
2	DP_HI	interrupt for DP_HI status change
1	SESS_VLD	interrupt for SESS_VLD status change
0	VBUS_VLD	interrupt for VBUS_VLD status change

**Interrupt Enable Low register (Set/Clear: 0CH/0DH):** This register enables interrupts on transition from true to false. For the bit allocation of this register, see [Table 29](#).

**Table 29: Interrupt Enable Low register: bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

**Table 30: Interrupt Enable Low register: bit description**

Bit	Symbol	Description
7	CR_INT	interrupt enable for CR_INT status change from 1 to 0
6	BDIS_ACON	interrupt enable for BDIS_ACON status change from 1 to 0
5	ID_FLOAT	interrupt enable for ID_FLOAT status change from 1 to 0
4	DM_HI	interrupt enable for DM_HI status change from 1 to 0
3	ID_GND	interrupt enable for ID_GND status change from 1 to 0
2	DP_HI	interrupt enable for DP_HI status change from 1 to 0
1	SESS_VLD	interrupt enable for SESS_VLD status change from 1 to 0
0	VBUS_VLD	interrupt enable for VBUS_VLD status change from 1 to 0

**Interrupt Enable High register (Set/Clear: 0EH/0FH):** The Interrupt Enable High register enables interrupts on transition from FALSE to TRUE. Table 31 provides the bit allocation of this register.

**Table 31: Interrupt Enable High register: bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

**Table 32: Interrupt Enable High register: bit description**

Bit	Symbol	Description
7	CR_INT	interrupt enable for CR_INT status change from 0 to 1
6	BDIS_ACON	interrupt enable for BDIS_ACON status change from 0 to 1
5	ID_FLOAT	interrupt enable for ID_FLOAT status change from 0 to 1
4	DM_HI	interrupt enable for DM_HI status change from 0 to 1
3	ID_GND	interrupt enable for ID_GND status change from 0 to 1
2	DP_HI	interrupt enable for DP_HI status change from 0 to 1
1	SESS_VLD	interrupt enable for SESS_VLD status change from 0 to 1
0	VBUS_VLD	interrupt enable for VBUS_VLD status change from 0 to 1

## 11.2 Interrupts

Table 26 indicates the signals that can generate interrupts. Any of the signals given in Table 26 can generate an interrupt when the signal becomes either LOW or HIGH. After an interrupt has been generated, the OTG controller should be able to read the status of each signal and the bit that indicates whether or not that signal generated the interrupt.

A bit in the Interrupt Latch register is set when any of these occurs:

- Writing logic 1 to its set address causes the corresponding bit to be set
- The corresponding bit in the Interrupt Enable High register is set, and the associated signal changes from LOW to HIGH
- The corresponding bit in the Interrupt Enable Low register is set, and the associated signal changes from HIGH to LOW.

The Interrupt Latch register bit is cleared by writing logic 1 to its clear address.

### 11.3 Autoconnect

The Host Negotiation Protocol (HNP) in the OTG supplement specifies the following sequence of events to transfer the role of the host from the A-device to the B-device:

1. The A-device puts the bus in the suspend state
2. The B-device simulates a disconnect by deasserting its DP pull-up
3. The A-device detects SE0 on the bus, and asserts its DP pull-up
4. The B-device detects that the DP line is HIGH, and takes the role of the host.

The OTG supplement specifies that the time between the B-device deasserting its DP pull-up and the A-device asserting its pull-up must be less than 3 ms. For an A-device with a slow interrupt response time, 3 ms may not be enough time to write an I<sup>2</sup>C-bus command to the ISP1301 to assert the DP pull-up. An alternative method is for the A-device transceiver to automatically assert the DP pull-up after detecting an SE0 from the B-device.

The sequence of events is as follows:

After finishing data transfers between the A-device and the B-device and before suspending the bus, the A-device sends SOFs. The B-device receives these SOFs, and does not transmit any packet back to the A-device. During this time, the A-device sets the BDIS\_ACON\_EN bit in the ISP1301. This enables the ISP1301 to look for SE0 whenever the A-device is not transmitting (that is, whenever the OE\_N/INT\_N pin of the ISP1301 is not asserted). After the BDIS\_ACON\_EN bit is set, the A-device stops transmitting SOFs and allows the bus to go to the idle state. If the B-device disconnects, the bus goes to SE0, and the ISP1301 logic automatically turns on the A-device pull-up.

## 12. Clock wake up scheme

This section explains the ISP1301 clock stop timing, events triggering the clock to wake up, and the timing of the clock wake up.

### 12.1 Power down event

The clock is stopped when the GLOBAL\_PWR\_DN bit is set. It takes approximately 8 ms for the clock to stop from the time the power down condition is detected. The clock always stops at its falling edge. The waveform is given in [Figure 6](#).

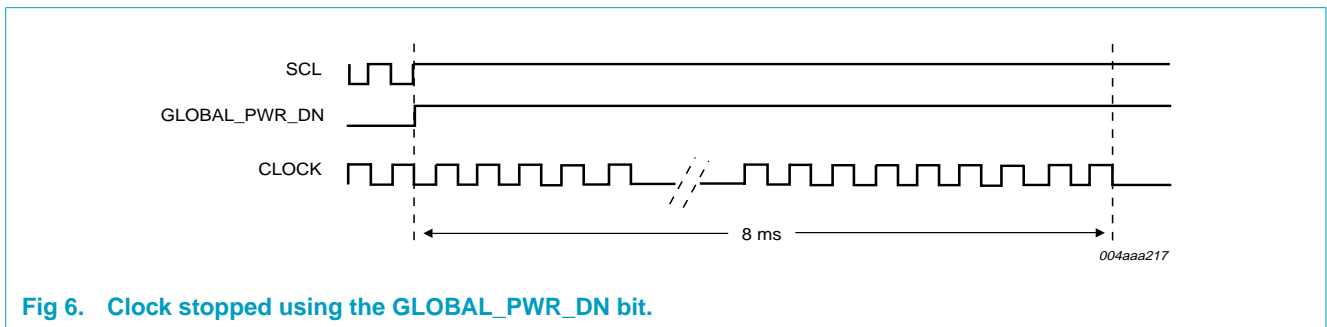


Fig 6. Clock stopped using the GLOBAL\_PWR\_DN bit.

### 12.2 Clock wake up events

The clock wakes up when any of the following events occur on the ISP1301 pins:

- SCL goes LOW
- $V_{BUS}$  goes above the session valid threshold (0.8 V to 2.0 V), provided the SESS\_VLD bit in the Interrupt Enable High register is set.
- ID changes when mini-A plug is inserted, provided the ID\_FLOAT bit in the Interrupt Enable Low register is set.
- ID changes when mini-A plug is removed, provided the ID\_FLOAT bit in the Interrupt Enable High register is set.
- DP goes HIGH, provided the DP\_HI bit in the Interrupt Enable High register is set.
- DM goes HIGH, provided the DM\_HI bit in the Interrupt Enable High register is set.

The event triggers the clock to start and a stable clock is guaranteed after about six clock periods, which is approximately 8  $\mu$ s. The startup analog clock time is 10  $\mu$ s. Therefore, the total estimated start time after a triggered event is about 20  $\mu$ s. The clock will always start at its rising edge.

Waveforms of the clock wake up because of different events are given in [Figure 7](#), [Figure 8](#), [Figure 9](#), [Figure 10](#) and [Figure 11](#).

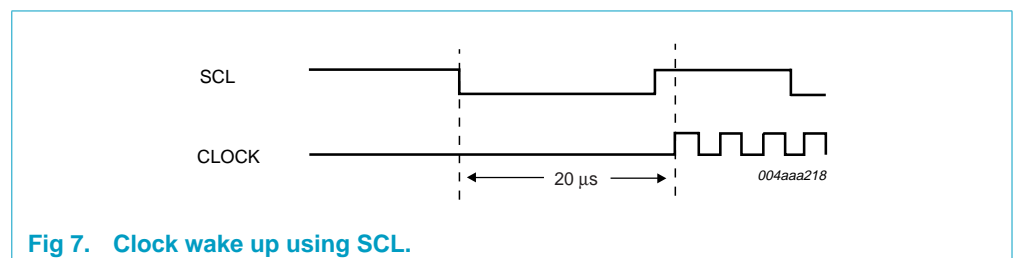


Fig 7. Clock wake up using SCL.



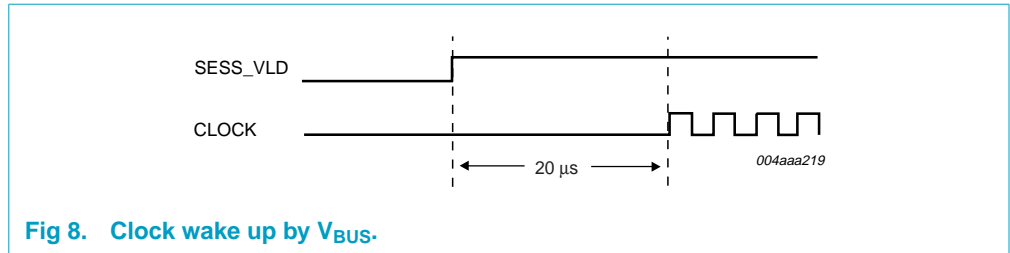


Fig 8. Clock wake up by VBUS.

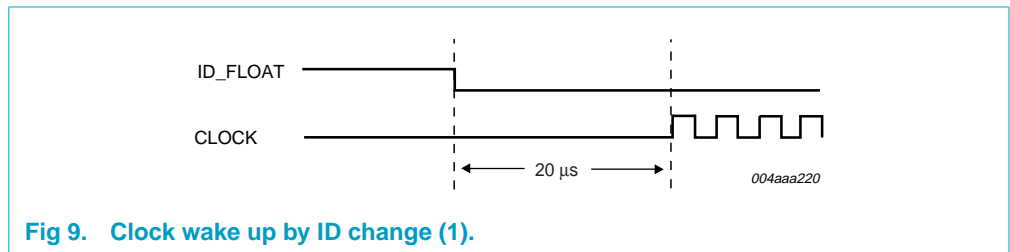


Fig 9. Clock wake up by ID change (1).

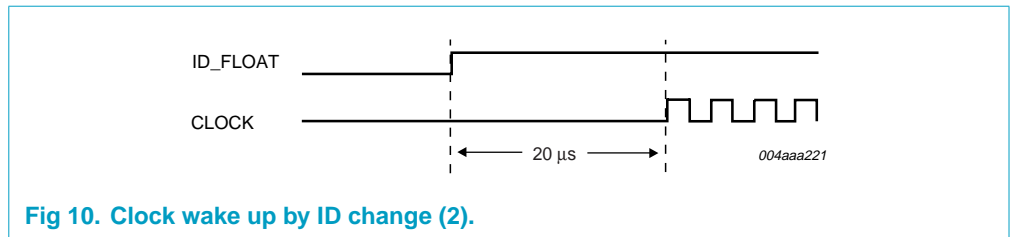


Fig 10. Clock wake up by ID change (2).

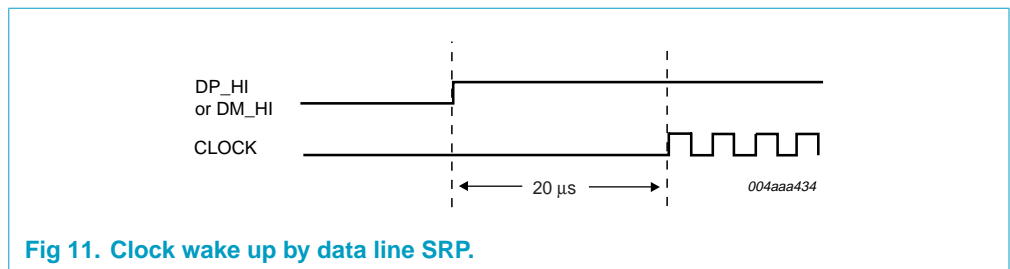


Fig 11. Clock wake up by data line SRP.

When an event is triggered and the clock is started, it will remain active for 8 ms. If the GLOBAL\_PWR\_DN bit is not cleared within this 8 ms period, the clock will stop. If the clock wakes up because of any event other than SCL going LOW, an interrupt will be generated once the clock is active.

## 13. I<sup>2</sup>C-bus protocol

For detailed information, refer to *The I<sup>2</sup>C-bus specification; version 2.1*.

### 13.1 I<sup>2</sup>C-bus byte transfer format

Table 33: I<sup>2</sup>C-bus byte transfer format<sup>[1]</sup>

S	Byte 1	A	Byte 2	A	Byte 3	A	...	A	P
	8 bits		8 bits		8 bits		...		

[1] S = Start; A = Acknowledge; P = Stop.

### 13.2 I<sup>2</sup>C-bus device address

Table 34: Device address byte 1

Bit	7	6	5	4	3	2	1	0
	device address							-
Name	A6	A5	A4	A3	A2	A1	A0	R/W
Value	0	1	0	1	1	0	X	X

Table 35: Bit description

Bit	Symbol	Description
7 to 1	A[6:0]	<b>Device address:</b> The device address of the ISP1301 is: 0101 10 (A0). The value of A0 (LSB) is loaded from pin ADR/PSW during reset (including power-on reset). If pin ADR/PSW = HIGH, bit A0 = 1; otherwise bit A0 = 0.
0	R/W	Read/write command.  0 — write 1 — read.

### 13.3 Write format

A write operation can be performed as:

- One-byte write to the specified register address
- Multi-byte write to N consecutive registers, starting from the specified start address. N defines the number of registers to write. If N = 1, only the start register is written.

#### 13.3.1 One-byte write

Figure 12 illustrates the byte sequence.

Table 36: Transfer format description for one-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits address of register K

**Table 36: Transfer format description for one-byte write...continued**

Byte	Description
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
P	master generates a STOP condition

### 13.3.2 Multiple-byte write

Figure 12 illustrates the byte sequence.

**Table 37: Transfer format description for multiple-byte write**

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits address of register K. This is the start address for writing multiple data bytes to consecutive registers. After a byte is written, the register address is automatically incremented by 1. <b>Remark:</b> If the master writes to a non-existent register, the slave must send a 'not ACK' and also must not increment the index address.
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
Write data K + 1	master writes data to register K + 1
ACK	slave generates an acknowledgment
:	:
Write data K + N - 1	master writes data to register K + N - 1. When the incremented address K + N - 1 becomes > 255, the register address rolls over to 0. Therefore, it is possible that some registers may be overwritten, if the transfer is not stopped before the rollover.
ACK	slave generates an acknowledgment
P	master generates a STOP condition

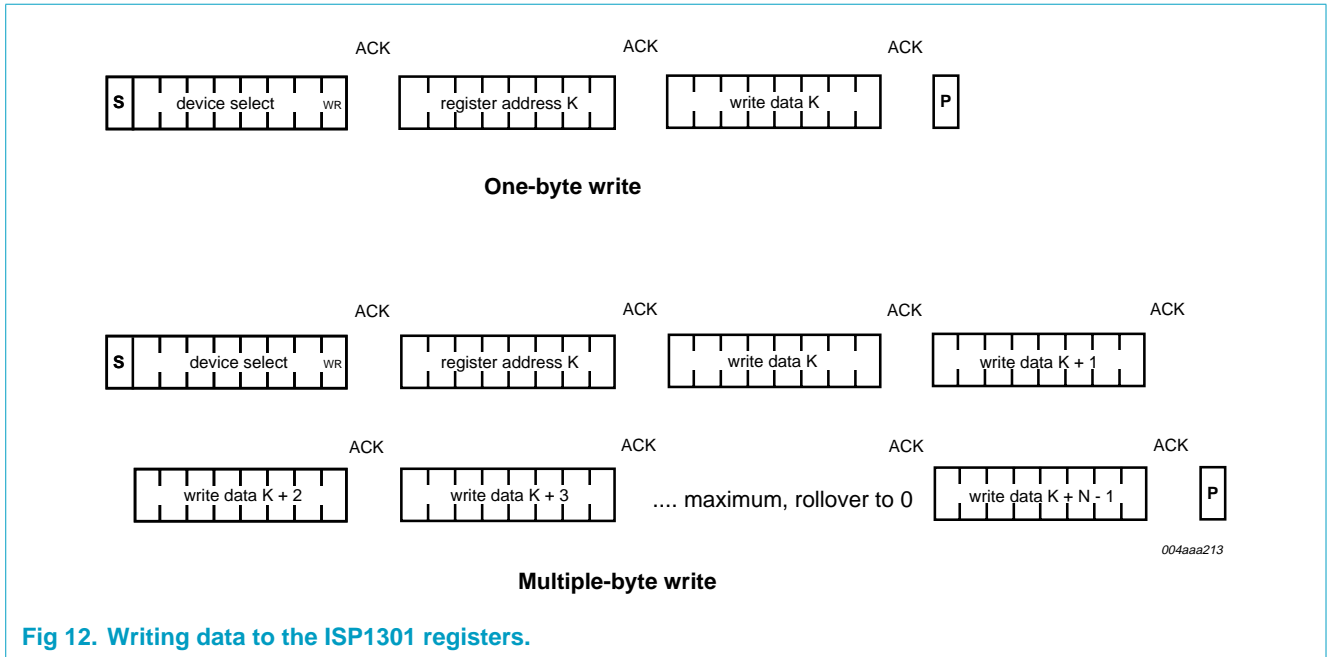


Fig 12. Writing data to the ISP1301 registers.

### 13.4 Read format

A read operation can be performed in two ways:

- Current address read: to read the register at the current address.
  - Single register read.
- Random address read: to read N registers starting at a specified address. N defines the number of registers to be read. If N = 1, only the start register is read.
  - Single register read
  - Multiple register read.

#### 13.4.1 Current address read

Figure 13 illustrates the byte sequence.

Table 38: Transfer format description for current address read

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. If the start address is not specified, the read operation starts from where the index register is pointing to because of a previous read or write operation.
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a stop condition

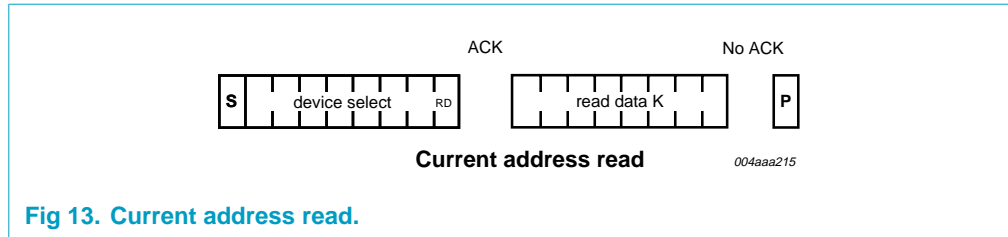


Fig 13. Current address read.

13.4.2 Random address read

Single read: Figure 14 illustrates the byte sequence.

Table 39: Transfer format description for single-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits device address and writes command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K to be read from
ACK	slave generates an acknowledgment
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a STOP condition

Multiple read: Figure 14 illustrates the byte sequence.

Table 40: Transfer format description for multiple-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K to be read from
ACK	slave generates an acknowledgment
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. After a byte is read, the address is automatically incremented by 1.
ACK	slave generates an acknowledgment
Read data K + 1	slave transmits and master reads data from register K + 1
ACK	slave generates an acknowledgment
:	:
Read data K + N - 1	slave transmits and master reads data register K + N - 1. This is the last register to read. After incrementing, the address rolls over to 0. Here, N represents the number of addresses available in the slave.
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a STOP condition

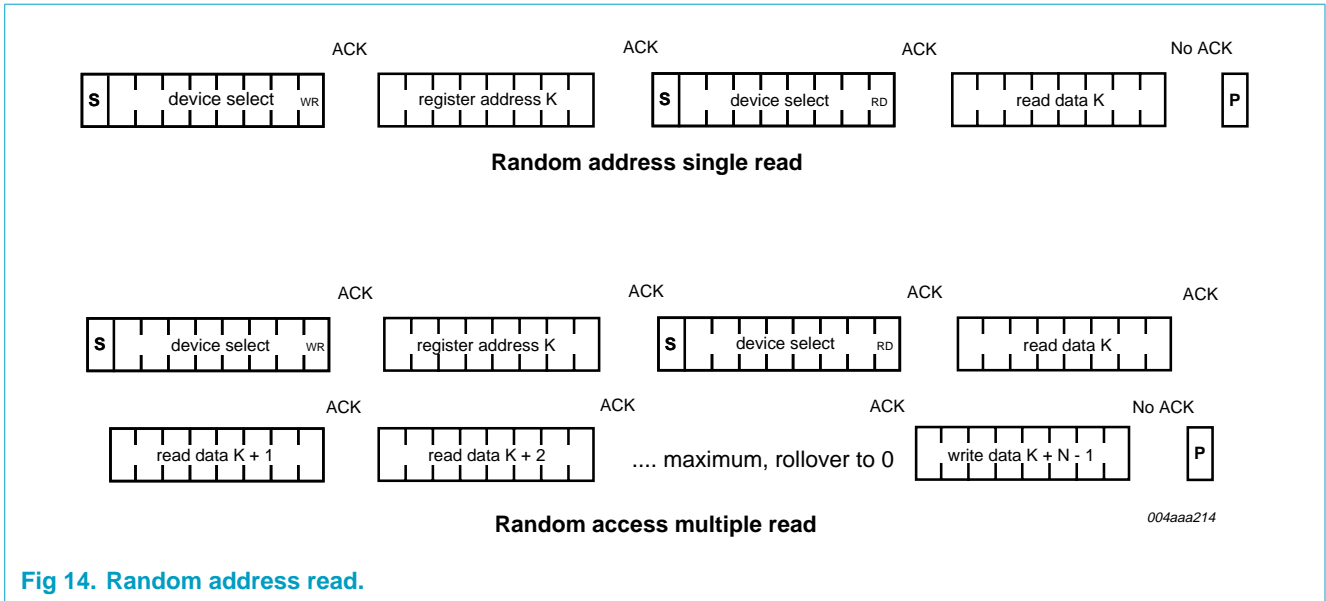


Fig 14. Random address read.

## 14. Limiting values

**Table 41: Absolute maximum ratings**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{BAT}$	supply voltage		-0.5	+5.5	V
$V_{DD\_LGC}$	I/O supply voltage		-0.5	+4.6	V
$V_I$	input voltage	$V_I = -1.8\text{ V to }+5.4\text{ V}$	-0.5	$V_{DD\_LGC} + 0.5$	V
$I_{lu}$	latch-up current		-	100	mA
$V_{esd}$	electrostatic discharge voltage	$I_{LI} < 1\ \mu\text{A}$			
		pins DP, DM, ID, $V_{BUS}$ , AGND, CGND and DGND	[1] -8	+8	kV
		all other pins	-2	+2	kV
$T_{stg}$	storage temperature		-60	+125	°C

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  resistor (Human Body Model). A 4.7  $\mu\text{F}$  capacitor is needed from  $V_{REG(3V3)}$  and  $V_{BUS}$  to ground.

## 15. Recommended operating conditions

**Table 42: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BAT}$	supply voltage		2.7	-	4.5	V
$V_{DD\_LGC}$	I/O supply voltage		[1] 1.65	-	3.6	V
$V_I$	input voltage		0	-	$V_{DD\_LGC}$	V
$V_{I(AI/O)}$	input voltage on analog I/O pins DP and DM		0	-	3.6	V
$V_{O(OD)}$	open-drain output pull-up voltage on pins SCL, SDA and INT_N		0	-	3.6	V
$T_{amb}$	ambient temperature		-40	-	+85	°C

[1]  $V_{DD\_LGC}$  should be less than or equal to  $V_{BAT}$ .

## 16. Static characteristics

**Table 43: Static characteristics: supply pins**

$V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Charge pump disabled</b>						
$V_{REG(3V3)}$	regulated supply voltage output	$V_{BAT} = 3.0\text{ V to }4.5\text{ V}$	[1] 3.0	-	3.6	V
		$V_{BAT} = 2.7\text{ V to }3.0\text{ V}$	2.7	-	3.0	V
$I_{BAT}$	operating supply current	transmitting and receiving at 12 Mbit/s; $C_L = 50\text{ pF}$ on pins DP and DM	[2] -	4	8	mA
$I_{DD\_LGC}$	operating I/O supply current	transmitting and receiving at 12 Mbit/s	[2] -	1	2	mA
$I_{BAT(idle)}$	supply current during full-speed idle and SE0	idle: $V_{DP} > 2.7\text{ V}$ , $V_{DM} < 0.3\text{ V}$ ; SE0: $V_{DP} < 0.3\text{ V}$ , $V_{DM} < 0.3\text{ V}$	[3] -	-	300	$\mu\text{A}$
$I_{DD\_LGC(static)}$	static I/O supply current	idle, SE0 or suspend	-	-	20	$\mu\text{A}$
$I_{BAT(pd)}$	power down mode supply current	bit GLOBAL_PWR_DN = 1	[3] -	-	20	$\mu\text{A}$
<b>Charge pump enabled</b>						
$I_{BAT(cp)}$	operating supply current for the charge pump	$I_{LOAD} = 8\text{ mA}$ ; ATX is idle	-	-	20	mA
		$I_{LOAD} = 0\text{ mA}$ ; ATX is idle	-	-	300	$\mu\text{A}$

[1] In the suspend mode, the minimum voltage is 2.7 V.

[2] Maximum value characterized only, not tested in production.

[3] Excluding any load current to the 1.5 k $\Omega$  and 15 k $\Omega$  pull-up and pull-down resistors (200  $\mu\text{A}$  typical).

**Table 44: Static characteristics: digital pins**

$V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input levels</b>						
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD\_LGC}$	V
$V_{IH}$	HIGH-level input voltage		$0.6V_{DD\_LGC}$	-	-	V
<b>Output levels</b>						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 2\text{ mA}$	-	-	0.4	V
		$I_{OL} = 100\text{ }\mu\text{A}$	-	-	0.15	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 2\text{ mA}$	[1] $V_{DD\_LGC} - 0.4$	-	-	V
		$I_{OH} = 100\text{ }\mu\text{A}$	$V_{DD\_LGC} - 0.15$	-	-	V
<b>Leakage current</b>						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
<b>Open-drain outputs</b>						
$I_{OZ}$	OFF-state output current		-5	-	+5	$\mu\text{A}$
<b>Capacitance</b>						
$C_{IN}$	input capacitance	pin to GND	-	-	10	pF

[1] Not applicable for open-drain outputs.



**Table 45: Static characteristics: analog I/O pins DP and DM** $V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input levels</b>						
$V_{DI}$	differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2	-	-	V
$V_{CM}$	differential common mode voltage	includes $V_{DI}$ range	0.8	-	2.5	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
<b>Output levels</b>						
$V_{OL}$	LOW-level output voltage	$R_L$ of 1.5 k $\Omega$ to +3.6 V	-	-	0.3	V
$V_{OH}$	HIGH-level output voltage	$R_L$ of 15 k $\Omega$ to GND				
		$V_{BAT} = 3.0\text{ V to }4.5\text{ V}$	2.8	-	3.6	V
		$V_{BAT} = 2.7\text{ V to }3.0\text{ V}$	2.6	-	3.0	V
<b>Leakage current</b>						
$I_{LZ}$	OFF-state leakage current		-1	-	+1	$\mu\text{A}$
<b>Capacitance</b>						
$C_{IN}$	transceiver capacitance	pin to GND	-	-	10	pF
<b>Resistance</b>						
$R_{PD}$	pull-down resistor on pins DP and DM		14.25	-	24.8	k $\Omega$
$R_{PU\_DP}$	pull-up resistor on pin DP	bus idle	900	-	1575	$\Omega$
		bus driven	1425	-	3090	$\Omega$
$R_{PU\_DM}$	pull-up resistor on pin DM	bus idle	900	-	1575	$\Omega$
		bus driven	1425	-	3090	$\Omega$
$Z_{DRV}$	driver output impedance	steady-state drive	[1] 34	-	44	$\Omega$
$Z_{INP}$	input impedance		10	-	-	M $\Omega$
<b>Termination</b>						
$V_{TERM}$	termination voltage for the upstream port pull-up resistor ( $R_{PU}$ )		3.0	-	3.6	V

[1] Includes external series resistors of 33  $\Omega \pm 1\%$  each on DP and DM.**Table 46: Static characteristics: analog I/O pin ID** $V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Resistance</b>						
$R_{PU\_ID}$	pull-up resistor on pin ID to $V_{REG(3V3)}$		77	-	130	k $\Omega$
$R_{PD\_ID}$	impedance to GND	bit ID_PULLDOWN = 1	-	-	10	$\Omega$

**Table 46: Static characteristics: analog I/O pin ID...continued** $V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{A\_ID}$	A-device ID impedance to GND	bit ID_GND = 1	-	-	1	k $\Omega$
$R_{B\_ID}$	B-device ID impedance to GND	bit ID_FLOAT = 1	800	-	-	k $\Omega$
$R_{ACC\_ID}$	Accessory device ID impedance to GND	bit ID_GND = 0; bit ID_FLOAT = 0	20	-	200	k $\Omega$

**Table 47: Static characteristics: charge pump** $V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Current</b>						
$I_{LOAD}$	maximum load current	$C_{ext} = 100\text{ nF}$ ; $V_{BUS} = 4.7\text{ V}$	-	-	8.0	mA
<b>Voltage</b>						
$V_{BUS}$	regulated $V_{BUS}$ output voltage	$I_{LOAD} = 8\text{ mA}$ ; $C_{ext} = 100\text{ nF}$	4.65	5	5.25	V
$V_{BUS(LK)}$	$V_{BUS}$ leakage voltage	charge pump disabled	-	-	0.2	V
$V_{th(VBUSVLD)}$	$V_{BUS}$ valid threshold		4.4	-	4.65	V
$V_{th(SESEND)}$	$V_{BUS}$ session end comparator threshold		0.2	-	0.8	V
$V_{hys(SESEND)}$	$V_{BUS}$ session end comparator hysteresis		-	150	-	mV
$V_{th(SESSVLD)}$	$V_{BUS}$ session valid comparator threshold		0.8	-	2.0	V
$V_{hys(SESSVLD)}$	$V_{BUS}$ session valid comparator hysteresis		-	200	-	mV
$V_{th(BSESSVLD)}$	$V_{BUS}$ session valid comparator threshold	for the B-device	2.0	-	4.0	V
$V_{hys(BSESSVLD)}$	$V_{BUS}$ session valid comparator hysteresis	for the B-device	-	200	-	mV
E	efficiency when loaded	$I_{LOAD} = 8\text{ mA}$ ; $V_{BAT} = 3\text{ V}$	-	75	-	%
<b>Resistance</b>						
$R_{VBUS(PU)}$	$V_{BUS}$ pull-up resistor	connect to $V_{REG(3V3)}$ when $VBUS\_CHRG = 1$	460	-	1000	$\Omega$
$R_{VBUS(PD)}$	$V_{BUS}$ pull-down resistor	connect to GND when $VBUS\_DISCHRG = 1$	660	-	1200	$\Omega$
$R_{VBUS(IDLE\_A)}$	$V_{BUS}$ idle impedance for A-device	ID pin connected to GND	40	-	100	k $\Omega$

## 17. Dynamic characteristics

**Table 48: Dynamic characteristics: reset and clock**

$V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Reset</b>						
$t_{W(\text{RESET\_N})}$	pulse width on input RESET_N		10	-	-	$\mu\text{s}$
<b>Internal clock</b>						
$f_{\text{clk}}$	clock frequency	bit GLOBAL_PWR_DN = 0	700	1000	1300	kHz

**Table 49: Dynamic characteristics: digital I/O pins**

$V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_{PU} = 1.5\text{ k}\Omega$  on DP to  $V_{TERM}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{TOI}$	bus turnaround time (OE_N/INT_N to DAT/VP and SE0/VM)	output-to-input; see <a href="#">Figure 19</a>	0	-	5	ns
$t_{TIO}$	bus turnaround time (OE_N/INT_N to DAT/VP and SE0/VM)	input-to-output; see <a href="#">Figure 19</a>	0	-	5	ns

**Table 50: Dynamic characteristics: analog I/O pins DP and DM**

$V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_{PU} = 1.5\text{ k}\Omega$  on DP to  $V_{TERM}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Driver characteristics</b>						
$t_{FR}$	rise time	$C_L = 50\text{ pF to }125\text{ pF}$ ; 10 % to 90 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 15</a>	4	-	20	ns
$t_{FF}$	fall time	$C_L = 50\text{ pF to }125\text{ pF}$ ; 90 % to 10 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 15</a>	4	-	20	ns
FRFM	differential rise/fall time matching ( $t_{FR}/t_{FF}$ )	excluding the first transition from idle state	90	-	111.1	%
$V_{CRS}$	output signal crossover voltage	excluding the first transition from idle state; see <a href="#">Figure 16</a>	[1] 1.3	-	2.0	V
<b>Driver timing</b>						
$t_{PLH(\text{drv})}$	driver propagation delay (DAT/VP, SE0/VM to DP, DM)	LOW-to-HIGH; see <a href="#">Figure 16</a> and <a href="#">Figure 20</a>	-	-	18	ns
$t_{PHL(\text{drv})}$	driver propagation delay (DAT/VP, SE0/VM to DP, DM)	HIGH-to-LOW; see <a href="#">Figure 16</a> and <a href="#">Figure 20</a>	-	-	18	ns
$t_{PHZ}$	driver disable delay (OE_N/INT_N to DP, DM)	HIGH-to-OFF; see <a href="#">Figure 17</a> and <a href="#">Figure 21</a>	-	-	15	ns
$t_{PLZ}$	driver disable delay (OE_N/INT_N to DP, DM)	LOW-to-OFF; see <a href="#">Figure 17</a> and <a href="#">Figure 21</a>	-	-	15	ns
$t_{PZH}$	driver enable delay (OE_N/INT_N to DP, DM)	OFF-to-HIGH; see <a href="#">Figure 17</a> and <a href="#">Figure 21</a>	-	-	15	ns

**Table 50: Dynamic characteristics: analog I/O pins DP and DM...continued**

$V_{BAT} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{DD\_LGC} = 1.65\text{ V to }3.6\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_{PU} = 1.5\text{ k}\Omega$  on DP to  $V_{TERM}$ ;  $T_{amb} = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PZL}$	driver enable delay (OE_N/INT_N to DP, DM)	OFF-to-LOW; see Figure 17 and Figure 21	-	-	15	ns
<b>Receiver timing</b>						
<b>Differential receiver</b>						
$t_{PLH(rcv)}$	propagation delay (DP, DM to RCV)	LOW-to-HIGH; see Figure 18 and Figure 22	-	-	15	ns
$t_{PHL(rcv)}$	propagation delay (DP, DM to RCV)	HIGH-to-LOW; see Figure 18 and Figure 22	-	-	15	ns
<b>Single-ended receiver</b>						
$t_{PLH(se)}$	propagation delay (DP, DM to VP and DAT/VP, VM and SE0/VM)	LOW-to-HIGH; see Figure 18 and Figure 22	-	-	18	ns
$t_{PHL(se)}$	propagation delay (DP, DM to VP and DAT/VP, VM and SE0/VM)	HIGH-to-LOW; see Figure 18 and Figure 22	-	-	18	ns

[1] Characterized only; not tested. Limits guaranteed by design.

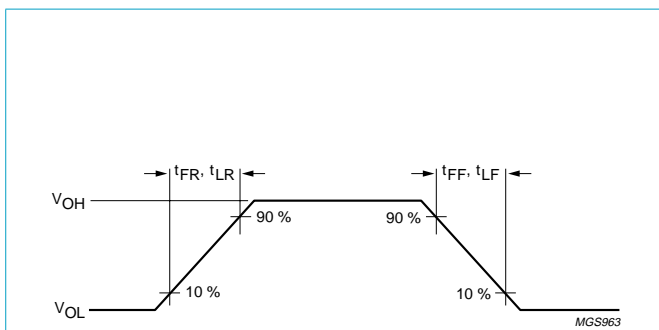


Fig 15. Rise and fall times.

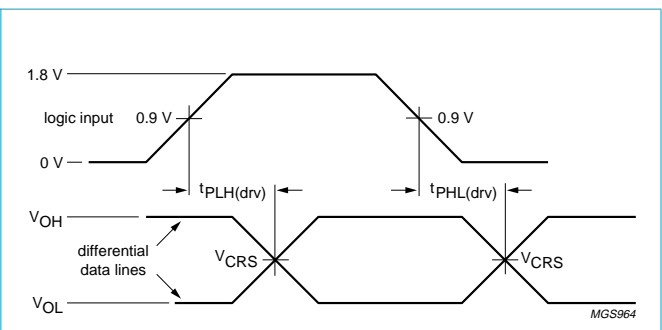


Fig 16. Timing of DAT/VP and SE0/VM to DP and DM.

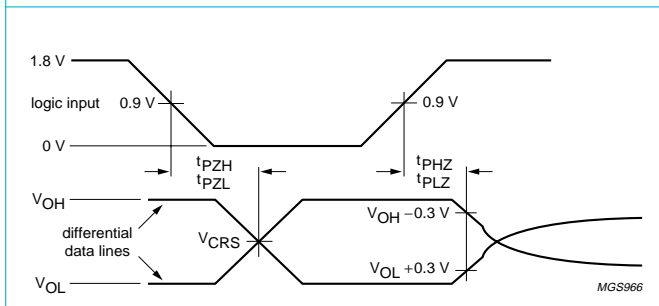


Fig 17. Timing of OE\_N/INT\_N to DP and DM.

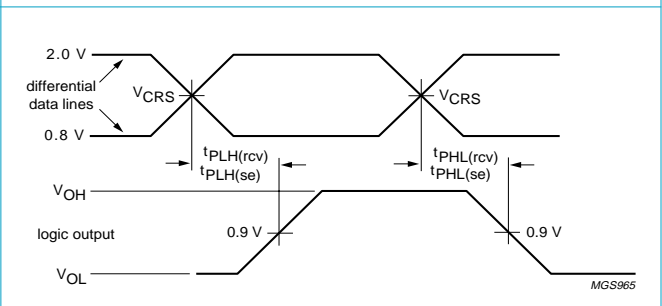


Fig 18. Timing of DP and DM to RCV, VP or DAT/VP and VM or SE0/VM.

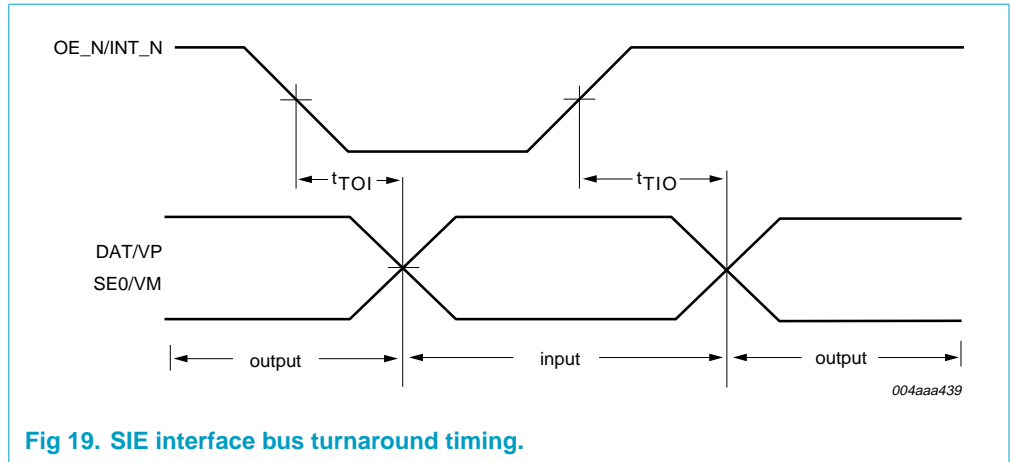


Fig 19. SIE interface bus turnaround timing.

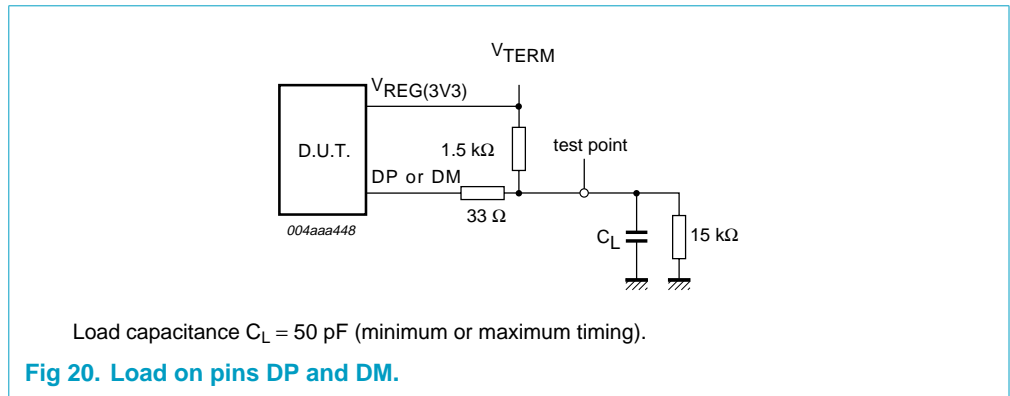


Fig 20. Load on pins DP and DM.

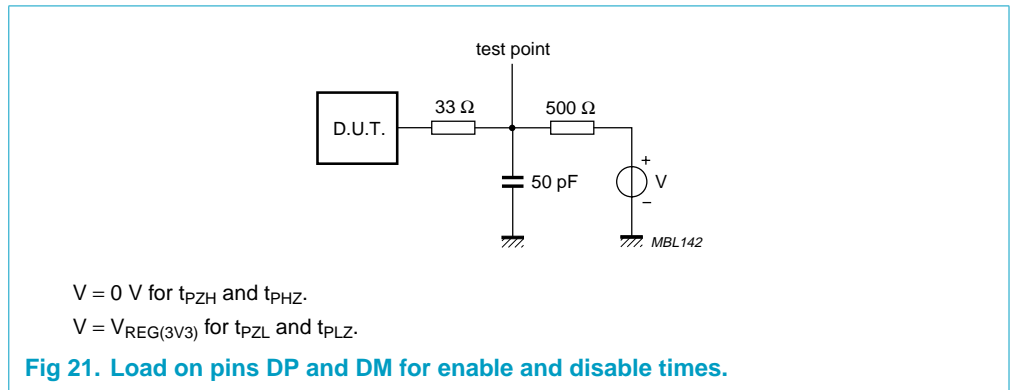


Fig 21. Load on pins DP and DM for enable and disable times.

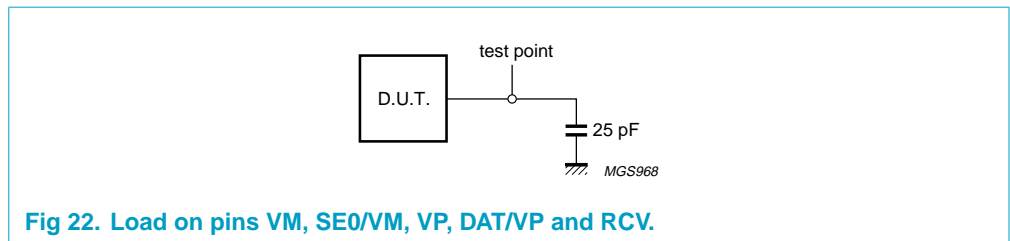


Fig 22. Load on pins VM, SE0/VM, VP, DAT/VP and RCV.

Table 51: Characteristics of I/O stages of I<sup>2</sup>C-bus lines (SDA, SCL)

Symbol	Parameter	Standard mode		Unit
		Min	Max	
$f_{SCL}$	SCL clock frequency	-	100	kHz
$t_{HD;STA}$	hold time for the START condition	4.0	-	$\mu$ s
$t_{LOW}$	LOW period of the SCL clock	4.7	-	$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock	4.0	-	$\mu$ s
$t_{SU;STA}$	set-up time for the START condition	4.7	-	$\mu$ s
$t_{SU;DAT}$	data set-up time	250	-	ns
$t_{HD;DAT}$	data hold time	0	-	$\mu$ s
$t_r$	rise time of SDA and SCL signals	-	1000	ns
$t_f$	fall time of SDA and SCL signals	-	300	ns
$t_{SU;STO}$	set-up time for the STOP condition	4.0	-	$\mu$ s
$t_{BUF}$	bus free time between a STOP and START condition	4.7	-	$\mu$ s

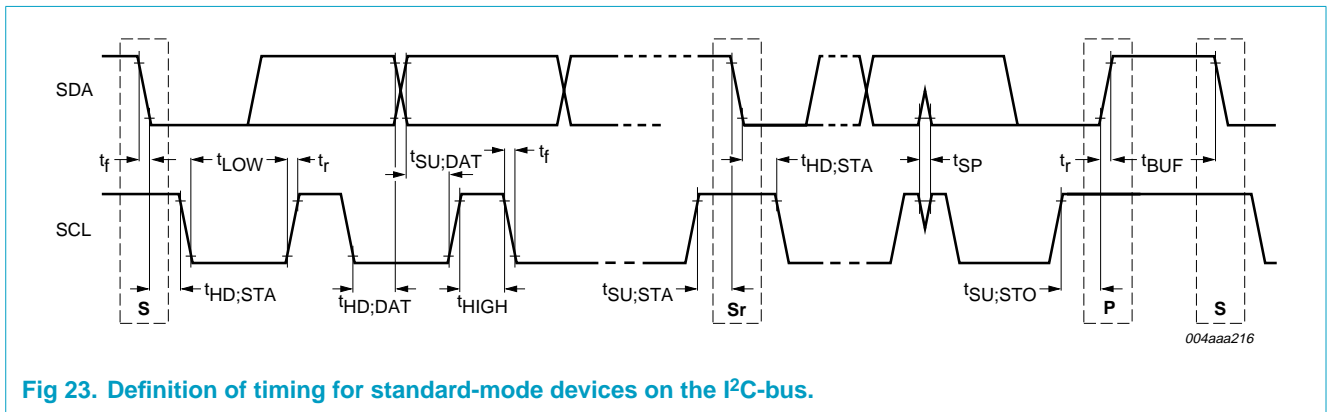


Fig 23. Definition of timing for standard-mode devices on the I<sup>2</sup>C-bus.

18. Application information

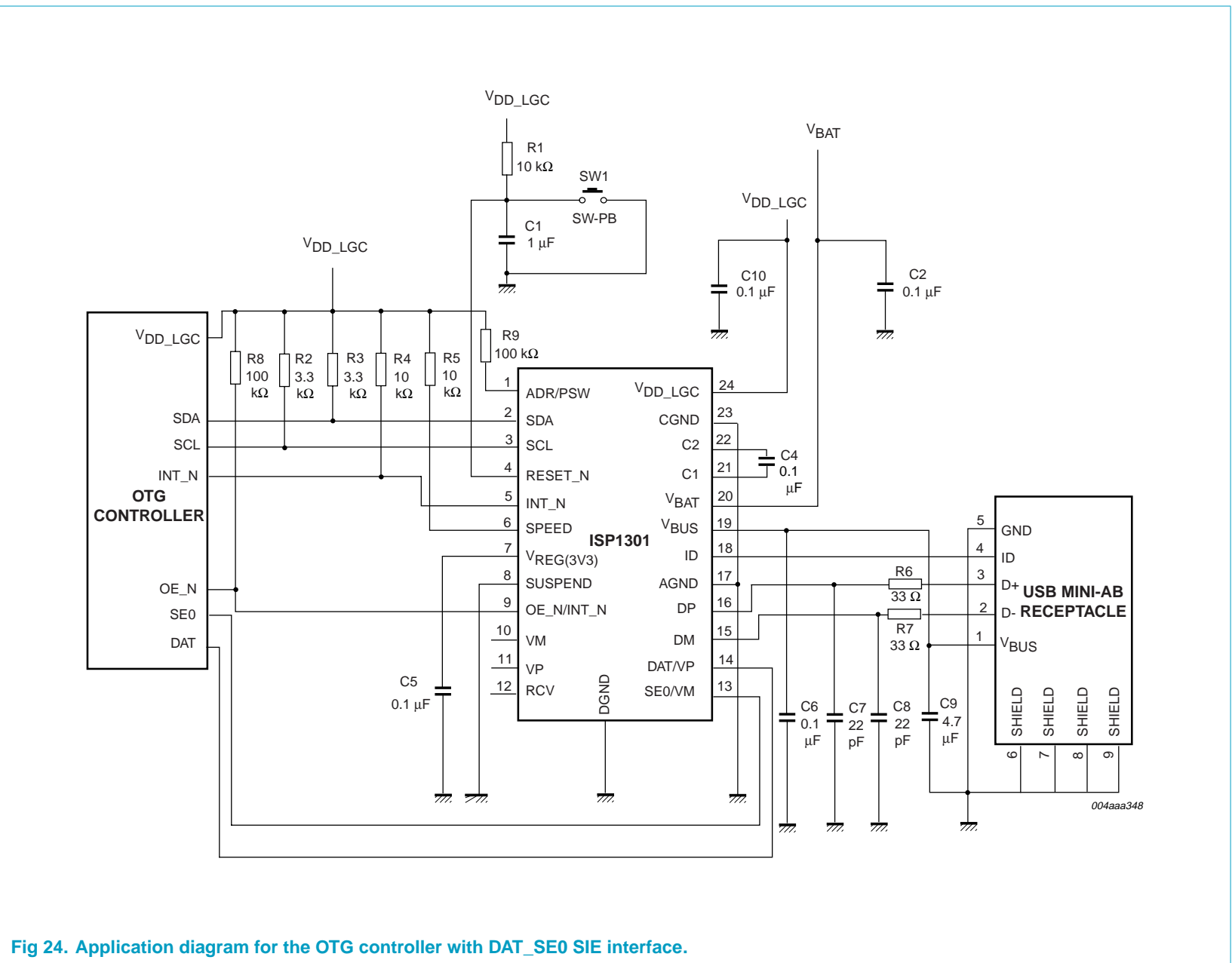
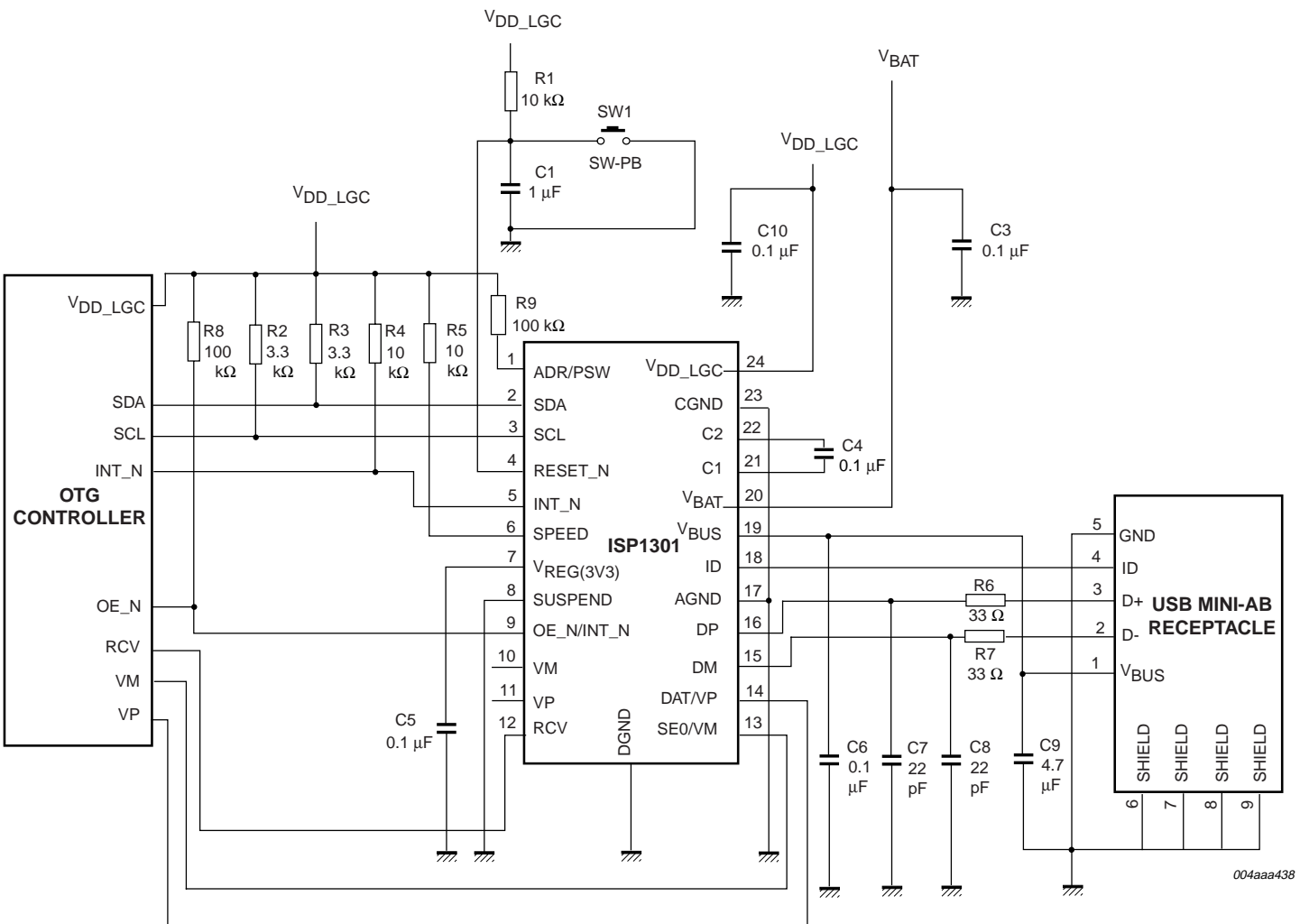


Fig 24. Application diagram for the OTG controller with DAT\_SE0 SIE interface.



004aaa438

Fig 25. Application diagram for the OTG controller with VP\_VM SIE interface.



19. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm

SOT616-1

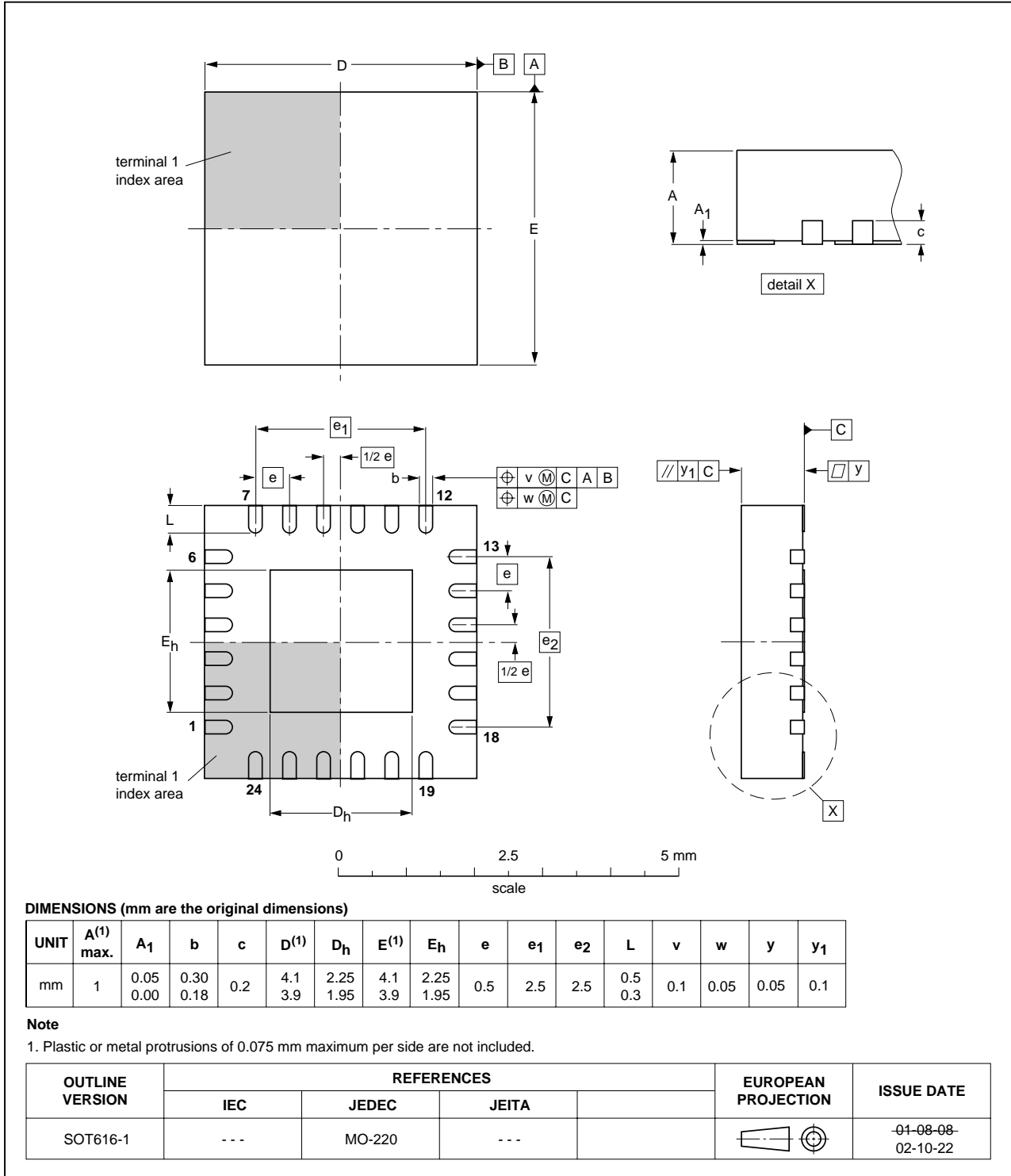


Fig 26. HVQFN24 package outline.

## 20. Soldering

### 20.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

### 20.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 20.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 20.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 20.5 Package related soldering information

**Table 52: Suitability of surface mount IC packages for wave and reflow soldering methods**

Package <sup>[1]</sup>	Soldering method	
	Wave	Reflow <sup>[2]</sup>
BGA, HTSSON..T <sup>[3]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[3]</sup> , TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>[4]</sup>	suitable
PLCC <sup>[5]</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>[5][6]</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>[7]</sup>	suitable
CWQCCN..L <sup>[8]</sup> , PMFP <sup>[9]</sup> , WQCCN..L <sup>[8]</sup>	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 21. Revision history

Table 53: Revision history

Rev	Date	CPCN	Description
01	20040414	-	Product data (9397 750 11355).

## 22. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 23. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 26. Trademarks

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## Contact information

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