ISP1561

Hi-Speed USB PCI host controller

Rev. 01 — 06 February 2003 **Product data**

1. General description

The ISP1561 is a PCI-based, single-chip Universal Serial Bus (USB) Host Controller. It integrates two Original USB Open Host Controller Interface (OHCI) cores, one Hi-Speed USB Enhanced Host Controller Interface (EHCI) core and four transceivers that are compliant with Hi-Speed USB and Original USB. The functional parts of the ISP1561 are fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *Open Host Controller Interface Specifications Rev. 1.0a*, *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 0.95*, *PCI Local Bus Specification Rev. 2.2* and *PCI Bus Power Management Interface Specification Rev. 1.1*.

The integrated high performance USB transceivers enable the ISP1561 to handle all Hi-Speed USB transfer speed modes: high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s). The ISP1561 provides four downstream ports that enables simultaneous connections of USB devices at different speeds.

The ISP1561 provides three downstream port status indicators—GoodLink™ along with green and amber LEDs—to allow user-rich messages of the Root Hub downstream ports status, without requiring detailed port information to be reflected in the internal registers.

The ISP1561 is fully compatible with various operating system drivers, such as Microsoft® Windows® standard OHCI and EHCI drivers that are present in Windows 98 Second Edition (SE), Windows Millennium Edition (Me), Windows XP and Windows 2000.

The ISP1561 directly interfaces to any 32-bit, 33 MHz PCI bus. It has 5 V-tolerant PCI pins that can source 3.3 V. The PCI interface fully complies with *PCI Local Bus Specification, Rev. 2.2*.

The ISP1561 is ideally suited for use in Hi-Speed USB host-enabled motherboards, Hi-Speed USB host PCI add-on card applications, mobile applications, and embedded solutions.

To facilitate motherboard development, the ISP1561 can use the available 48 MHz clock signal to reduce the total cost of a solution. However, to reduce the electromagnetic interference (EMI), it is recommended that the 12 MHz clock is used in PCI add-on card designs.

1.1 Abbreviations

DID — Device ID

EHCI — Enhanced Host Controller Interface

EMI — electromagnetic interference

HC — Host Controller

HCCA — Host Controller Communication Area

HCD — Host Controller Driver

OHCI — Open Host Controller Interface

PMC — Power Management Capabilities

PME — Power Management Event

PMCSR — Power Management Control/Status

USB — Universal Serial Bus

VID — Vendor ID.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
- Two Original USB OHCI cores comply with *Open Host Controller Interface Specification for USB Rev. 1.0a*
- One Hi-Speed USB EHCI core complies with *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 0.95*
- Supports PCI 32-bit, 33 MHz interface compliant with *PCI Local Bus Specification Rev. 2.2* with support for the $D3_{cold}$ standby and wake-up modes; all I/O pins are 3.3 V standard, but 5 V-tolerant
- Compliant with *PCI Bus Power Management Interface Specification Rev. 1.1* for all hosts (EHCI and OHCI), and supports all power states: D0, D1, D2, $D3_{hot}$ and $D3_{cold}$
- Four downstream ports with support for three types of downstream port indicator LEDs: GoodLink™, amber and green LEDs
- CLKRUN support for mobile applications, such as internal notebook design
- Configurable subsystem ID and subsystem Vendor ID through external EEPROM
- Configurable two or four port root hub
- Digital and analog power separation
- Supports hot Plug and Play and remote wake-up of peripherals
- Supports individual power switching and individual overcurrent protection for downstream ports
- Supports partial dynamic port-routing capability for downstream ports that allows sharing of the same physical downstream ports between the Original USB Host Controller and the Hi-Speed USB Host Controller
- Supports legacy PS/2 keyboards and mice
- Uses 12 MHz crystal oscillator to reduce system cost and EMI emissions
- Operates at +3.3 V power supply input
- Full industrial operating temperature range from –40 to +85 °C
- Full-scan design with high fault coverage (93% to 95%) ensures high quality
- LQFP128 package available.

3. Applications

- PC motherboard
- Notebook
- PCI add-on card
- Set-Top Box (STB)
- Web appliance.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1561BM	LQFP128	plastic low profile quad flat package; 128 leads; body 14 x 14 x 1.4 mm	SOT420-1

5. Block diagram

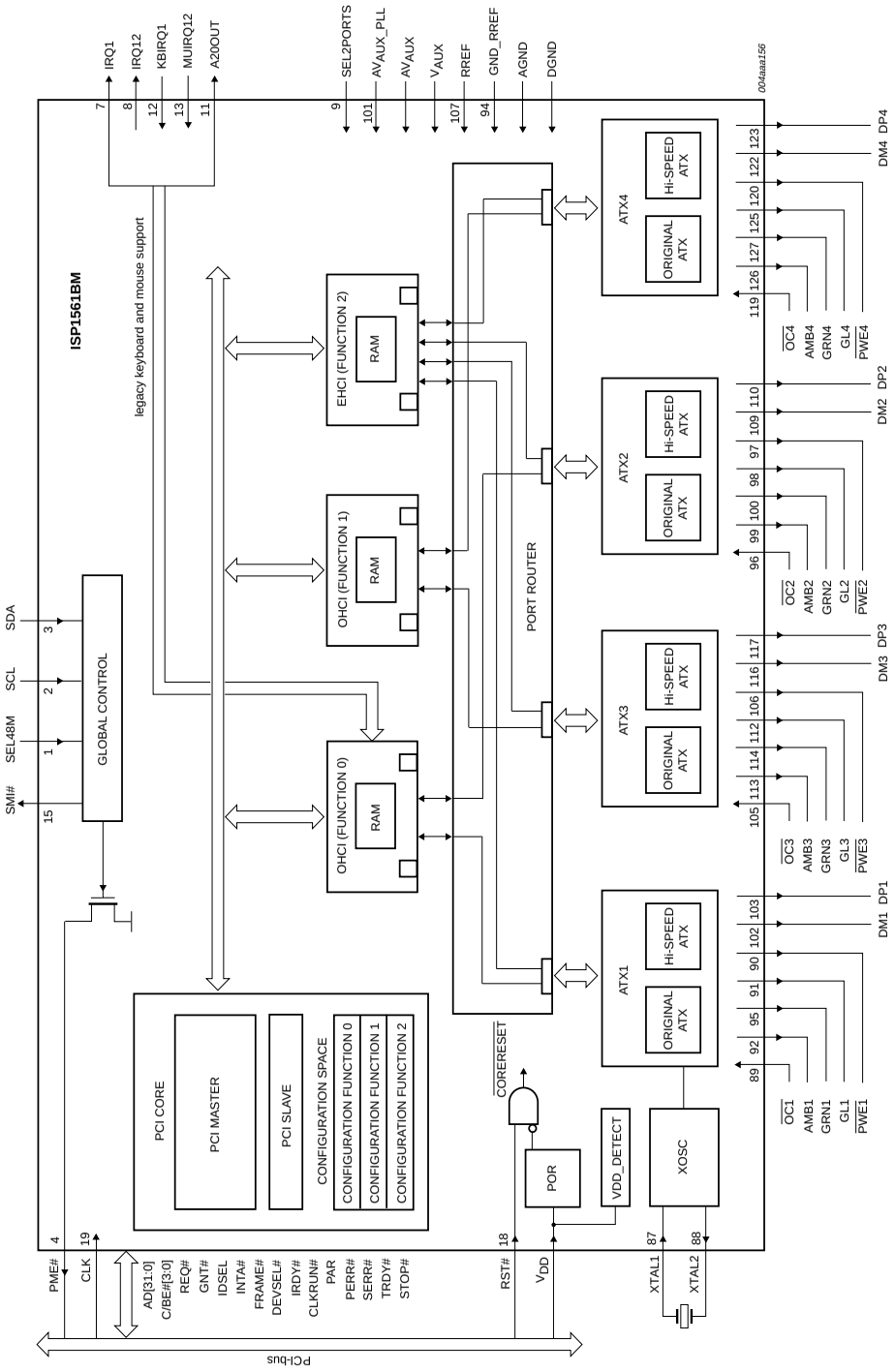


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

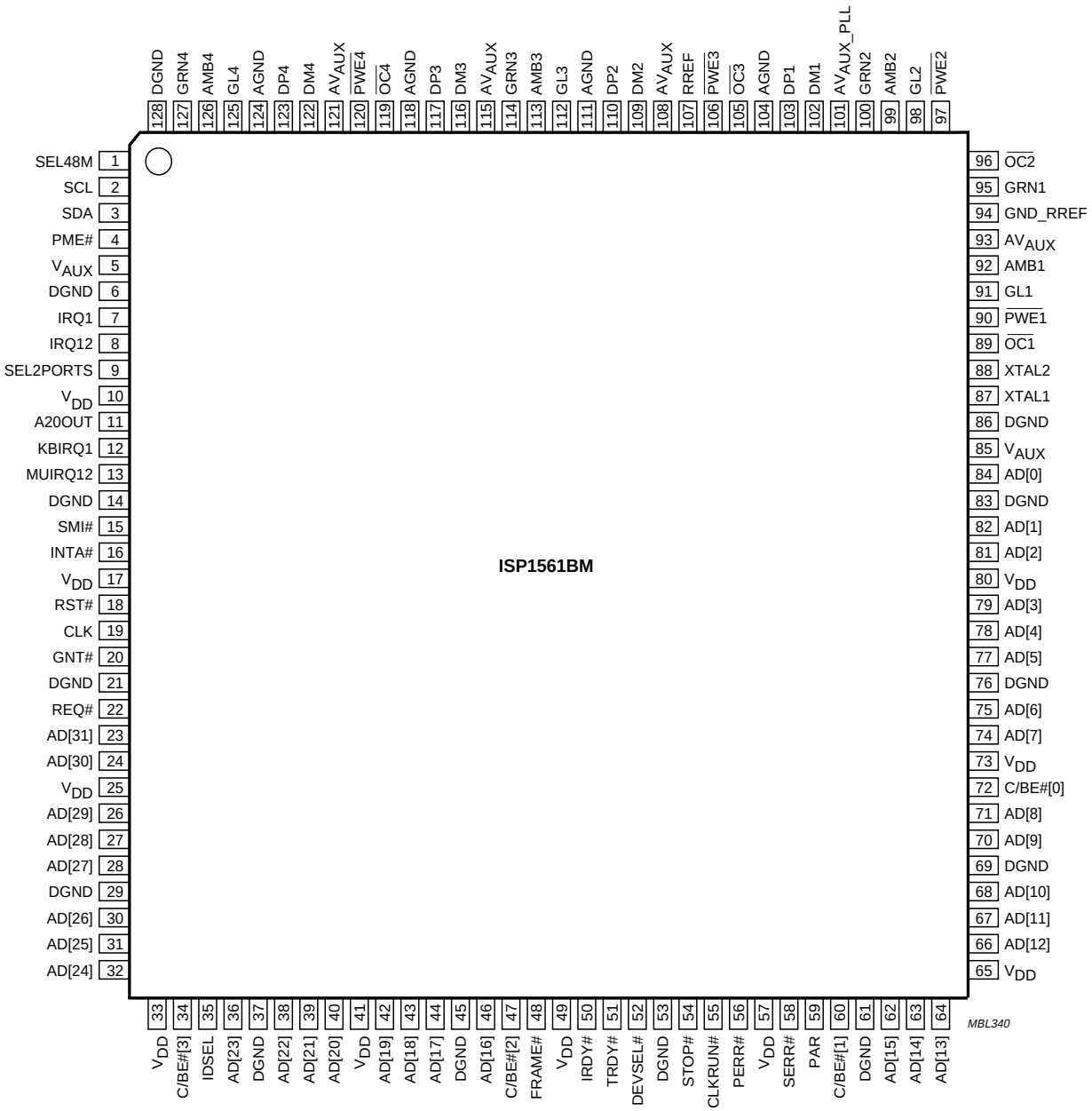


Fig 2. Pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol[1]	Pin	Type	Description
SEL48M	1	I	selection between 12 MHz crystal and 48 MHz oscillator; push-pull; TTL with hysteresis; 5 V tolerant **0 —** 12 MHz crystal is used **1 —** 48 MHz oscillator is used
SCL	2	O	I^2C-bus clock (open-drain)[2]
SDA	3	I/O	I^2C-bus data (open-drain)[2]
PME#	4	O	PCI Power Management Event; used by a device to request a change in the device or system power state; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
V_{AUX}	5	-	auxiliary voltage (3.3 V)
DGND	6	-	digital ground
IRQ1	7	O	system keyboard interrupt; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
IRQ12	8	O	system mouse interrupt; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
SEL2PORTS	9	I	active downstream port selection; push-pull; TTL with hysteresis; 5 V tolerant **0 —** all the four ports are active **1 —** only port 1 and port 2 are active; port 3 and port 4 are inactive
V_{DD}	10	-	supply voltage (3.3 V)
A20OUT	11	O	legacy gate 20 output; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
KBIRQ1	12	I	legacy keyboard interrupt input; push-pull; TTL with hysteresis; 5 V tolerant[3]
MUIRQ12	13	I	legacy mouse interrupt input; push-pull; TTL with hysteresis; 5 V tolerant[3]
DGND	14	-	digital ground
SMI#	15	O	System Management Interrupt; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
INTA#	16	O	PCI interrupt; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
V_{DD}	17	-	supply voltage (3.3 V)
RST#	18	I	PCI reset; used to bring PCI-specific registers, sequencers and signals to a consistent state; push-pull; TTL with hysteresis; 5 V tolerant
CLK	19	I	PCI system clock (33 MHz)
GNT#	20	I	PCI grant; indicates to the agent that access to the bus has been granted
DGND	21	-	digital ground

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
REQ#	22	O	PCI request; indicates to the arbitrator that the agent wants to use the bus
AD[31]	23	I/O	bit 31 of multiplexed PCI address and data
AD[30]	24	I/O	bit 30 of multiplexed PCI address and data
V_{DD}	25	-	supply voltage (3.3 V)
AD[29]	26	I/O	bit 29 of multiplexed PCI address and data
AD[28]	27	I/O	bit 28 of multiplexed PCI address and data
AD[27]	28	I/O	bit 27 of multiplexed PCI address and data
DGND	29	-	digital ground
AD[26]	30	I/O	bit 26 of multiplexed PCI address and data
AD[25]	31	I/O	bit 25 of multiplexed PCI address and data
AD[24]	32	I/O	bit 24 of multiplexed PCI address and data
V_{DD}	33	-	supply voltage (3.3 V)
C/BE#[3]	34	I/O	byte 3 of multiplexed PCI bus command and byte enable
IDSEL	35	I	PCI initialization device select; used as a chip select during configuration read and write transactions
AD[23]	36	I/O	bit 23 of multiplexed PCI address and data
DGND	37	-	digital ground
AD[22]	38	I/O	bit 22 of multiplexed PCI address and data
AD[21]	39	I/O	bit 21 of multiplexed PCI address and data
AD[20]	40	I/O	bit 20 of multiplexed PCI address and data
V_{DD}	41	-	supply voltage (3.3 V)
AD[19]	42	I/O	bit 19 of multiplexed PCI address and data
AD[18]	43	I/O	bit 18 of multiplexed PCI address and data
AD[17]	44	I/O	bit 17 of multiplexed PCI address and data
DGND	45	-	digital ground
AD[16]	46	I/O	bit 16 of multiplexed PCI address and data
C/BE#[2]	47	I/O	byte 2 of multiplexed PCI bus command and byte enable
FRAME#	48	I/O	PCI cycle frame; driven by the master to indicate the beginning and duration of an access
V_{DD}	49	-	supply voltage (3.3 V)
IRDY#	50	I/O	PCI initiator ready; indicates ability of the initiating agent to complete the current data phase of a transaction
TRDY#	51	I/O	PCI target ready; indicates ability of the target agent to complete the current data phase of a transaction
DEVSEL#	52	I/O	PCI device select; indicates if any device has been selected on the bus
DGND	53	-	digital ground
STOP#	54	I/O	PCI stop; indicates that the current target is requesting the master to stop the current transaction
CLKRUN#	55	I/O	PCI CLKRUN signal; push-pull input; three-state output; 5 ns slew rate control; TTL with hysteresis; 5 V tolerant

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
PERR#	56	I/O	PCI parity error; used to report data parity errors during all PCI transactions except a Special Cycle
V_{DD}	57	-	supply voltage (3.3 V)
SERR#	58	O	PCI system error; used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic; push-pull, open-drain; 10 ns slew rate control; CMOS; 5 V tolerant
PAR	59	I/O	PCI parity
C/BE#[1]	60	I/O	byte 1 of multiplexed PCI bus command and byte enable
DGND	61	-	digital ground
AD[15]	62	I/O	bit 15 of multiplexed PCI address and data
AD[14]	63	I/O	bit 14 of multiplexed PCI address and data
AD[13]	64	I/O	bit 13 of multiplexed PCI address and data
V_{DD}	65	-	supply voltage (3.3 V)
AD[12]	66	I/O	bit 12 of multiplexed PCI address and data
AD[11]	67	I/O	bit 11 of multiplexed PCI address and data
AD[10]	68	I/O	bit 10 of multiplexed PCI address and data
DGND	69	-	digital ground
AD[9]	70	I/O	bit 9 of multiplexed PCI address and data
AD[8]	71	I/O	bit 8 of multiplexed PCI address and data
C/BE#[0]	72	I/O	byte 0 of multiplexed PCI bus command and byte enable
V_{DD}	73	-	supply voltage (3.3 V)
AD[7]	74	I/O	bit 7 of multiplexed PCI address and data
AD[6]	75	I/O	bit 6 of multiplexed PCI address and data
DGND	76	-	digital ground
AD[5]	77	I/O	bit 5 of multiplexed PCI address and data
AD[4]	78	I/O	bit 4 of multiplexed PCI address and data
AD[3]	79	I/O	bit 3 of multiplexed PCI address and data
V_{DD}	80	-	supply voltage (3.3 V)
AD[2]	81	I/O	bit 2 of multiplexed PCI address and data
AD[1]	82	I/O	bit 1 of multiplexed PCI address and data
DGND	83	-	digital ground
AD[0]	84	I/O	bit 0 of multiplexed PCI address and data
V_{AUX}	85	-	auxiliary voltage (3.3 V)
DGND	86	-	digital ground
XTAL1	87	I	crystal oscillator input; this can also be a 12 or 48 MHz clock input
XTAL2	88	O	crystal oscillator output (12 MHz)
$\overline{OC1}$	89	I	overcurrent sense input for the USB downstream port 1 (digital); push-pull; TTL with hysteresis; 5 V tolerant

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
$\overline{PWE1}$	90	I/O	power enable for the USB downstream port 1 (open-drain). Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
GL1	91	I/O	GoodLink LED indicator output for the USB downstream port 1 (open-drain); the LED is OFF by default, blinks ON upon USB traffic; bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AMB1	92	I/O	amber LED indicator output for the USB downstream port 1 (open-drain); the LED is OFF by default; the LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AV_{AUX}	93	-	analog auxiliary voltage (3.3 V); supply voltage
GND_RREF	94	-	reference ground; RREF resistor must be connected to this pin
GRN1	95	I/O	green LED indicator output for the USB downstream port 1 (open-drain); the LED is OFF by default.The LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
$\overline{OC2}$	96	I	overcurrent sense input for the USB downstream port 2 (digital). Push-pull; TTL with hysteresis; 5 V tolerant
$\overline{PWE2}$	97	I/O	power enable for the USB downstream port 2 (open-drain). Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
GL2	98	I/O	GoodLink LED indicator output for the USB downstream port 2 (open-drain); the LED is OFF by default, blinks ON upon USB traffic. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AMB2	99	I/O	amber LED indicator output for the USB downstream port 2 (open-drain); the LED is OFF by default; The LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
GRN2	100	I/O	green LED indicator output for the USB downstream port 2 (open-drain); the LED is OFF by default; The LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AV_{AUX_PLL}	101	-	analog auxiliary voltage (3.3 V); supply voltage for PLL
DM1	102	AI/O	D–; analog connection for the USB downstream port 1
DP1	103	AI/O	D+; analog connection for the USB downstream port 1
AGND	104	-	analog ground
$\overline{OC3}$	105	I	overcurrent sense input for the USB downstream port 3 (digital). Push-pull; TTL with hysteresis; 5 V tolerant

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
$\overline{PWE3}$	106	I/O	power enable for the USB downstream port 3 (open-drain). Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
RREF	107	AI/O	analog connection for the external resistor (12 kΩ ± 1%)
AV_{AUX}	108	-	analog auxiliary voltage (3.3 V); supply voltage
DM2	109	AI/O	D–; analog connection for the USB downstream port 2
DP2	110	AI/O	D+; analog connection for the USB downstream port 2
AGND	111	-	analog ground
GL3	112	I/O	GoodLink LED indicator output for the USB downstream port 3 (open-drain). The LED is OFF by default, blinks ON upon USB traffic. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AMB3	113	I/O	amber LED indicator output for the USB downstream port 3 (open-drain). The LED is OFF by default; the LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
GRN3	114	I/O	green LED indicator output for the USB downstream port 3 (open-drain); the LED is OFF by default; the LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AV_{AUX}	115	-	analog auxiliary voltage (3.3 V); supply voltage
DM3	116	AI/O	D–; analog connection for the USB downstream port 3
DP3	117	AI/O	D+; analog connection for the USB downstream port 3
AGND	118	-	analog ground
$\overline{OC4}$	119	I	overcurrent sense input for the USB downstream port 4 (digital) push-pull; TTL with hysteresis; 5 V tolerant
$\overline{PWE4}$	120	I/O	power enable for the USB downstream port 4 (open-drain). Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
AV_{AUX}	121	-	analog auxiliary voltage (3.3 V); supply voltage
DM4	122	AI/O	D–; analog connection for the USB downstream port 4
DP4	123	AI/O	D+; analog connection for the USB downstream port 4
AGND	124	-	analog ground
GL4	125	I/O	GoodLink LED indicator output for the USB downstream port 4 (open-drain). The LED is OFF by default, blinks ON upon USB traffic. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant

Table 2: Pin description *…continued*

Symbol[1]	Pin	Type	Description
AMB4	126	I/O	amber LED indicator output for the USB downstream port 4 (open-drain); this pin acts as an input only during the power-up sequence and thereafter, acts as an output. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant **1 —** FF in PMC register; supports $D3_{cold}$ **0 —** EF in PMC register; does not support $D3_{cold}$
GRN4	127	I/O	green LED indicator output for the USB downstream port 4 (open-drain) The LED is OFF by default; the LED can be programmed to enable it to blink. Bi-directional pin; push-pull input; three-state output; 10 ns slew rate control; TTL; 5 V tolerant
DGND	128	-	digital ground

[1] Symbol names ending with a '#' (for example, NAME#) represent active LOW signals for PCI pins. Symbol names with an overscore (for example, $\overline{\text{NAME}}$) represent active LOW signals for USB pins.

[2] The pull-up resistor should be always present even if I^2C EEPROM is not used.

[3] If legacy support is not used, connect this pin to ground.

7. Functional description

7.1 OHCI Host Controller

An OHCI Host Controller transfers data to devices at the Original USB defined bit rate of 12 Mbit/s or 1.5 Mbit/s.

7.2 EHCI Host Controller

The EHCI Host Controller transfers data to a Hi-Speed USB compliant device at the Hi-Speed USB defined bit rate of 480 Mbit/s. When the EHCI Host Controller has the ownership of a port, the OHCI Host Controllers are not allowed to modify the port register. All additional port bit definitions required for the Enhanced Host Controller are not visible to the OHCI Host Controller.

7.3 Dynamic port-routing logic

The port-routing feature allows sharing of the same physical downstream ports between the Original USB Host Controller and the Hi-Speed USB Host Controller. This requirement of the *Enhanced Host Controller Interface Specification* provides four downstream ports, and these ports are multiplexed with the ports of the two OHCIs. The first and the third downstream ports are always connected to the first OHCI, and the second and the fourth downstream ports are always connected to the second OHCI.

The EHCI is responsible for the port-routing switching mechanism. Two register bits are used for ownership switching. During power-on and system reset, the default ownership of all downstream ports is the OHCIs. The Enhanced Host Controller driver controls the ownership during normal functionality.

7.4 Hi-Speed USB analog transceivers

The Hi-Speed USB analog transceivers interface directly to the USB cables via integrated termination resistors. These transceivers can transmit and receive serial data at all data rates: high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).

7.5 LED indicators for downstream ports

Indication of a good USB connection is provided through the GoodLink technology (open-drain, a maximum current of 20 mA). During enumeration, LED indicators blink ON momentarily corresponding to the enumeration traffic of the ISP1561 downstream ports. The LED also blinks ON whenever there is valid traffic to the downstream port. In the suspend mode, the LED is OFF.

The GoodLink feature provides a user-friendly indication on the status of the USB traffic between the host and downstream hubs and devices. It is a useful diagnostics tool to isolate faulty equipment and helps to reduce field support and hotline costs.

The system designer can also program two optional port indicators— a green LED and an amber LED—to indicate the status of the Host Controller. These port indicators are implemented as per the USB specification.

All LED indicators are open-drain output.

7.6 Power management

The ISP1561 provides an advanced power management capabilities interface that is compliant with *PCI Bus Power Management Interface Specification, Rev. 1.1*. Power is controlled and managed by the interaction between drivers and PCI registers. See Section 10 for a detailed description on power management.

7.7 Legacy support

The ISP1561 provides legacy support for a USB keyboard and mouse. This means that the keyboard and mouse should be able to work even before the OS boot-up, with the necessary support in the system's BIOS. Section 11.2 provides detailed description on legacy support in the ISP1561.

7.8 Phase-Locked Loop (PLL)

A 12 to 30 MHz and 48 MHz clock multiplier PLL is integrated on-chip. This allows the use of a low-cost 12 MHz crystal, which also minimizes EMI. No external components are required for the PLL to operate.

8. PCI

8.1 PCI interface

The PCI interface has three functions. The first function (#0) and the second function (#1) are for the OHCI Host Controllers, and the third function (#2) is for the EHCI Host Controller. All functions supports both master and target accesses and share the same PCI interrupt signal INTA#. These functions provide memory-mapped, addressable operational registers as required in *Open Host Controller Interface Specifications Rev. 1.0a* and *Enhanced Host Controller Specification for Universal Serial Bus Rev. 0.95*.

Additionally, function #0 provides legacy keyboard and mouse support to comply with *Open Host Controller Interface Specification Rev. 1.0a*.

Each function has its own configuration space, and the PCI enumerator should allocate the memory address space for each of these functions. Power management is implemented in each PCI function and all power states are provided. This allows the system to achieve low power consumption by switching off the functions which are not required.

8.1.1 PCI configuration space

PCI Local Bus Specification Rev. 2.2 requires that each of the three PCI functions of the ISP1561 provides its own PCI configuration registers, which can vary in size. In addition to the basic PCI configuration header registers, these functions implement the capability registers to support power management.

The registers of each of these functions are accessed by the respective driver. The detailed description of the various PCI configuration registers is given in Section 8.2.

8.1.2 PCI Initiator/Target

A PCI initiator initiates PCI transactions to the PCI bus; a PCI target responds to PCI transactions as a slave. In the case of the ISP1561, the two Open Host Controllers and the Enhanced Host Controller function as both initiators or the targets of PCI transactions issued by the host CPU.

All USB Host Controllers have their own operational registers, which can be accessed by the system driver software. Drivers use these registers to configure the Host Controller hardware system, issue commands to it and/or monitor the status of the current hardware operation. The Host Controller plays the role of a PCI target. All operational registers of the Host Controllers are PCI transaction targets of the CPU.

Normal USB transfers require the Host Controller to access system memory fields, which are allocated by USB Host Controller Drivers (HCDs) and PCI drivers. The Host Controller hardware interacts with the HCD by accessing these buffers. The Host Controller works as an initiator in this case, and becomes a PCI master.

8.2 PCI configuration registers

The OHCI USB Host Controllers and EHCI USB Host Controller contain two sets of software-accessible hardware registers: PCI configuration registers and memory-mapped Host Controller registers.

A set of the configuration registers are implemented for each of the three PCI functions of the ISP1561, see Table 3.

Remark: In addition to the normal PCI header (from offset index 00H to 3FH), implementation-specific registers are defined to support power management and function-specific features.

Table 3: PCI configuration space registers of OHCI1, OHCI2 and EHCI[1]

Address (Hex)	Bits 31 to 22	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0	Reset Hex Value		
					Func0 OHCI1	Func1 OHCI2	Func2 EHCI
00	DID[15:0]		VID[15:0]		1561 1131	1561 1131	1562 1131
04	Status[15:0]		Command[15:0]		0210 **0000**	0210 **0000**	0210 **0000**
08	Class Code[23:0]			REVID[7:0]	0C0310 30	0C0310 30	0C0320 30
0C	BIST[7:0]	Header Type[7:0]	LT[7:0]	CLS[7:0]	00 80 **00 00**	00 80 **00 00**	00 80 **00 00**
10	BAR 0[31:0]				**00000**000	**00000**000	**000000**00
14	Base Address Register 1, 2, 3, 4, 5 (Not configurable to prevent setting by the driver)				00000000	00000000	00000000
18							
1C							
20							
24							
28	Cardbus CIS Pointer[31:0]				00000000	00000000	00000000
2C	SID[15:0]		SVID[15:0]		1561 1131	1561 1131	1562 1131
30	Expansion ROM Base Address[31:0]				00000000	00000000	00000000
34	Reserved			CP[7:0]	000000 DC	000000 DC	000000 DC
38	Reserved				00000000	00000000	00000000

Table 3: PCI configuration space registers of OHCI1, OHCI2 and EHCI[1] *…continued*

Address (Hex)	Bits 31 to 22	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0	Reset Hex Value		
					Func0 OHCI1	Func1 OHCI2	Func2 EHCI
3C	Max_Lat[7:0]	Min_Gnt[7:0]	Interrupt Pin[7:0]	IL[7:0]	**2A 01 01 00**	**2A 01 01 00**	**10 02 01 00**
40	Reserved		Retry Time-out	TRDY Time-out	0000 **80 00**	0000 **80 00**	0000 **80 00**
Enhanced Host Controller-specific PCI registers							
60	PORTWAKECAP[15:0]		FLADJ[7:0]	SBRN[7:0]	-	-	**XX1F 20** 20[2]
Power management registers							
DC	PMC[15:0]		Next_Item_Ptr [7:0]	Cap_ID[7:0]	5202 00 01	5202 00 01	FF02 00 01
E0	DATA[7:0]	PMCSR_BSE [7:0]	PMCSR[15:0]		00 00 **0000**	00 00 **0000**	00 00 **XX00**[2]

[1] Reset hex values that are highlighted (for example, **0**) indicate read/write access, and reset hex values that are not highlighted (for example, 0) indicate read-only.

[2] XX is 1FH for four ports or 07H for two ports.

The Host Controller Driver (HCD) does not usually interact with the PCI configuration space. The configuration space is used only by the PCI enumerator to identify the USB Host Controller and assign the appropriate system resources by reading the Vendor ID (VID) and the Device ID (DID).

8.2.1 PCI configuration header registers

The Enhanced Host Controller implements the normal PCI header register values, except the values for the memory-mapping base address register, serial bus number and Device ID.

Vendor ID register (address: 00H): This read-only register identifies the manufacturer of the device. PCI Special Interest Group (PCI-SIG) assigns valid vendor identifiers to ensure the uniqueness of the identifier. The bit description is shown in Table 4.

Table 4: Vendor ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	VID[15:0]	R	1131H	**Vendor ID**: This read-only register value is assigned to Philips Semiconductors by PCI-SIG as 1131H.

Device ID register (address: 02H): Device ID is a two-byte read-only register that identifies a particular device. This identifier is allocated by Philips Semiconductors. Table 5 shows the bit description of the register.

Table 5: Device ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	DID[15:0]	R	156XH[1]	**Device ID**: This register value is defined by Philips Semiconductors to identify the USB Host Controller IC product.

[1] X is 1H for OHCI1 and OHCI2 and X is 2H for EHCI.

Command register (address: 04H): This is a two-byte register that provides coarse control over the ability of a device to generate and respond to PCI cycles. The bit allocation of the Command register is given in Table 6. When logic 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not support this base level of functionality.

Table 6: Command register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved						FBBE	SERRE
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SCTRL	PER	VGAPS	MWIE	SC	BM	MS	IOS
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R	R/W	R	R/W	R/W	R/W

Table 7: Command register: bit description

Bit	Symbol	Description
15 to 10	-	reserved
9	FBBE	**Fast Back-to-Back Enable:** This bit controls whether or not a master can do fast back-to-back transactions to different devices. The initialization software needs to set this bit if all targets are fast back-to-back capable. **0 —** fast back-to-back transactions are only allowed to the same agent (value after RST#) **1 —** the master is allowed to generate fast back-to-back transactions to different agents
8	SERRE	**SERR# Enable**: This bit is an enable bit for the SERR# driver. All devices that have an SERR# pin must implement this bit. Address parity errors are reported only if this bit and the PER bit are logic 1. **0 —** disable the SERR# driver **1 —** enable the SERR# driver
7	SCTRL	**Stepping Control**: This bit is used to control whether or not a device does address and data stepping. Devices that never do stepping must clear this bit. Devices that always do stepping must set this bit. Devices that can do either, must make this bit read/write and have it initialize to logic 1 after RST#.
6	PER	**Parity Error Response**: This bit controls the response of a device to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is logic 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation. The state of this bit after RST# is logic 0. Devices that check parity must implement this bit. Devices are required to generate parity even if parity checking is disabled.

Table 7: Command register: bit description *...continued*

Bit	Symbol	Description
5	VGAPS	**VGA Palette Snoop**: This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. When this bit is logic 1, palette snooping is enabled (that is, the device does not respond to palette register writes and snoops the data). When the bit is logic 0, the device should treat palette write accesses like all other accesses. VGA compatible devices should implement this bit.
4	MWIE	**Memory Write and Invalidate Enable**: This is an enable bit for using the Memory Write and Invalidate command. When this bit is logic 1, masters may generate the command. When it is logic 0, Memory Writes must be used instead. State after RST# is logic 0. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
3	SC	**Special Cycles**: Controls the action of a device on Special Cycle operations. A value of logic 0 causes the device to ignore all Special Cycle operations. A value of logic 1 allows the device to monitor Special Cycle operations. State after RST# is logic 0.
2	BM	**Bus Master**: Controls the ability of a device to act as a master on the PCI bus. A value of logic 0 disables the device from generating PCI accesses. A value of logic 1 allows the device to behave as a bus master. State after RST# is logic 0.
1	MS	**Memory Space**: Controls the response of a device to Memory Space accesses. A value of logic 0 disables the device response. A value of logic 1 allows the device to respond to Memory Space accesses. State after RST# is logic 0.
0	IOS	**IO Space**: Controls the response of a device to I/O Space accesses. A value of logic 0 disables the device response. A value of logic 1 allows the device to respond to I/O Space accesses. State after RST# is logic 0.

Status register (address: 06H): The Status register is a two-byte read-only register used to record status information on PCI bus-related events (bit allocation: see Table 8).

Table 8: Status register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	DPE	SSE	RMA	RTA	STA	DEVSELT[1:0]		MDPE
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FBBC	reserved	66MC	CL	reserved			
Reset	0	0	0	1	0	0	0	0
Access	R	-	R	R	-	-	-	-

Table 9: Status register: bit description

Bit	Symbol	Description
15	DPE	**Detected Parity Error**: This bit must be set by the device whenever it detects a parity error, even if the parity error handling is disabled.
14	SSE	**Signaled System Error**: This bit must be set whenever the device asserts SERR#. Devices that never assert SERR# do not need to implement this bit.
13	RMA	**Received Master Abort**: This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
12	RTA	**Received Target Abort**: This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
11	STA	**Signaled Target Abort**: This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that never signal Target-Abort do not need to implement this bit.
10 to 9	DEVSELT[1:0]	**DEVSEL Timing**: These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL#: **00B —** for fast **01B —** for medium **10B —** for slow **11B —** is reserved These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.
8	MDPE	**Master Data Parity Error:** This bit is implemented by bus masters. It is set when the following three conditions are met: • The bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write). • The agent setting the bit acted as the bus master for the operation in which error occurred. • The Parity Error Response bit (in the Command register) is set.
7	FBBC	**Fast Back-to-Back Capable**: This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to logic 1 if the device can accept these transactions and must be set to logic 0 otherwise.
6	-	reserved

Table 9: Status register: bit description…*continued*

Bit	Symbol	Description
5	66MC	**66 MHz Capable**: This read-only bit indicates whether or not this device is capable of running at 66 MHz. A value of logic 0 indicates 33 MHz, and a value of logic 1 indicates 66 MHz.
4	CL	**Capabilities List**: This read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34H. A value of logic 0 indicates that no New Capabilities linked list is available. A value of logic 1 indicates that the value read at offset 34H is a pointer in Configuration Space to a linked list of new capabilities.
3 to 0	-	reserved

Revision ID register (address: 08H): This one-byte read-only register indicates a device specific revision identifier. The value is chosen by the vendor. This field is a vendor defined extension of the Device ID. The Revision ID register bit description is given in Table 10.

Table 10: Revision ID register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	REVID[7:0]	R	30H	**Revision ID**: This byte specifies the design revision number of functions.

Class Code register (address: 09H): Class Code is a 24-bit read-only register used to identify the generic function of the device, and in some cases, a specific register-level programming interface. Table 11 shows the bit allocation of the register.

The Class Code register is divided into three byte-size fields. The upper byte is a base class code that broadly classifies the type of function the device performs. The middle byte is a sub-class code that identifies more specifically the function of the device. The lower byte identifies a specific register-level programming interface, if any, so that device independent software can interact with the device.

Table 11: Class Code register: bit allocation

Bit	23	22	21	20	19	18	17	16
Symbol	BCC[7:0]							
Reset	0CH							
Access	R							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	SCC[7:0]							
Reset	03H							
Access	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RLPI[7:0]							
Reset	X0H[1]							
Access	R							

[1] X is 1H for OHCI1 and OHCI2; X is 2H for EHCI.

Table 12: Class Code register: bit description

Bit	Symbol	Description
23 to 16	BCC[7:0]	**Base Class Code**: 0CH is the base class code assigned to this byte, and it implies a serial bus controller.
15 to 8	SCC[7:0]	**Sub-Class Code**: 03H is the sub-class code assigned to this byte, and it implies the USB Host Controller.
7 to 0	RLPI[7:0]	**Register-Level Programming Interface**: 10H is the programming interface code assigned to OHCI, which is USB 1.1 specification compliant. 20H is the programming interface code assigned to EHCI, which is USB 2.0 specification compliant.

CacheLine Size register (address: 0CH): The CacheLine Size register is a read/write single byte register that specifies the system cacheline size in units of DWords. This register must be implemented by master devices that can generate the Memory Write and Invalidate command. The value in this register is also used by master devices to determine whether to use Read, Read Line, or Read Multiple commands for accessing memory.

Slave devices that want to allow memory bursting using a cacheline-wrap addressing mode must implement this register to know when a burst sequence wraps to the beginning of the cacheline.

This field must be initialized to logic 0 on activation of RST#. Table 13 shows the bit description of the CacheLine Size register.

Table 13: CacheLine Size register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	CLS[7:0]	R/W	00H	**CacheLine Size**: This byte identifies the system cacheline size.

Latency Timer register (address: 0DH): This one-byte register specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master. The Latency Time register bit description is given in Table 14.

This register must be implemented as writable by any master that can burst more than two data phases. This register may be implemented as read-only for devices that burst two or fewer data phases, but the fixed value must be limited to 16 or less. The register must be initialized to logic 0 at RST#, if programmable.

Table 14: Latency Timer register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	LT[7:0]	R/W	00H	**Latency Timer**: This byte identifies the latency timer.

Header Type register (address: 0EH): The Header Type register identifies the layout of the second part of the predefined header (beginning at byte 10H in Configuration Space). It also identifies whether or not the device contains multiple functions (bit allocation: see Table 15).

Table 15: Header Type register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MFD	HT[6:0]						
Reset	1	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 16: Header Type register: bit description

Bit	Symbol	Description
7	MFD	**Multi-Function Device**: This bit identifies a multi-function device. If the bit is logic 0, then the device is a single function. If the bit is logic 1, then the device has multiple functions.
6 to 0	HT[6:0]	**Header Type**: These bits identify the layout of the part of the predefined header beginning at byte 10H in Configuration Space.

BIST register (address: 0FH): This register is used for control and status of Built in Self Test (BIST). Devices that do not support BIST must always return a value of logic 0 (that is, treat it as a reserved register). A device whose BIST is invoked must not prevent normal operation of the PCI bus. The BIST register is not used in the ISP1561. Therefore, the logic value returned is always zero.

Base Address registers: Power-up software needs to build a consistent address map before booting the machine to an operating system. This means it has to determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, power-up software can map the I/O controllers into reasonable locations and proceed with system boot. To do this mapping in a device independent manner, the base registers for this mapping are placed in the predefined header portion of Configuration Space.

The bit 0 in all Base Address registers is read-only and used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return logic 0 in bit 0. Base Address registers that map to I/O Space must return logic 1 in bit 0.

The bit description of the BAR 0 register is given in Table 17.

Base Address register 0 (BAR 0) — (address: 10H)

Table 17: BAR 0 register: bit description

Bit	Symbol	Access	Value	Description
31 to 0	BAR 0[31:0]	R/W	0000 0000H	**Base Address to Memory-Mapped Host Controller Register Space**: The memory size required by OHCI and EHCI are 4 K and 256 bytes, respectively. Therefore, BAR 0[31:12] is assigned to the two OHCI ports, and BAR 0[31:8] is assigned to the EHCI port.

Base Address register 1, 2, 3, 4, 5 (BAR 1, 2, 3, 4, 5) — (address: 14H, 18H, 1CH, 20H and 24H): The BAR 1, 2, 3, 4, 5 register spaces are not used in the ISP1561.

CardBus CIS Pointer register (address: 28H): This four-byte register is used by devices that want to share silicon between CardBus and PCI. The CardBus CIS Pointer register is used to point to the Card Information Structure (CIS) for the CardBus card. This register is not implemented in the ISP1561.

Subsystem Vendor ID register (address: 2CH): The Subsystem Vendor ID register is used to uniquely identify the expansion board or subsystem where the PCI device resides. This register allows expansion board vendors to further distinguish their boards, even though the boards may have the same Vendor ID and Device ID.

Subsystem Vendor IDs are assigned by PCI-SIG to maintain uniqueness. The bit description of the Subsystem Vendor ID register is given in Table 18.

Table 18: Subsystem Vendor ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	SVID[15:0]	R	1131H	**Subsystem Vendor ID**: 1131H is the subsystem Vendor ID assigned to Philips Semiconductors.

Subsystem ID register (address: 2EH): Subsystem ID values are vendor specific. The bit description of the Subsystem ID register is given in Table 19.

Table 19: Subsystem ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	SID[15:0]	R	156XH[1]	**Subsystem ID**: For the ISP1561, Philips Semiconductors has defined OHCI functions as 1561H, and the EHCI function as 1562H.

[1] X is 1H for OHCI1 and OHCI2; X is 2H for EHCI.

Expansion ROM Base Address register (address: 30H): Some PCI devices, especially those intended for use on expansion boards in the PC architecture, require local EPROMs for expansion ROM. This four-byte register at offset 30H in a type 00H predefined header is defined to handle the base address and size information for this expansion ROM. The ISP1561 does not support expansion EPROM.

Capabilities Pointer register (address: 34H): The Capabilities Pointer register is used to point to a linked list of new capabilities implemented by the device. This register is only valid if the CL bit in the Status register is set. If implemented, bit 1 and bit 0 are reserved and should be set to 00B. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities. The bit description of the register is given in Table 20.

Table 20: Capabilities Pointer register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	CP[7:0]	R	DCH	**Capabilities Pointer**: EHCI manages power efficiently using this register. This Power Management register is allocated at offset DCH. Only one Host Controller is needed to manage power in the ISP1561.

Interrupt Line register (address: 3CH): The Interrupt Line register is a one-byte read/write register used to communicate interrupt line routing information. This register must be implemented by any device (or device function) that uses an interrupt pin. The interrupt allocation is done by the BIOS. The POST software needs to write the routing information into this register as it initializes and configures the system. The bit description of the Interrupt Line register is given in Table 21.

The value in this register tells which input of the system interrupt controller(s) the interrupt pin of the device is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.

Table 21: Interrupt Line register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	IL[7:0]	R/W	00H	**Interrupt Line**: Indicates which IRQ is used for reporting interrupt from the ISP1561.

Interrupt Pin register (address: 3DH): This one-byte register is use to specify which interrupt pin the device (or device function) uses. The bit description is given in Table 22.

A value of 1H corresponds to INTA#. A value of 2H corresponds to INTB#. A value of 3H corresponds to INTC#. A value of 4H corresponds to INTD#. Devices or functions that do not use an interrupt pin must put a logic 0 in this register.

Table 22: Interrupt Pin register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	IP[7:0]	R/W	01H	**Interrupt Pin**: INTA# is the default interrupt pin used by the ISP1561.

Minimum Grant and Maximum Latency registers (address: 3EH and 3FH): The Min_Gnt and Max_Lat registers are used to specify the desired settings of the device for Latency Timer values. For both registers, the value specifies a period of time in units of 250 ns. Values of 0 indicates that the device has no major requirements for the settings of Latency Timers.The Min_Gnt register bit description is given in Table 23.

Table 23: Min_Gnt register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	Min_Gnt[7:0]	R/W	0XH[1]	**Min_Gnt**: It is used to specify how long a burst period the device needs assuming a clock rate of 33 MHz.

[1] X is 1H for OHCI1 and OHCI2; X is 2H for EHCI.

The Max_Lat register bit description is given in Table 24.

Table 24: Max_Lat register: but description

Bit	Symbol	Access	Value	Description
7 to 0	Max_Lat[7:0]	R/W	XXH[1]	**Max_Lat**: It is used to specify how often the device needs to gain access to the PCI bus.

[1] XX is 2AH for OHCI1 and OHCI2; XX is 10H for EHCI.

8.2.2 Enhanced Host Controller-specific PCI registers

In addition to the PCI configuration header registers, EHCI needs some additional PCI configuration space registers to indicate the serial bus release number, downstream port wake-up event capability and adjust the USB bus frame length for Start-of-Frame (SOF). The EHCI-specific PCI registers are given in Table 25.

Table 25: EHCI-specific PCI registers

Offset	Register
60H	Serial Bus Release Number (SBRN)
61H	Frame Length Adjustment (FLADJ)
62-63H	Port Wake Capability (PORTWAKECAP)

SBRN register (address: 60H): The SBRN register is a one-byte register, and the bit description is given in Table 26. This register contains the release number of the USB specification with which this USB Host Controller module is complaint.

Table 26: SBRN register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	SBRN[7:0]	R	20H	**Serial Bus Specification Release Numbe**r: This register value is to identify Serial Bus Specification Release 2.0. All other combinations are reserved.

FLADJ register (address: 61H): This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written to these six bits, the length of the frame is adjusted. The bit allocation of the register is given in Table 27.

Table 27: FLADJ register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		FLADJ[5:0]					
Reset	0	0	1	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Table 28: FLADJ register: bit description

Bit	Symbol	Description
7 to 6	-	reserved
5 to 0	FLADJ[5:0]	**Frame Length Timing Value**: Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32 (20H), which gives a SOF cycle time of 60000.

FLADJ Value	SOF cycle time (480 MHz)
0 (00H)	59488
1 (01H)	59504
2 (02H)	59520
:	:
31(1FH)	59984
32 (20H)	60000
:	:
62 (3EH)	60480
63 (3FH)	60496

PORTWAKECAP register (address: 62H): The PORTWAKECAP register is a two-byte register, and the bit description is given in Table 29. This register is used to establish a policy about which ports are to be used for wake events. Bit positions 1 to 15 in the mask correspond to a physical port implemented on the current EHCI controller. A logic 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or overcurrent events as wake-up events. This is an information only mask register. The bits in this register do not affect the actual operation of the

EHCI Host Controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. System software uses the information in this register when enabling devices and ports for remote wake-up.

Table 29: PORTWAKECAP register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	PORTWAKECAP[15:0]	R/W	001FH	**Port Wake Up Capability Mask**: EHCI does not implement this feature.

8.2.3 Power management registers

Table 30: Power Management registers

Offset	Register
value read from address 34H + 0H	Capability Identifier (Cap_ID)
value read from address 34H + 1H	Next Item Pointer (Next_Item_Ptr)
value read from address 34H + 2H	Power Management Capabilities (PMC)
value read from address 34H + 4H	Power Management Control/Status (PMCSR)
value read from address 34H + 6H	Power Management Control/Status (PMCSR_BSE)
value read from address 34H + 7H	Data

Cap_ID register (address: value read from address 34H + 0H): The Capability Identifier (Cap_ID) register, when read by the system software as 01H indicates that the data structure currently being pointed to is the PCI Power Management data structure. Each function of a PCI device may have only one item in its capability list with Cap_ID set to 01H. The bit description o the register is given in Table 31.

Table 31: Cap_ID register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	Cap_ID[7:0]	R	01H	**ID**: This field when 01H identifies the linked list item as being the PCI Power Management registers.

Next_Item_Ptr register (address: value read from address 34H + 1H): The Next Item Pointer (Next_Item_Ptr) register (see Table 32) describes the location of the next item in the function's capability list. The value given is an offset into the function's PCI Configuration Space. If the function does not implement any other capabilities defined by the PCI-SIG for inclusion in the capabilities list, or if power management is the last item in the list, then this register must be set to 00H.

Table 32: Next_Item_Ptr register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	Next_Item_Ptr[7:0]	R	00H	**Next Item Pointer**: This field provides an offset into the function's PCI Configuration Space pointing to the location of the next item in the function's capability list. If there are no additional items in the Capabilities List, this register is set to 00H.

PMC register (address: value read from address 34H + 2H): The Power Management Capabilities (PMC) register is a two-byte register, and the bit allocation is given in Table 33. This read-only register provides information on the capabilities of the function related to power management.

Table 33: PMC register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PME_S[4:0]					D2_S	D1_S	AUX_C[2:0]
Reset	X[1]	1	X[2]	1	X[2]	X[2]	1	X[2]
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AUX_C[2:0]		DSI	reserved	PMI	VER[2:0]		
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	-	R	R	R	R

[1] X is 0 for OHCI1, OHCI2 and EHCI S1; X is 1 for EHCI S3.

[2] X is 0 for OHCI1 and OHCI2; X is 1 for EHCI.

Table 34: PMC register: bit description

Bit	Symbol	Description
15 to 11	PME_S[4:0]	**PME_Support**: This 5-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. **PME_S[0] —** PME# can be asserted from D0 **PME_S[1] —** PME# can be asserted from D1 **PME_S[2] —** PME# can be asserted from D2 **PME_S[3] —** PME# can be asserted from $D3_{hot}$ **PME_S[4] —** PME# can be asserted from $D3_{cold}$
10	D2_S	**D2_Support**: If this bit is logic 1, this function supports the D2 Power Management State. Functions that do not support D2 must always return a value of logic 0 for this bit.
9	D1_S	**D1_Support**: If this bit is logic 1, this function supports the D1 Power Management State. Functions that do not support D1 must always return a value of logic 0 for this bit.

Table 34: PMC register: bit description *…continued*

Bit	Symbol	Description
8 to 6	AUX_C[2:0]	**Aux_Current**: This three-bit field reports the V_{AUX} auxiliary current requirements for the PCI function. If the Data register has been implemented by this function: • A read from this field needs to return a value of 000B. • The Data register takes precedence over this field for V_{AUX} current requirement reporting. If the PME# generation from $D3_{cold}$ is not supported by the function (PMC(15) = 0), this field must return a value of 000B when read. For functions that support PME# from $D3_{cold}$ and do not implement the Data register, the bit assignments correspond to the maximum current required for V_{AUX} are: **111 —** 375 mA **110 —** 320 mA **101 —** 270 mA **100 —** 220 mA **011 —** 160 mA **010 —** 100 mA **001 —** 55 mA **000 —** 0 (self powered)
5	DSI	**Device Specific Initialization**: This bit indicates whether special initialization of this function is required, beyond the standard PCI configuration header, before the generic class device driver is able to use it. **Remark:** This bit is not used by some operating systems. For example, Microsoft Windows and Windows NT® do not use this bit to determine whether to use D3. Instead, they use capabilities of the driver to determine this. Logic 1 indicates that the function requires a device specific initialization sequence following transition to D0 un-initialized state.
4	-	reserved
3	PMI	**PME Clock**: When this bit is logic 1, it indicates that the function relies on the presence of the PCI clock for the PME# operation. When this bit is logic 0, it indicates that no PCI clock is required for the function to generate PME#. Functions that do not support the PME# generation in any state must return logic 0 for this field.
2 to 0	VER[2:0]	**Version**: A value of 010B indicates that this function complies with *PCI Power Management Interface Specification Rev. 1.1*.

The logic level of the AMB4 pin at power-on determines the default value of the PMC registers. If this pin is connected to V_{DD} as a pull-up, then the ISP1561 supports $D3_{cold}$ (in the case of notebook design). If this pin is left open or is pulled down, then the ISP1561 does not support $D3_{cold}$ (in the case of PCI add-on card design).

PMCSR register (address: value read from address 34H + 4H): The Power Management Control/Status (PMCSR) register is a two-byte register used to manage the power management state of the PCI function as well as to enable and monitor Power Management Events (PMEs). The bit allocation of the register is given in Table 35.

Table 35: PMCSR register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PMES	DS[1:0]		D_S[3:0]				PMEE
Reset	X[1]	0	0	0	0	0	0	X[1]
Access	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						PS[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	R/W	R/W

[1] Sticky bit, if the function supports PME# from $D3_{cold}$ then X is indeterminate at the time of initial operating system boot; X is 0 if the function does not support PME# from $D3_{cold}$.

Table 36: PMCSR register: bit description

Bit	Symbol	Description
15	PMES	**PME Status**: This bit is set when the function would normally assert the PME# signal independent of the state of the PME_EN bit. Writing logic 1 to this bit clears it and causes the function to stop asserting PME# (if enabled). Writing logic 0 has no effect. This bit defaults to logic 0 if the function does not support the PME# generation from $D3_{cold}$. If the function supports the PME# generation from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
14 to 13	DS[1:0]	**Data Scale**: This two-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field vary depending on which data value has been selected by the D_S field. This field is a required component of the Data register (offset 7) and must be implemented if the Data register is implemented. If the Data register has not been implemented, this field must return 00B when PMCSR is read.
12 to 9	D_S[3:0]	**Data_Select**: This four-bit field is used to select which data is to be reported through the Data register and the D_S field. This field is a required component of the Data register (offset 7) and must be implemented if the Data register is implemented. If the Data register has not been implemented, this field must return 00B when PMCSR is read.

Table 36: PMCSR register: bit description…*continued*

Bit	Symbol	Description
8	PMEE	**PME Enabled**: Logic 1 enables the function to assert PME#. When it is logic 0, PME# assertion is disabled. This bit defaults to logic 0 if the function does not support the PME# generation from $D3_{cold}$. If the function supports PME# from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. Functions that do not support the PME# generation from any D-state (that is, PMC[15:11] = 00000B), may hardwire this bit to be read-only always returning logic 0 when read by system software.
7 to 2	-	reserved
1 to 0	PS[1:0]	**Power State**: This two-bit field is used to determine the current power state of the EHCI function and to set the function into a new power state. The definition of the field values is given as: **00B —** for D0 **01B —** for D1 **10B —** for D2 **11B —** for $D3_{hot}$ If the software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no status change occurs.

PMCSR_BSE register (address: value read from address 34H + 6H): The PMCSR PCI-to-PCI Bridge Support Extensions (PMCSR_BSE) register supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges. The bit allocation of this register is given in Table 37.

Table 37: PMCSR_BSE register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BPCC_En	B2_B3#	reserved					
Reset	R	R	R	R	R	R	R	R
Access	0[1]	0[1]	0	0	0	0	0	0

[1] Internally hardwired.

Table 38: PMCSR_BSE register: bit description

Bit	Symbol	Description
7	BPCC_En	**Bus Power/Clock Control Enable** **1 —** Indicates that the bus power/clock control mechanism as defined in Table 39 is enabled. **0 —** Indicates that the bus/power control policies as defined in Table 39 have been disabled. When the Bus Power/Clock Control mechanism is disabled, the bridge's PMCSR PS (Power State) field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
6	B2_B3#	**B2/B3 support for $D3_{hot}$**: The state of this bit determines the action that is to occur as a direct result of programming the function to $D3_{hot}$. **1 —** Indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus's PCI clock will be stopped (B2). **0 —** Indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus will have its power removed (B3). This bit is only meaningful if bit 7 (BPCC_En) is logic 1.
5 to 0	-	reserved

Table 39: PCI bus power and clock control

Originating device's bridge PM state	Secondary bus PM state	Resultant actions by bridge (either direct or indirect)
D0	B0	none
D1	B1	none
D2	B2	clock stopped on secondary bus
$D3_{hot}$	B2, B3	clock stopped and V_{CC} removed from secondary bus (B3 only). For definition of B2_B3#, see Table 38.
$D3_{cold}$	B3	none

Data register (address: value read from address 34H + 7H): The Data register is an optional, 1-byte register that provides a mechanism for the function to report state dependent operating data, such as power consumed or heat dissipation. Table 40 shows the bit description of the register.

Table 40: Data register: bit description

Bit	Symbol	Access	Value	Description
7 to 0	DATA[7:0]	R	00H	**DATA**: This register is used to report the state dependent data requested by the D_S (Data_Select) field. The value of this register is scaled by the value reported by the DS (Data_Scale) field.

9. I²C-bus interface

A simple I²C-bus interface is provided in the ISP1561 to read customized vendor ID, product ID and some other configuration bits from an external EEPROM.

The I²C-bus interface is intended for bidirectional communication between ICs via two serial bus wires, SDA (data) and SCL (clock). Both lines are driven by open-drain circuits and must be connected to the positive supply voltage via pull-up resistors.

9.1 Protocol

The I²C-bus protocol defines the following conditions:

- **Bus free**: both SDA and SCL are HIGH
- **START**: a HIGH-to-LOW transition on SDA, while SCL is HIGH
- **STOP**: a LOW-to-HIGH transition on SDA, while SCL is HIGH
- **Data valid**: after a START condition, data on SDA are stable during the HIGH period of SCL; data on SDA may only change while SCL is LOW.

Each device on the I²C-bus has a unique slave address, which the master uses to select a device for access.

The master starts a data transfer using a START condition and ends it by generating a STOP condition. Transfers can only be initiated when the bus is free. The receiver must acknowledge each byte by means of a LOW level on SDA during the ninth clock pulse on SCL.

For detailed information please consult *The I²C-bus and how to use it.*, order number 9398 393 40011.

9.2 Hardware connections

Via the I²C-bus interface the ISP1561 can be connected to an external EEPROM. The hardware connections are shown in Figure 3.

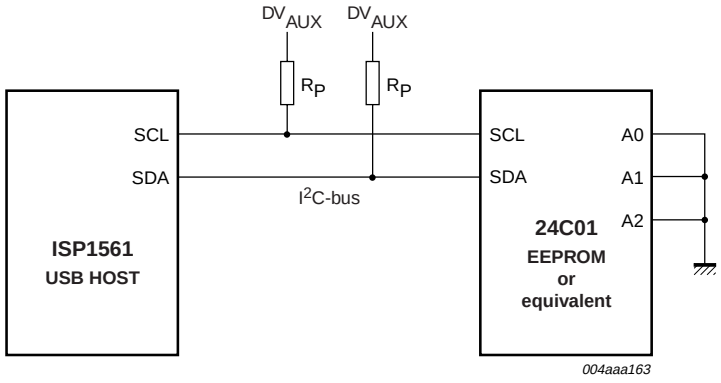
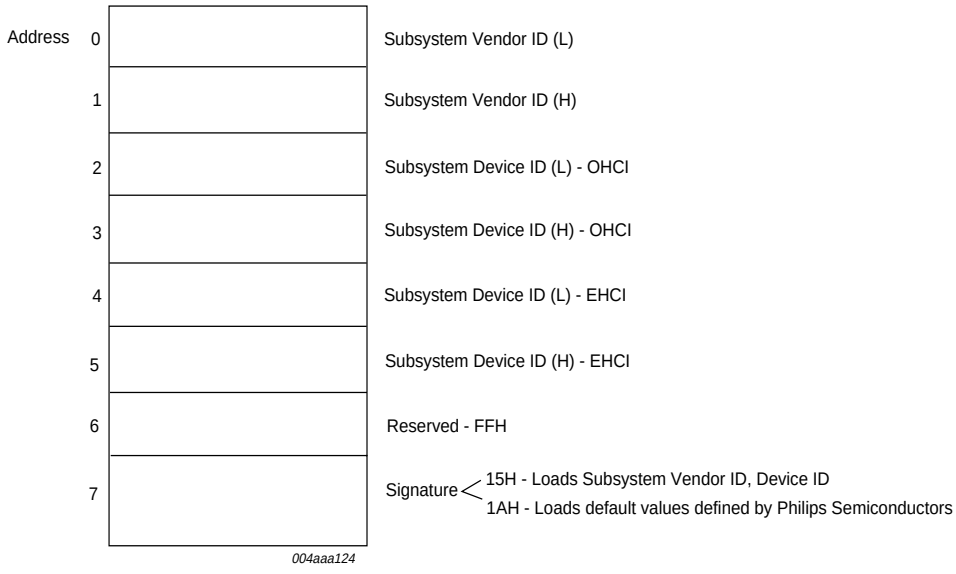


Fig 3. EEPROM connection diagram.

The slave address which ISP1561 uses to access the EEPROM is 1010000B. Page mode addressing is not supported, so pins A0, A1 and A2 of the EEPROM must be connected to ground (logic 0).

9.3 Information loading from EEPROM

Figure 4 shows the content of the EEPROM memory. If the EEPROM is not present, the default values of Device ID (DID), Vendor ID (VID), subsystem VID and subsystem DID assigned to Philips Semiconductors by PCI-SIG will be loaded. See Table 3 for these default value. For instructions on programming the EEPROM, refer to *Designing a USB 2.0 Host PCI Adapter Using the ISP1561 Application Note* and *ISP1561 Evaluation Board User's Guide*.



L = LOW; H = HIGH.

Fig 4. Information loading from EEPROM.

10. Power management

10.1 PCI bus power states

The PCI bus can be characterized by one of the four power management states– B0, B1, B2 and B3.

B0 state (PCI clock = 33 MHz, PCI bus power = ON) — This corresponds to the bus being fully operational.

B1 state (PCI clock = intermittent clock operation mode, PCI bus power = ON) — When a PCI bus is in B1, V_{DD} is still applied to all devices on the bus. However, no bus transactions are allowed to take place on the bus. The B1 state indicates a perpetual idle state on the PCI bus.

B2 state (PCI clock = Stop, PCI bus power = ON) — V_{DD} is still applied on the bus, but the clock is stopped and held in the LOW state.

B3 state (PCI clock = Stop, PCI bus power = OFF) — V_{DD} has been removed from all devices on the PCI bus segment.

10.2 USB bus states

Reset state — When the USB bus is in the reset state, the USB system is stopped.

Operational state — When the USB bus is in the active state, the USB system is operating normally.

Suspend state — When the USB bus is in the suspend state, the USB system is stopped.

Resume state — When the USB bus is in the resume state, the USB system is operating normally.

11. USB Host Controller registers

Each Host Controller contains a set of on-chip operational registers that are mapped into non-cache memory of system addressable space. This memory space must begin on a DWord (32-bit) boundary. The size of the allocated space is defined by the initial value in the BAR 0 register. Host Controller drivers need to interact with these registers to implement USB and legacy support functionality.

After the PCI enumeration driver finishes the PCI device configuration, the new base address of these memory-mapped operational registers is defined in BAR 0. The Host Controller Driver (HCD) can access these registers by using the address of base address value + offset. Table 41 contains a list of Host Controller registers.

Table 41: USB Host Controller registers

Address (Hex)	OHCI Register	Reset Hex Value[1]						EHCI Register
		Func0 OHCI1 (2P)	Func0 OHCI1 (1P)	Func1 OHCI2 (2P)	Func1 OHCI2 (1P)	Func2 EHCI (4P)	Func2 EHCI (2P)	
00	HcRevision	00000**110**	00000**110**	00000**010**	00000**010**	**0095000C**	**0095000C**	CAPLENGTH/ HCIVERSION
04	HcControl	00000000	00000000	00000000	00000000	**00002214**	**00002214**	HCSPARAMS
08	HcCommandStatus	00000000	00000000	00000000	00000000	**00000012**	**00000012**	HCCPARAMS
0C	HcInterruptStatus	00000000	00000000	00000000	00000000	00080000	00080000	USBCMD
10	HcInterruptEnable	00000000	00000000	00000000	00000000	00001000	00001000	USBSTS
14	HcInterruptDisable	00000000	00000000	00000000	00000000	00000000	00000000	USBINTR
18	HcHCCA	00000000	00000000	00000000	00000000	00000000	00000000	FRINDEX
1C	HcPeriodCurrentED	00000000	00000000	00000000	00000000	00000000	00000000	CTRLDSSEGMENT
20	HcControlHeadED	00000000	00000000	00000000	00000000	00000000	00000000	PERIODICLISTBASE
24	HcControlCurrentED	00000000	00000000	00000000	00000000	00000000	00000000	ASYNCLISTADDR
28	HcBulkHeadED	00000000	00000000	00000000	00000000	-	-	Reserved
2C	HcBulkCurrentED	00000000	00000000	00000000	00000000	-	-	Reserved
30	HcDoneHead	00000000	00000000	00000000	00000000	-	-	Reserved
34	HcFmInterval	00002EDF	00002EDF	00002EDF	00002EDF	-	-	Reserved
38	HcFmRemaining	00000000	00000000	00000000	00000000	-	-	Reserved
3C	HcFmNumber	00000000	00000000	00000000	00000000	-	-	Reserved
40	HcPeriodicStart	00000000	00000000	00000000	00000000	-	-	Reserved
44	HcLSThreshold	00000628	00000628	00000628	00000628	-	-	Reserved
48	HcRhDescriptorA	**FF000902**	**FF000901**	**FF000902**	**FF000901**	-	-	Reserved
4C	HcRhDescriptorB	00000000	00000000	00000000	00000000	00000000	00000000	CONFIGFLAG
50	HcRhStatus	00000000	00000000	00000000	00000000	**00002000**	**00002000**	PORTSC1
54	HcRhPortStatus[1]	00000000	00000000	00000000	00000000	**00002000**	**00002000**	PORTSC2
58	HcRhPortStatus[2]	00000000	-	00000000	-	**00002000**	-	PORTSC3
5C	Reserved	-	-	-	-	**00002000**	-	PORTSC4
FF-60	Reserved	-	-	-	-	-	-	-
100	HceControl	00000000	00000000	00000000	00000000	-	-	-

Table 41: USB Host Controller registers *...continued*

Address (Hex)	OHCI Register	Reset Hex Value[1]						EHCI Register
		Func0 OHCI1 (2P)	Func0 OHCI1 (1P)	Func1 OHCI2 (2P)	Func1 OHCI2 (1P)	Func2 EHCI (4P)	Func2 EHCI (2P)	
104	HceInput	00000000	00000000	00000000	00000000	-	-	-
108	HceOutput	00000000	00000000	00000000	00000000	-	-	-
10C	HceStatus	00000000	00000000	00000000	00000000	-	-	-

[1] Reset hex values that are highlighted (for example, **0**) are the ISP1561 implementation specific reset values, and reset hex values that are not highlighted (for example, 0) are complaint with OHCI and EHCI specification.

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For the OHCI Host Controller, these registers are divided into two types: one set of operational registers for the USB operation and one set of legacy support registers for the legacy keyboard and mouse operation.

For the Enhanced Host Controller, there are two types of registers: one set of read-only capability registers and one set of read/write operational registers.

11.1 OHCI USB Host Controller operational registers

OHCI Host Controller Drivers (HCDs) need to communicate with these registers to implement USB data transfers. Based on their functions, these registers are classified into four partitions:

- Control and Status
- Memory Pointer
- Frame Counter
- Root Hub.

11.1.1 HcRevision register (address: value read from func0 or func1 of address 10H + 00H)

Table 42: HcRevision register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							L
Reset	0	0	0	0	0	0	0	X[1]
Access	-	-	-	-	-	-	-	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	REV[7:0]							
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R	R	R	R

[1] X is 1 for OHCI1 (2P) and OHCI1 (1P); X is 0 for OHCI2 (2P) and OHCI2 (1P).

Table 43: HcRevision register: bit description

Bit	Symbol	Description
31 to 9	-	reserved
8	L	**Legacy**: **0 —** does not support legacy devices **1 —** supports legacy keyboard and mouse
7 to 0	REV[7:0]	**Revision**: This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this Host Controller. For example, a value of 11H corresponds to version 1.1. All of the Host Controller implementations that are compliant with this specification need to have a value of 10H.

11.1.2 HcControl register (address: value read from func0 or func1 of address 10H + 04H)

The HcControl register defines the operating modes for the Host Controller. All the fields in this register, except for HostControllerFunctionalState (HCFS) and RemoteWakeupConnected (RWC), are modified only by the HCD. The bit allocation is given in Table 44.

Table 44: HcControl register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved					RWE	RWC	IR
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	HCFS[1:0]		BLE	CLE	IE	PLE	CBSR[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 45: HcControl register: bit description

Bit	Symbol	Description
31 to 11	-	reserved
10	RWE	**RemoteWakeupEnable:** This bit is used by the HCD to enable or disable the remote wake-up feature upon the detection of upstream resume signaling. When this bit is set and the RD bit in HcInterruptStatus is set, a remote wake-up is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	RWC	**RemoteWakeupConnected:** This bit indicates whether the Host Controller supports remote wake-up signaling. If remote wake-up is supported and used by the system, it is the responsibility of the system firmware to set this bit during POST. The Host Controller clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wake-up signaling of the host system is host-bus-specific and is not described in this specification.
8	IR	**InterruptRouting**: This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. The HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. The HCD uses this bit as a tag to indicate the ownership of the Host Controller.
7 to 6	HCFS[1:0]	**HostControllerFunctionalState** for USB: **00B —** USBRESET **01B —** USBRESUME **10B —** USBOPERATIONAL **11B —** USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. The HCD may determine whether the Host Controller has begun sending SOFs by reading the SF field of HcInterruptStatus. This field may be changed by the Host Controller only when in the USBSUSPEND state. The Host Controller may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. The Host Controller enters USBSUSPEND after a software reset; it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	BLE	**BulkListEnable**: This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by the HCD, processing of the Bulk list does not occur after the next SOF. The Host Controller checks this bit whenever it wants to process the list. When disabled, the HCD may modify the list. If HcBulkCurrentED is pointing to an Endpoint Descriptor (ED) to be removed, the HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

Table 45: HcControl register: bit description…*continued*

Bit	Symbol	Description
4	CLE	**ControlListEnable**: This bit is set to enable the processing of the Control list in the next Frame. If cleared by the HCD, processing of the Control list does not occur after the next SOF. The Host Controller must check this bit whenever it wants to process the list. When disabled, the HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, the HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
3	IE	**IsochronousEnable:** This bit is used by the HCD to enable or disable processing of isochronous EDs. While processing the periodic list in a frame, the Host Controller checks the status of this bit when it finds an Isochronous ED (F = 1). If set (enabled), the Host Controller continues processing the EDs. If cleared (disabled), the Host Controller halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	PLE	**PeriodicListEnable:** This bit is set to enable the processing of the periodic list in the next Frame. If cleared by the HCD, processing of the periodic list does not occur after the next SOF. The Host Controller must check this bit before it starts processing the list.
1 to 0	CBSR[1:0]	**ControlBulkServiceRatio**: This specifies the service ratio of Control EDs over Bulk EDs. Before processing any of the non-periodic lists, the Host Controller must compare the ratio specified with its internal count on how many non-empty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count needs to be retained when crossing the frame boundary. After a reset, the HCD is responsible for restoring this value. **00B —** 1:1 **01B —** 2:1 **10B —** 3:1 **11B —** 4:1

11.1.3 HcCommandStatus register (address: value read from func0 or func1 of address 10H + 08H)

The HcCommandStatus register is used by the Host Controller to receive commands issued by the HCD, and it also reflects the current status of the Host Controller. To the HCD, it appears to be a “write to set” register. The Host Controller must ensure that bits written as logic 1 become set in the register while bits written as logic 0 remain unchanged in the register. The HCD may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The HCD has normal read access to all bits.

The SOC[1:0] (SchedulingOverrunCount) field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun

error is detected, the Host Controller increments the counter and sets the SO (SchedulingOverrun) field in the HcInterruptStatus register. Table 46 shows the bit allocation of the HcCommandStatus register.

Table 46: HcCommandStatus register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved						SOC[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved				OCR	BLF	CLF	HCR
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

Table 47: HcCommandStatus register: bit description

Bit	Symbol	Description
31 to 18	-	reserved
17 to 16	SOC[1:0]	**SchedulingOverrunCount:** The bit is incremented on each scheduling overrun error. It is initialized to 00B and wraps around at 11B. It needs to be incremented when a scheduling overrun is detected even if the SO bit in HcInterruptStatus has already been set. This is used by the HCD to monitor any persistent scheduling problems.
15 to 4	-	reserved
3	OCR	**OwnershipChangeRequest**: This bit is set by an OS HCD to request a change of control of the Host Controller. When set, the Host Controller needs to set the OC (OwnershipChange) field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from the OS HCD.

Table 47: HcCommandStatus register: bit description…*continued*

Bit	Symbol	Description
2	BLF	**BulkListFilled**: This bit is used to indicate whether there are any Transfer Descriptors (TDs) on the Bulk list. It is set by the HCD whenever it adds a TD to an ED in the Bulk list. When the Host Controller begins to process the head of the Bulk list, it checks bulk-filled (BF). If BLF (BulkListFilled) is logic 0, the Host Controller does not need to process the Bulk list. If BLF is logic 1, the Host Controller needs to start processing the Bulk list and set BF to logic 0. If the Host Controller finds a TD on the list, then the Host Controller needs to set BLF to logic 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if the HCD does not set BLF, then BLF is still logic 0 when the Host Controller completes processing the Bulk list and the Bulk list processing stops.
1	CLF	**ControlListFilled**: This bit is used to indicate whether there are any TDs on the Control list. It is set by the HCD whenever it adds a TD to an ED in the Control list. When the Host Controller begins to process the head of the Control list, it checks ControlListFilled (CLF). If CLF is logic 0, the Host Controller does not need to process the Control list. If control-filled (CF) is logic 1, the Host Controller needs to start processing the Control list and set CLF to logic 0. If the Host Controller finds a TD on the list, then the Host Controller needs to set CLF to logic 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set CLF, then CLF is still logic 0 when the Host Controller completes processing the Control list and the Control list processing stops.
0	HCR	**HostControllerReset:** This bit is set by the HCD to initiate a software reset of the Host Controller. Regardless of the functional state of the Host Controller, it moves to the USBSUSPEND state in which most of the operational registers are reset except those stated otherwise; for example, the IR (InterruptRouting) field of HcControl, and no Host bus accesses are allowed. This bit is cleared by the Host Controller upon the completion of the reset operation. The reset operation must be completed within 10 µs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

11.1.4 HcInterruptStatus register (address: value read from func0 or func1 of address 10H + 0CH)

This register is a four-byte register that provides the status of the events that cause hardware interrupts. The bit allocation of the register is given in Table 48. When an event occurs, the Host Controller sets the corresponding bit in this register. When a bit becomes set, a hardware interrupt is generated if the interrupt is enabled in the HcInterruptEnable register (see Table 50) and the MIE (MasterInterruptEnable) bit is set. The HCD may clear specific bits in this register by writing logic 1 to the bit positions to be cleared. The HCD may not set any of these bits. The Host Controller does not clear the bit.

Table 48: HcInterruptStatus register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved	OC			reserved			
Reset	0	0	0	0	0	0	0	0
Access	-	R/W	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49: HcInterruptStatus register: bit description

Bit	Symbol	Description
31	–	reserved
30	OC	**OwnershipChange:** This bit is set by the Host Controller when HCD sets the OCR (OwnershipChangeRequest) field in HcCommandStatus. This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is forced to 0 when the SMI# pin is not implemented.
29 to 7	-	reserved
6	RHSC	**RootHubStatusChange:** This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	FNO	**FrameNumberOverflow:** This bit is set when the MSB of HcFmNumber (bit 15) changes value, or after the HccaFrameNumber has been updated.
4	UE	**UnrecoverableError:** This bit is set when the Host Controller detects a system error not related to USB. The Host Controller should not proceed with any processing nor signaling before the system error has been corrected. The HCD clears this bit after the Host Controller has been reset.
3	RD	**ResumeDetected:** This bit is set when the Host Controller detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when the HCD sets the USBRESUME state.

Table 49: HcInterruptStatus register: bit description…*continued*

Bit	Symbol	Description
2	SF	**StartOfFrame:** At the start of each frame, this bit is set by the Host Controller and an SOF token is generated at the same time.
1	WDH	**WritebackDoneHead**: This bit is set immediately after the Host Controller has written HcDoneHead to HccaDoneHead. Further, updates of HccaDoneHead occur only after this bit has been cleared. The HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	SO	**SchedulingOverrun:** This bit is set when USB schedules for current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun causes the SOC (SchedulingOverrunCount) of HcCommandStatus to be incremented.

11.1.5 HcInterruptEnable register (address: value read from func0 or func1 of address 10H + 10H)

Each enable bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control which events generate a hardware interrupt. If the following conditions occur:

- A bit is set in the HcInterruptStatus register.
- The corresponding bit in the HcInterruptEnable register is set.
- The MIE (MasterInterruptEnable) bit is set.

Then, a hardware interrupt is requested on the host bus.

Writing logic 1 to a bit in this register sets the corresponding bit, whereas writing logic 0 to a bit in this register leaves the corresponding bit unchanged. On a read, the current value of this register is returned.

The bit allocation is given in Table 50.

Table 50: HcInterruptEnable register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	MIE	OC	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 51: HcInterruptEnable register: bit description

Bit	Symbol	Description
31	MIE	**MasterInterruptEnable**: Logic 0 is ignored by the Host Controller. Logic 1 enables interrupt generation by events specified in other bits of this register.
30	OC	**0** — ignore **1** — enable interrupt generation due to Ownership Change
29 to 7	-	reserved
6	RHSC	**0** — ignore **1** — enable interrupt generation due to Root Hub Status Change
5	FNO	**0** — ignore **1** — enable interrupt generation due to Frame Number Overflow
4	UE	**0** — ignore **1** — enable interrupt generation due to Unrecoverable Error
3	RD	**0** — ignore **1** — enable interrupt generation due to Resume Detect
2	SF	**0** — ignore **1** — enable interrupt generation due to Start-of-Frame
1	WDH	**0** — ignore **1** — enable interrupt generation due to HcDoneHead Writeback
0	SO	**0** — ignore **1** — enable interrupt generation due to Scheduling Overrun

11.1.6 HcInterruptDisable register (address: value read from func0 or func1 of address 10H + 14H)

Each disable bit in the HcInterruptDisable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptDisable register is coupled with the HcInterruptEnable register. Therefore, writing logic 1 to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing logic 0 to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged. On a read, the current value of the HcInterruptEnable register is returned. The register contains four bytes, and the bit allocation is given in Table 52.

Table 52: HcInterruptDisable register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	MIE	OC	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	-	-	-	-	-	-

Bit	23	22	21	20	19	18	17	16
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 53: HcInterruptDisable register: bit description

Bit	Symbol	Description
31	MIE	**MasterInterruptEnable**: Logic 0 is ignored by the Host Controller. Logic 1 disables interrupt generation due to events specified in other bits of this register. This field is set after a hardware or software reset. (Interrupts are disabled).
30	OC	**0** — ignore **1** — disable interrupt generation due to Ownership Change
29 to 7	-	reserved
6	RHSC	**0** — ignore **1** — disable interrupt generation due to Root Hub Status Change
5	FNO	**0** — ignore **1** — disable interrupt generation due to Frame Number Overflow
4	UE	**0** — ignore **1** — disable interrupt generation due to Unrecoverable Error
3	RD	**0** — ignore **1** — disable interrupt generation due to Resume Detect
2	SF	**0** — ignore **1** — disable interrupt generation due to Start-of-Frame
1	WDH	**0** — ignore **1** — disable interrupt generation due to HcDoneHead Writeback
0	SO	**0** — ignore **1** — disable interrupt generation due to Scheduling Overrun

11.1.7 HcHCCA register (address: value read from func0 or func1 of address 10H + 18H)

The HcHCCA register contains the physical address of the Host Controller Communication Area (HCCA). The bit allocation is given in Table 54. The HCD determines the alignment restrictions by writing all 1s to HcHCCA and reading the content of HcHCCA. The alignment is evaluated by examining the number of zeroes

in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 will always return logic 0 when read. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the HCD.

Table 54: HcHCCA register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	HCCA[23:16]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	HCCA[15:8]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	HCCA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Table 55: HcHCCA register: bit description

Bit	Symbol	Description
31 to 8	HCCA[23:0]	**Host Controller Communication Area Base Address**: This is the base address of the HCCA.
7 to 0	-	reserved

11.1.8 HcPeriodCurrentED register (address: value read from func0 or func1 of address 10H + 1CH)

The HcPeriodCurrentED register contains the physical address of the current Isochronous or Interrupt ED. Table 56 gives the bit allocation of the register.

Table 56: HcPeriodicCurrentED register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	PCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	PCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8
Symbol	PCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	-	-	-	-

Table 57: HcPeriodCurrentED register: bit description

Bit	Symbol	Description
31 to 4	PCED[27:0]	**PeriodCurrentED**: This is used by the Host Controller to point to the head of one of the Periodic lists that needs to be processed in the current Frame. The content of this register is updated by the Host Controller after a periodic ED has been processed. The HCD may read the content in determining which ED is currently being processed at the time of reading.
3 to 0	-	reserved

11.1.9 HcControlHeadED register (address: value read from func0 or func1 of address 10H + 20H)

The HcControlHeadED register contains the physical address of the first ED of the Control list. The bit allocation is given in Table 58.

Table 58: HcControlHeadED register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	CHED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	CHED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	CHED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CHED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	-	-	-	-

Table 59: HcControlHeadED register: bit description

Bit	Symbol	Description
31 to 4	CHED[27:0]	**ControlHeadED:** The Host Controller traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of the Host Controller.
3 to 0	-	reserved

11.1.10 HcControlCurrentED register (address: value read from func0 or func1 of address 10H + 24H)

The HcControlCurrentED register contains the physical address of the current ED of the Control list. The bit allocation is given in Table 60.

Table 60: HcControlCurrentED register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	CCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	CCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	CCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	-	-	-	-

Table 61: HcControlCurrentED register: bit description

Bit	Symbol	Description
31 to 4	CCED[27:0]	**ControlCurrentED**: This pointer is advanced to the next ED after serving the present one. The Host Controller needs to continue processing the list from where it left off in the last frame. When it reaches the end of the Control list, the Host Controller checks the CLF (ControlListFilled) bit of HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. The HCD is allowed to modify this register only when the CLE (ControlListEnable) bit of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. Initially, this is set to logic 0 to indicate the end of the Control list.
3 to 0	-	reserved

11.1.11 HcBulkHeadED register (address: value read from func0 or func1 of address 10H + 28H)

This is a four-byte register, and the bit allocation is given in Table 62. The register contains the physical address of the first ED of the Bulk list.

Table 62: HcBulkHeadED register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	BHED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BHED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BHED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BHED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	-	-	-	-

Table 63: HcBulkHeadED register: bit description

Bit	Symbol	Description
31 to 4	BHED[27:0]	**BulkHeadED:** The Host Controller traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of the Host Controller.
3 to 0	-	reserved

11.1.12 HcBulkCurrentED register (address: value read from func0 or func1 of address 10H + 2CH)

This register contains the physical address of the current endpoint of the Bulk list. As the Bulk list needs to be served in a round-robin fashion, the endpoints are ordered according to their insertion to the list. The bit allocation is given in Table 64.

Table 64: HcBulkCurrentED register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	BCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Symbol	BCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	-	-	-	-

Table 65: HcBulkCurrentED register: bit description

Bit	Symbol	Description
31 to 4	BCED[27:0]	**BulkCurrentED**: This is advanced to the next ED after the Host Controller has served the present one. The Host Controller continues processing the list from where it left off in the last frame. When it reaches the end of the Bulk list, the Host Controller checks the CLF (ControlListFilled) bit of HcControl. If the CLF bit is not set, nothing is done. If the CLF bit is set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the CLF bit. The HCD can only modify this register when the BLE (BulkListEnable) bit of HcControl is cleared. When HcControl is set, the HCD reads the instantaneous value of this register. This is initially set to 0 to indicate the end of the Bulk list.
3 to 0	-	reserved

11.1.13 HcDoneHead register (address: value read from func0 or func1 of address 10H + 30H)

The HcDoneHead register contains the physical address of the last completed TD that was added to the Done queue. In normal operation, the HCD does not need to read this register as its content is periodically written to the HCCA. Table 66 contains the bit allocation of the register.

Table 66: HcDoneHead register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	DH[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	DH[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DH[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	DH[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	-	-	-	-

Table 67: HcDoneHead register: bit description

Bit	Symbol	Description
31 to 4	DH[27:0]	**DoneHead:** When a TD is completed, the Host Controller writes the content of HcDoneHead to the NextTD field of the TD. The Host Controller then overwrites the content of HcDoneHead with the address of this TD. This is set to logic 0 whenever the Host Controller writes the content of this register to HCCA.
3 to 0	-	reserved

11.1.14 HcFmInterval register (address: value read from func0 or func1 of address 10H + 34H)

The HcFmInterval register contains a 14-bit value that indicates the bit time interval in a frame, (that is, between two consecutive SOFs) and a 15-bit value indicating the full-speed maximum packet size that the Host Controller may transmit or receive without causing a scheduling overrun. The HCD may carry out minor adjustment on the FI (FrameInterval) by writing a new value over the present one at each SOF. This provides the possibility for the Host Controller to synchronize with an external clocking resource and to adjust any unknown local clock offset. The bit allocation of the register is given in Table 68.

Table 68: HcFmInterval register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	FIT	FSMPS[14:8]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	FSMPS[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved		FI[13:8]					
Reset	0	0	1	0	1	1	1	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FI[7:0]							
Reset	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 69: HcFmInterval register: bit description

Bit	Symbol	Description
31	FIT	**FrameIntervalToggle**: The HCD toggles this bit whenever it loads a new value to FrameInterval.
30 to 16	FSMPS[14:0]	**FSLargestDataPacket**: This field specifies a value that is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits that can be sent or received by the Host Controller in a single transaction at any given time without causing a scheduling overrun. The field value is calculated by the HCD.
15 to 14	-	reserved
13 to 0	FI[13:0]	**FrameInterval:** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to 11,999. The HCD should store the current value of this field before resetting the Host Controller because this causes the field to be reset the nominal value. The HCD can then restore the stored value upon the completion of the reset sequence.

11.1.15 HcFmRemaining register (address: value read from func0 or func1 of address 10H + 38H)

The HcFmRemaining register is a 14-bit down counter showing the bit time remaining in the current Frame. Table 70 contains the bit allocation of this four-byte register.

Table 70: HcFmRemaining register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	FRT	reserved						
Reset	0	0	0	0	0	0	0	0
Access	R/W	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved		FR[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FR[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 71: HcFmRemaining register: bit description

Bit	Symbol	Description
31	FRT	**FrameRemainingToggle:** This bit is loaded from the FIT (FrameIntervalToggle) field of HcFmInterval whenever FR (FrameRemaining) reaches 0. This bit is used by the HCD for the synchronization between FI (FrameInterval) and FR.
30 to 14	-	reserved
13 to 0	FR[13:0]	**FrameRemaining:** This counter is decremented at each bit time. When it reaches 0, it is reset by loading the FI value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, the Host Controller re-loads the content with the FI of HcFmInterval and uses the updated value from the next SOF.

11.1.16 HcFmNumber register (address: value read from func0 or func1 of address 10H + 3CH)

This register is a 16-bit counter, and the bit allocation is given in Table 72. It provides a timing reference among events happening in the Host Controller and the HCD. The HCD may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

Table 72: HcFmNumber register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved		FN[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 73: HcFmNumber register: bit description

Bit	Symbol	Description
31 to 14	-	reserved
13 to 0	FN[13:0]	**FrameNumber**: This is incremented when HcFmRemaining is re-loaded. It needs to be rolled over to 0H after FFFFH. When entering the USBOPERATIONAL state, this is incremented automatically. The content is written to HCCA after the Host Controller has incremented FrameNumber at each frame boundary and sent a SOF but before the Host Controller reads the first ED in that frame. After writing to HCCA, the Host Controller sets the SF (StartofFrame) in HcInterruptStatus.

11.1.17 HcPeriodicStart register (address: value read from func0 or func1 of address 10H + 40H)

The HcPeriodicStart register has a 14-bit programmable value that determines when is the earliest time the Host Controller should start processing the periodic list. The bit allocation is given in Table 74.

Table 74: HcPeriodicStart register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved		P_S[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	P_S[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 75: HcPeriodicStart register: bit description

Bit	Symbol	Description
31 to 14	-	reserved
13 to 0	P_S[13:0]	**PeriodicStart:** After a hardware reset, this field is cleared. This is then set by the HCD during the Host Controller initialization. The value is calculated roughly as 10% of the HcFmInterval. A typical value is 3E67H. When HcFmRemaining reaches the value specified, processing of the periodic lists have priority over Control/Bulk processing. The Host Controller, therefore, starts processing the Interrupt list after completing the current Control or the Bulk transaction that is in progress.

11.1.18 HcLSThreshold register (address: value read from func0 or func1 of address 10H + 44H)

This register contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the Host Controller nor the HCD are allowed to change this value. The bit allocation of the HcLSThreshold register is given in Table 76.

Table 76: HcLSThreshold register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved				LST[11:8]			
Reset	0	0	0	0	0	1	1	0
Access	-	-	-	-	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LST[7:0]							
Reset	0	0	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77: HcLSThreshold register: bit description

Bit	Symbol	Description
31 to 12	-	reserved
11 to 0	LST[11:0]	**LSThreshold**: This field contains a value that is compared to the FR (FrameRemaining) field prior to initiating a low-speed transaction. The transaction is started only if FR ≥ this field. The value is calculated by the HCD with the consideration of transmission and setup overhead.

11.1.19 HcRhDescriptorA register (address: value read from func0 or func1 of address 10H + 48H)

The HcRhDescriptorA register is the first of two registers describing the characteristics of the Root Hub. Reset values are implementation-specific. The descriptor length (11), descriptor type (TBD) and hub controller current (0) fields of the hub Class Descriptor are emulated by the HCD. All other fields are located in the HcRhDescriptorA and HcRhDescriptorB registers. Table 78 contains the bit allocation of the HcRhDescriptorA register.

Table 78: HcRhDescriptorA register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	POTPGT[7:0]							
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved			NOCP	OCPM	DT	NPS	PSM
Reset	0	0	0	0	1	0	0	1
Access	-	-	-	R/W	R/W	R	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	NDP[7:0]							
Reset	0	0	0	0	0	0	X[1]	X[2]
Access	R	R	R	R	R	R	R	R

[1] X is 1 for OHCI1 (2P) and OHCI2 (2P); X is 0 for OHCI1 (1P) and OHCI2 (1P).

[2] X is 0 for OHCI1 (2P) and OHCI2 (2P); X is 1 for OHCI1 (1P) and OHCI2 (1P).

Table 79: HcRhDescriptorA register: bit description

Bit	Symbol	Description
31 to 24	POTPGT[7:0]	**PowerOnToPowerGoodTime:** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT × 2 ms.
23 to 13	-	reserved
12	NOCP	**NoOverCurrentProtection:** This bit describes how the overcurrent status for Root Hub ports are reported. When this bit is cleared, the OCPM (OverCurrentProtectionMode) field specifies global or per-port reporting. **0 —** overcurrent status is reported collectively for all downstream ports **1 —** no overcurrent protection supported
11	OCPM	**OverCurrentProtectionMode**: This bit describes how the overcurrent status for Root Hub ports are reported. At reset, this fields reflects the same mode as PowerSwitchingMode. This field is valid only if the NOCP field is cleared. **0 —** overcurrent status is reported collectively for all downstream ports **1 —** overcurrent status is reported on a per-port basis
10	DT	**DeviceType**: This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read 0.

Table 79: HcRhDescriptorA register: bit description…*continued*

Bit	Symbol	Description
9	NPS	**NoPowerSwitching**: This bit is used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PSM (PowerSwitchingMode) field specifies global or per-port switching. **0 —** ports are power switched **1 —** ports are always powered on when the Host Controller is powered on
8	PSM	**PowerSwitchingMode:** This bit is used to specify how the power switching of Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NPS field is cleared. **0 —** all ports are powered at the same time. **1 —** each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PPCM (PortPowerControlMask) bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
7 to 0	NDP[7:0]	**NumberDownstreamPorts:** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OHCI is 15.

11.1.20 HcRhDescriptorB register (address: value read from func0 or func1 of address 10H + 4CH)

The HcRhDescriptorB register is the second of two registers describing the characteristics of the Root Hub. The bit allocation is given in Table 80. These fields are written during initialization to correspond with the system implementation. Reset values are implementation-specific.

Table 80: HcRhDescriptorB register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	PPCM[15:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	PPCM[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DR[15:8]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	DR[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 81: HcRhDescriptorB register: bit description

Bit	Symbol	Description
31 to 16	PPCM[15:0]	**PortPowerControlMask:** Each bit indicates whether a port is affected by a global power control command when PowerSwitchingMode is set. When set, the power state of the port is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. **Bit 0 —** reserved **Bit 1 —** Ganged-power mask on Port #1 **Bit 2 —** Ganged-power mask on Port #2.
15 to 0	DR[15:0]	**DeviceRemovable:** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. **Bit 0 —** reserved **Bit 1 —** Device attached to Port #1 **Bit 2 —** Device attached to Port #2.

11.1.21 HcRhStatus register (address: value read from func0 or func1 of address 10H + 50H)

The HcRhStatus register is divided into two parts. The lower word of a DWord represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written as logic 0. Table 82 contains the bit allocation of the register.

Table 82: HcRhStatus register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	CRWE	reserved						
Reset	0	0	0	0	0	0	0	0
Access	R/W	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved						CCIC	LPSC
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DRWE	reserved						
Reset	0	0	0	0	0	0	0	0
Access	R/W	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						OCI	LPS
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	R	RW

Table 83: HcRhStatus register: bit description

Bit	Symbol	Description
31	CRWE	On write—**ClearRemoteWakeupEnable:** Writing logic 1 clears DRWE (DeviceRemoteWakeupEnable). Writing logic 0 has no effect.
30 to 18	-	reserved
17	CCIC	**OverCurrentIndicatorChange:** This bit is set by hardware when a change has occurred to the OCI (OverCurrentIndicator) field of this register. The HCD clears this bit by writing logic 1. Writing logic 0 has no effect.
16	LPSC	On read—**LocalPowerStatusChange:** The Root Hub does not support the local power status feature. Therefore, this bit is always logic 0. On write—**SetGlobalPower:** In the global power mode (PowerSwitchingMode = 0), this bit is written to logic1 to turn on power to all ports (clear PortPowerStatus). In the per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing logic 0 has no effect.
15	DRWE	On read—**DeviceRemoteWakeupEnable:** This bit enables the bit ConnectStatusChange as a resume event, causing a state transition USBSUSPEND to USBRESUME and setting the ResumeDetected interrupt. **0 —** ConnectStatusChange is not a remote wake-up event **1 —** ConnectStatusChange is a remote wake-up event On write—**SetRemoteWakeupEnable:** Writing logic 1 sets DRWE (DeviceRemoteWakeupEnable). Writing logic 0 has no effect.
14 to 2	-	reserved
1	OCI	**OverCurrentIndicator:** This bit reports overcurrent conditions when global reporting is implemented. When set, an overcurrent condition exists. When clear, all power operations are normal. If the per-port overcurrent protection is implemented, this bit is always logic 0.
0	LPS	On read—**LocalPowerStatus:** The Root Hub does not support the local power status feature. Therefore, this bit is always read as logic 0. On write—**ClearGlobalPower:** In the global power mode (PowerSwitchingMode = 0), this bit is written to logic 1 to turn off power to all ports (clear PortPowerStatus). In the per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing logic 0 has no effect.

11.1.22 HcRhPortStatus[1:4] register (address: value read from func0 or func1 of address 10H + 54H)

The HcRhPortStatus[1:4] register is used to control and report port events on a per-port basis. NumberDownstreamPorts represents the number of HcRhPortStatus registers that are implemented in hardware. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behavior. If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change is postponed until the transaction completes. Reserved bits should always be written logic 0. The bit allocation of the register is given in Table 84.

Table 84: HcRhPortStatus[1:4] register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved			PRSC	OCIC	PSSC	PESC	CSC
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved						LSDA	PPS
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			PRS	POCI	PSS	PES	CCS
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Table 85: HCRhPortStatus[1:4] register: bit description

Bit	Symbol	Description
31 to 21	-	reserved
20	PRSC	**PortResetStatusChange:** This bit is set at the end of the 10 ms port reset signal. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** port reset is not complete **1 —** port reset is complete
19	OCIC	**PortOverCurrentIndicatorChange:** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when the Root Hub changes the POCI (PortOverCurrentIndicator) bit. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** no change in PortOverCurrentIndicator **1 —** POCI has changed

Table 85: HCRhPortStatus[1:4] register: bit description *...continued*

Bit	Symbol	Description
18	PSSC	**PortSuspendStatusChange:** This bit is set when the full resume sequence has been completed. This sequence includes the 20 ms resume pulse, LS EOP and 3 ms re-synchronization delay. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. This bit is also cleared when ResetStatusChange is set. **0 —** resume is not completed **1 —** resume is completed
17	PESC	**PortEnableStatusChange:** This bit is set when hardware events cause the PES (PortEnableStatus) bit to be cleared. Changes from the HCD writes do not set this bit. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** no change in PES **1 —** change in PES
16	CSC	**ConnectStatusChange:** This bit is set whenever a connect or disconnect event occurs. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. If CCS (CurrentConnectStatus) is cleared when a SetPortReset, SetPortEnable or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status because these writes should not occur if the port is disconnected. **0 —** no change in CCS **1 —** change in CCS **Remark:** If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15 to 10	-	reserved
9	LSDA	On read—**LowSpeedDeviceAttached:** This bit indicates the speed of the device attached to this port. When set, a low-speed device is attached to this port. When clear, a full-speed device is attached to this port. This field is valid only when the CCS is set. **0 —** port is not suspended **1 —** port is suspended On write—**ClearPortPower:** The HCD can clear the PPS (PortPowerStatus) bit by writing logic 1 to this bit. Writing logic 0 has no effect.

Table 85: HCRhPortStatus[1:4] register: bit description *...continued*

Bit	Symbol	Description
8	PPS	On read—**PortPowerStatus:** This bit reflects the port power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. The HCD can set this bit by writing SetPortPower or SetGlobalPower. The HCD can clear this bit by writing ClearPortPower or ClearGlobalPower. PowerSwitchingMode and PortPowerControlMask[NDP] determine which power control switches are enabled. In the global switching mode (PowerSwitchingMode = 0), only Set/ClearGlobalPower controls this bit. In the per-port power switching (PowerSwitchingMode = 1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CCS (CurrentConnectStatus), PES (PortEnableStatus), PSS (PortSuspendStatus) and PRS (PortResetStatus) should be reset. **0 —** port power is OFF **1 —** port power is ON On write—**SetPortPower:** The HCD can write logic 1 to set the PPS (PortPowerStatus) bit. Writing logic 0 has no effect. **Remark:** This bit always reads logic1 if power switching is not supported.
7 to 5	-	reserved
4	PRS	On read—**PortResetStatus:** When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed and PRSC (PortResetStatusChange) is set, this bit is cleared. **0 —** port reset signal is not active **1 —** port reset signal is active On write—**SetPortReset:** The HCD can set the port reset signaling by writing a 1 to this bit. Writing a 0 has no effect. If CCS is cleared, this write does not set PRS (PortResetStatus) but instead sets CCS. This informs the driver that it attempted to reset a disconnected port.
3	POCI	On read—**PortOverCurrentIndicator:** This bit is valid only when the Root Hub is configured to show overcurrent conditions are reported on a per-port basis. If the per-port overcurrent reporting is not supported, this bit is set to logic 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. **0 —** no overcurrent condition **1 —** overcurrent condition detected On write—**ClearSuspendStatus:** The HCD can write logic 1 to initiate a resume. Writing logic 0 has no effect. A resume is initiated only if PSS (PortSuspendStatus) is set.

Table 85: HCRhPortStatus[1:4] register: bit description *...continued*

Bit	Symbol	Description
2	PSS	On read—**PortSuspendStatus:** This bit indicates whether the port is suspended or is in the resume sequence. It is set by a SetSuspendState write and cleared when PSSC (PortSuspendStatusChange) is set at the end of the resume interval. This bit is not set if CCS (CurrentConnectStatus) is cleared. This bit is also cleared when PRSC (PortResetStatusChange) is set at the end of the port reset or when the Host Controller is placed in the USBRESUME state. If an upstream resume is in progress, it will propagate to the Host Controller. **0 —** port is not suspended **1 —** port is suspended On write**—SetPortSuspend:** The HCD can set the PSS (PortSuspendStatus) bit by writing logic 1 to this bit. Writing logic 0 has no effect. If CCS is cleared, this write does not set PSS; instead it sets CSS. This informs the driver that it attempted to suspend a disconnected port.
1	PES	On read**—PortEnableStatus:** This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power or operational bus error is detected. This change also causes PortEnabledStatusChange to be set. The HCD can set this bit by writing SetPortEnable and clear it by writing ClearPortEnable. This bit cannot be set when CCS (CurrentConnectStatus) is cleared. This bit is also set at the completion of a port reset when ResetStatusChange is set or at the completion of a port suspend when SuspendStatusChange is set. **0 —** port is disable **1 —** port is enabled On write**—SetPortEnable:** The HCD can set PES (PortEnableStatus) by writing logic 1. Writing logic 0 has no effect. If CCS is cleared, this write does not set PES, but instead sets CSC (ConnectStatusChange). This informs the driver that it attempted to enable a disconnected port.
0	CCS	On read—**CurrentConnectStatus:** This bit reflects the current state of the downstream port. **0 —** no device connected **1 —** device connected On write—**ClearPortEnable:** The HCD can write logic 1 to this bit to clear the PES (PortEnableStatus) bit. Writing logic 0 has no effect. The CCS (CurrentConnectStatus) bit, on read, is not affected by any write to ClearPortEnable. **Remark:** This bit always reads logic 1 when the attached device is nonremovable (DeviceRemoveable[NDP]).

11.2 USB legacy support registers

The ISP1561 supports legacy keyboards and mice. Four operational registers are used to provide the legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100H.

Table 86: Legacy support registers

Offset	Register	Description
100H	HceControl	Used to enable and control the emulation hardware and report various status information
104H	HceInput	Emulation of the legacy Input Buffer register
108H	HceOutput	Emulation of the legacy Output Buffer register where keyboard and mouse data is to be written by software
10CH	HceStatus	Emulation of the legacy Status register

Table 87: Emulated registers

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60H	IN	HceOutput	IN from port 60H sets OutputFull in HceStatus to 0
60H	OUT	HceInput	OUT to port 60H sets InputFull to 1 and CmdData to 0 in HceStatus
64H	IN	HceStatus	IN from port 64H returns current value of HceStatus with no other side effect
64H	OUT	HceInput	OUT to port 64H sets InputFull to 0 and CmdData in HceStatus to 1

11.2.1 HceControl register (address: value read from func0 or func1 of address 10H + 100H)

Table 88: HceControl register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							A20S
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IRQ12A	IRQ1A	GA20S	EIRQEn	IRQEn	C_P	EI	EE
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Table 89: HceControl register: bit description

Bit	Symbol	Description
31 to 9	-	reserved
8	A20S	**A20State**: This bit indicates the current state of Gate A20 on the keyboard controller. It is used to compare against value written to 60H when GA20S (GateA20Sequence) is active.
7	IRQ12A	**IRQ12Active**: This bit indicates that a positive transition on IRQ12 from the keyboard controller has occurred. Writing a logic 1 sets IRQ12 to logic 0 (inactive). Writing a logic 0 to this bit has no effect.
6	IRQ1A	**IRQ1Active**: This bit indicates that a positive transition on IRQ1 from the keyboard controller has occurred. Writing a logic 1 sets IRQ1 to logic 0 (inactive). Writing a logic 0 to this bit has no effect.
5	GA20S	**GateA20Sequence**: This bit is set by the Host Controller when a data value of D1H is written to I/O port 64H and cleared, on a write to I/O port 64H of any value other than D1H.
4	EIRQEn	**ExternalIRQEn**: When this bit is set to logic 1, IRQ1 and IRQ12 from the keyboard controller cause an emulation interrupt. This bit is independent of the setting of the EE (EmulationEnable) bit in this register.
3	IRQEn	**IRQEn**: When this bit is set, the Host Controller generates IRQ1 or IRQ12 as long as the OUT_FULL (OutputFull) bit in HceStatus is set to logic 1. If the AUX_OUT_FULL (AuxOutputFull) bit of HceStatus is logic 0, then IRQ1 is generated; if it is logic 1, then an IRQ12 is generated.
2	C_P	**CharacterPending**: When this bit is set, an emulation interrupt is generated when the OUT_FULL (OutputFull) bit of the HceStatus register is set to logic 0.
1	EI	**EmulationInterrupt**: This bit shows the emulation interrupt condition. **logic 0 —** legacy emulation enabled **logic 1 —** legacy emulation disabled
0	EE	**EmulationEnable**: When this bit is set to logic 1, the Host Controller is enabled for legacy emulation. The Host Controller decodes accesses to I/O registers 60H and 64H and enables interrupts on IRQ1 and/or IRQ12. The Host Controller also generates an emulation interrupt at appropriate times to invoke the emulation software.

11.2.2 HceInput register (address: value read from func0 or func1 of address 10H + 104H)

The HceInput register is a four-byte register, and the bit allocation is given in Table 90. I/O data that is written to ports 60H and 64H is captured in this register when emulation is enabled. This register may be read or written directly by accessing it in the Host Controller's operational register space. When accessed directly in a memory cycle, reads and writes of this register have no side effects.

Table 90: HceInput register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IN_DATA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 91: HceInput register: bit description

Bit	Symbol	Description
31 to 8	-	reserved
7 to 0	IN_DATA[7:0]	**InputData**: This register holds data that is written to I/O ports 60H or 64H.

11.2.3 HceOutput register (address: value read from func0 or func1 of address 10H + 108H)

Data placed in this register by the emulation software is returned when I/O port 60H is read and emulation is enabled. On a read of this location, the OUT_FULL (OutputFull) bit in HceStatus is set to logic 0. The bit allocation is given in Table 92.

Table 92: HceOutput register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_DATA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 93: HceOutput register: bit description

Bit	Symbol	Description
31 to 8	-	reserved
7 to 0	OUT_DATA[7:0]	**OutputData**: This register holds the data that is returned when an I/O read of port 60H is requested by application software.

11.2.4 HceStatus register (address: value read from func0 or func1 of address 10H + 10CH)

The contents of the HceStatus register are returned on an I/O read of port 64H when emulation is enabled. Reads and writes of port 60H and writes to port 64H can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects. Table 94 contains the bit allocation.

Table 94: HceStatus register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PARITY	TIMEOUT	AUX_OUT_FULL	INH_SW	CMD_DATA	FLAG	IN_FULL	OUT_FULL
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 95: HceStatus register: bit description

Bit	Symbol	Description
31 to 8	-	reserved
7	PARITY	**Parity**: This bit indicates parity error on keyboard and mouse data.
6	TIMEOUT	**Timeout**: This bit indicates a timeout.

Table 95: HceStatus register: bit description…*continued*

Bit	Symbol	Description
5	AUX_OUT_FULL	**AuxOutputFull**: IRQ12 is asserted whenever this bit is set to logic 1, OUT_FULL (OutputFull) is set to logic 1, and the IRQEn bit is set.
4	INH_SW	**Inhibit Switch**: This bit reflects the state of the keyboard inhibit switch. If set, the keyboard is active.
3	CMD_DATA	**CmdData**: The Host Controller sets this bit to logic 0 on an I/O write to port 60H and to logic 1 on an I/O write to port 64H.
2	FLAG	**Flag**: Nominally used as a system flag by software to indicate a warm or cold boot.
1	IN_FULL	**InputFull**: Except for the case of a Gate A20 sequence, this bit is set to logic 1 on an I/O write to address 60H or 64H. While this bit is set to logic 1 and emulation is enabled, an emulation interrupt condition exists.
0	OUT_FULL	**OutputFull**: The Host Controller sets this bit to logic 0 on a read of I/O port 60H. If IRQEn is set, AUX_OUT_FULL (AuxOutputFull) determines which IRQ is activated. While this bit is logic 0 and CharacterPending in HceControl is set to logic 1, an emulation interrupt condition exists.

11.3 EHCI controller capability registers

Other than the OHCI Host Controller, there are some registers in EHCI that define the capability of EHCI. The address range of these registers is located before the operational registers.

11.3.1 CAPLENGTH/HCIVERSION register (address: value read from func2 of address 10H + 00H)

The bit allocation of this four-byte register is given in Table 96.

Table 96: CAPLENGTH/HCIVERSION register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	HCIVERSION[15:8]							
Reset	1	0	0	1	0	1	0	1
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	HCIVERSION[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CAPLENGTH[7:0]							
Reset	0	0	0	0	1	1	0	0
Access	R	R	R	R	R	R	R	R

Table 97: CAPLENGTH/HCIVERSION register: bit description

Bit	Symbol	Description
31 to 24	-	reserved
23 to 8	HCIVERSION [15:0]	**Host Controller Interface Version Number**: It contains a BCD encoding of the version number if the interface to which the Host Controller interface conforms to the standard.
7 to 0	CAPLENGTH [7:0]	**Capability Register Length**: This is used as an offset. It is added to the register base to find the beginning of the Operational Register Space.

11.3.2 HCSPARAMS register (address: value read from func2 of address 10H + 04H)

The Host Controller Structural Parameters (HCSPARAMS) register is a set of fields that are structural parameters. The bit allocation is given in Table 98.

Table 98: HCSPARAMS register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	DPN[3:0]				reserved			P_INDICATOR
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	-	-	-	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	N_CC[3:0]				N_PCC[3:0]			
Reset	0	0	1	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PRR	reserved		PPC	N_PORTS[3:0]			
Reset	0	0	0	1	0	1	0	0
Access	R	-	-	R	R	R	R	R

Table 99: HCSPARAMS register: bit description

Bit	Symbol	Description
31 to 24	-	reserved
23 to 20	DPN[3:0]	**Debug Port Number**: This field identifies which of the Host Controller ports is the debug port. A non-zero value in this field indicates the presence of a debug port. The value in this register must not be greater than N_PORTS.
19 to 17		reserved
16	P_INDICATOR	**Port Indicators**: This bit indicates whether the ports support port indicator control. When this bit is logic 1, the port status and control registers include a read/writeable field for controlling the state of the port indicator.

Table 99: HCSPARAMS register: bit description…*continued*

Bit	Symbol	Description
15 to 12	N_CC [3:0]	**Number of Companion Controller**: This field indicates the number of companion controllers associated with this Hi-Speed USB Host Controller. A value of zero in this field indicates there are no companion Host Controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the Host Controller root ports. A value larger than zero in this field indicates there are companion Original USB Host Controller(s). Port-ownership hand-offs are supported.
11 to 8	N_PCC [3:0]	**Number of Ports per Companion Controller**: This field indicates the number of ports supported per companion Host Controller. It is used to indicate the port routing configuration to system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, N_PCC could have been 4, in which the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC.
7	PRR	**Port Routing Rules**: This field indicates the method used for mapping ports to the companion controllers. **0 —** The first N_PCC ports are routed to the lowest numbered function companion Host Controller, the next N_PCC ports are routed to the next lowest function companion controller, and so on. **1 —** The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array.
6 to 5	-	reserved
4	PPC	**Port Power Control:** This field indicates whether the Host Controller implementation includes port power control. Logic 1 indicates the port has port power switches. Logic 0 indicates the port does not have port power switches. The value of this field affects the functionality of the Port Power field in each port status and control register.
3 to 0	N_PORTS [3:0]	**N_Ports**: This field specifies the number of physical downstream ports implemented on this Host Controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1H to FH. Logic 0 in this field is undefined.

11.3.3 HCCPARAMS register (address: value read from func2 of address 10H + 08H)

The Host Controller Capability Parameters (HCCPARAMS) register is a four-byte register, and the bit allocation is given in Table 100.

Table 100: HCCPARAMS register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IST[3:0]				reserved		PFLF	64AC
Reset	0	0	0	1	0	0	1	0
Access	R	R	R	R	-	-	R	R

Table 101: HCCPARAMS register: bit description

Bit	Symbol	Description
31 to 8	-	reserved
7 to 4	IST[3:0]	**Isochronous Scheduling Threshold**: Default = implementation dependent. This field indicates, relative to the current position of the executing Host Controller, where software can reliably update the isochronous schedule. When (IST[3]) is logic 0, then the value of the least significant 3 bits indicates the number of microframes a Host Controller can hold a set of isochronous data structures (one or more) before flushing the state. When IST[3] is logic 1, then host software assumes the Host Controller may cache an isochronous data structure for an entire frame.
3 to 2	-	reserved
1	PFLF	**Programmable Frame List Flag**: Default = implementation dependent. If this bit is cleared, the system software must use a frame list length of 1024 elements with this Host Controller. The USBCMD register FLS (Frame List Size) field is a read-only register and should be cleared. If PFLF is set, the system software can specify and use a smaller frame list and configure the host via the USBCMD register FLS field. The frame list must always be aligned on a 4 K page boundary to ensure that the frame list is always physically contiguous.
0	64AC	**64-bit Addressing Capability**: This field documents the addressing range capability. **0 —** data structures using 32-bit address memory pointers **1 —** data structures using 64-bit address memory pointers

11.4 Operational registers of Enhanced USB Host Controller

11.4.1 USBCMD register (address: value read from func2 of address 10H + 0CH)

The USB Command (USBCMD) register indicates the command to be executed by the serial Host Controller. Writing to this register causes a command to be executed. Table 102 shows the USBCMD register bit allocation.

Table 102: USBCMD register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	ITC[7:0]							
Reset	0	0	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LHCR	IAAD	ASE	PSE	FLS[1:0]		HC RESET	RS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 103: USBCMD register: bit description

Bit	Symbol	Description
31 to 24	-	reserved
23 to 16	ITC[7:0]	**Interrupt Threshold Control**: Default 08H. This field is used by system software to select the maximum rate at which the Host Controller will issue interrupts. Valid values are defined below. If software writes an invalid value to this register, the results are undefined. **00H —** reserved **01H —** 1 microframe **02H —** 2 microframes **04H —** 4 microframes **08H —** 8 microframes (equals 1 ms) **10H —** 16 microframes (equals 2 ms) **20H —** 32 microframes (equals 4 ms) **40H —** 64 microframes (equals 8 ms) Software modifications to this field while HCH (HCHalted) bit is zero results in undefined behavior.

Table 103: USBCMD register: bit description...*continued*

Bit	Symbol	Description
15 to 8	-	reserved
7	LHCR	**Light Host Controller Reset**: This control bit is not required. It allows the driver software to reset the EHCI controller without affecting the state of the ports or the relationship to the companion Host Controllers. If not implemented, a read of this field will always return zero.If implemented, on read: **logic 0 —** indicates the Light Host Controller Reset has completed and it is ready for the host software to re-initialize the Host Controller **logic 1 —** indicates the Light Host Controller Reset has not yet completed
6	IAAD	**Interrupt on Asynchronous Advance Doorbell**: This bit is used as a doorbell by software to tell the Host Controller to issue an interrupt the next time it advances the asynchronous schedule. Software must write logic 1 to this bit to ring the doorbell. When the Host Controller has evicted all appropriate cached schedule states, it sets the IAA (Interrupt on Asynchronous Advance) status bit in the USBSTS register. If the IAAE (Interrupt on Asynchronous Advance Enable) bit in the USBINTR register is a one, then the Host Controller will assert an interrupt at the next interrupt threshold. The Host Controller sets this bit to a zero after it sets the IAA (Interrupt on Asynchronous Advance) status bit in the USBSTS register. Software should not set this bit when the asynchronous schedule is inactive as this results in an undefined value.
5	ASE	**Asynchronous Schedule Enable**: Default = 0. This bit controls whether the Host Controller skips processing the Asynchronous Schedule. **logic 0 —** Do not process the Asynchronous Schedule **logic 1 —** Use the ASYNCLISTADDR register to access the Asynchronous Schedule
4	PSE	**Periodic Schedule Enable**: Default 0. This bit controls whether the Host Controller skips processing the Periodic Schedule. **logic 0 —** Do not process the Periodic Schedule **logic 1 —** Use the PERIODICLISTBASE register to access the Periodic Schedule
3 to 2	FLS[1:0]	**Frame List Size**: Default 00B. This field is R/W only if PFLF (Programmable Frame List Flag) in the HCCPARAMS register is set to a one. This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index register should be used for the Frame List Current index. **00B —** 1024 elements (4096 bytes) **01B —** 512 elements (2048 bytes) **10B —** 256 elements (1024 bytes) for small environments **11B —** reserved.

Table 103: USBCMD register: bit description...*continued*

Bit	Symbol	Description
1	HCRESET	**Host Controller Reset**: This control bit is used by the software to reset the Host Controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. Setting this bit causes the Host Controller to reset its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion Host Controller(s). The software must re-initialize the Host Controller to return it to an operational state. This bit is cleared by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should check the HCH (HCHalted) bit in the USBSTS register is zero before setting this bit. Attempting to reset an actively running Host Controller results in undefined behavior.
0	RS	**Run/Stop**: 1 = Run. 0 = Stop. When set, the Host Controller executes the schedule. The Host Controller continues execution as long as this bit is set. When this bit is cleared, the Host Controller completes the current and active transactions in the USB pipeline, and then halts. The HCH (HCHalted) bit in the USBSTS register indicates when the Host Controller has finished the transaction and has entered the stopped state. Software should check HCH (HCHalted) in the USBSTS register is logic 1 before setting this bit.

11.4.2 USBSTS register (address: value read from func2 of address 10H + 10H)

The USB Status (USBSTS) register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software clears the register bits by writing ones to them. The bit allocation is given in Table 104.

Table 104: USBSTS register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	ASS	PSSTAT	RECL	HCH	reserved			
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	-	-	-	-

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		IAA	HSE	FLR	PCD	USB ERRINT	USBINT
Reset	0	0	0	0	0	0	0	0
Access	-	-	R	R/W	R/W	R/W	R/W	R/W

Table 105: USBSTS register: bit description

Bit	Symbol	Description
31 to 16	-	reserved
15	ASS	**Asynchronous Schedule Status**: 0 = Default. The bit reports the current real status of the Asynchronous Schedule. If this bit is zero, the status of the Asynchronous Schedule is disabled. If this bit is one, the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software changes the ASE (Asynchronous Schedule Enable) bit in the USBCMD register. When this bit and the ASE (Asynchronous Schedule Enable) bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	PSSTAT	**Periodic Schedule Status**: 0 = Default. This bit reports the current status of the Periodic Schedule. If this bit is zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software changes the PSE (Periodic Schedule Enable) bit in the USBCMD register. When this bit and the PSE bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	RECL	**Reclamation**: 0 = Default. This is a read-only status bit that is used to detect an empty asynchronous schedule.
12	HCH	**HCHalted**: 1 = Default. This bit is zero when the Run/Stop bit of the USBCMD register is one. The Host Controller sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to zero, either by software or by the Host Controller hardware (for example, on an internal error).
11 to 6	-	reserved
5	IAA	**Interrupt on Asynchronous Advance**: 0 = Default. System software can force the Host Controller to issue an interrupt the next time the Host Controller advances the asynchronous schedule by writing a one to the IAAD (Interrupt on Asynchronous Advance Doorbell) bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	HSE	**Host System Error**: The Host Controller sets this bit when a serious error occurs during a host system access involving the Host Controller module. In a PCI system, conditions that set this bit include PCI Parity error, PCI Master Abort and PCI Target Abort. When this error occurs, the Host Controller clears the RS (Run/Stop) bit in the USBCMD register to prevent further execution of the scheduled TDs.

Table 105: USBSTS register: bit description…*continued*

Bit	Symbol	Description
3	FLR	**Frame List Rollover**: The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the FLS (Frame List Size) field of the USBCMD register) is 1024, the Frame Index Register rolls over every time bit 13 of the FRINDEX register toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time bit 12 of the FRINDEX register toggles.
2	PCD	**Port Change Detect**: The Host Controller sets this bit to a one when any port, where the PO (Port Owner) bit is cleared, has a change to a one or a Force Port Resume bit changes to a one as a result of a J-K transition detected on a suspended port. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that, on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the logical OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change and connect status change).
1	USBERRINT	**USB Error Interrupt**: The Host Controller sets this bit when completion of a USB transaction results in an error condition (for example, error counter underflow). If the TD (Transfer Descriptor) on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set.
0	USBINT	**USB Interrupt**: The Host Controller sets this bit on completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

11.4.3 USBINTR register (address: value read from func2 of address 10H + 14H)

The USB Interrupt Enable (USBINTR) register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USBSTS to allow the software to poll for events. The USBSTS register bit allocation is give in Table 106.

Table 106: USBINTR register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved		IAAE	HSEE	FLRE	PCIE	USBERR INTE	USBINTE
Reset	0	0	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Table 107: USBINTR register: bit description

Bit	Symbol	Description
31 to 6	-	reserved
5	IAAE	**Interrupt on Asynchronous Advance Enable**: When this bit is set and the IAA (Interrupt on Asynchronous Advance) bit in the USBSTS register is set, the Host Controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the IAA (Interrupt on Asynchronous Advance) bit.
4	HSEE	**Host System Error Enable**: When this bit is set and the Host System Error Status bit in the USBSTS register is set, the Host Controller issues an interrupt. The interrupt is acknowledged by software clearing the HSE (Host System Error) bit.
3	FLRE	**Frame List Rollover Enable**: When this bit is set and the FLR (Frame List Rollover) bit in the USBSTS register is set, the Host Controller issues an interrupt. The interrupt is acknowledged by software clearing the FLR (Frame List Rollover) bit.
2	PCIE	**Port Change Interrupt Enable**: When this bit is set and the PCD (Port Change Detect) bit in the USBSTS register is set, the Host Controller issues an interrupt. The interrupt is acknowledged by software clearing the PCD (Port Change Detect) bit.
1	USB ERRINTE	**USB Error Interrupt Enable**: When this bit is set and the USBERRINT bit in the USBSTS register is set, the Host Controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	USBINTE	**USB Interrupt Enable**: When this bit is set and the USBINT bit in the USBSTS register is set, the Host Controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

11.4.4 FRINDEX register (address: value read from func2 of address 10H + 18H)

The Frame Index (FRINDEX) register is used by the Host Controller to index into the periodic frame list. The register updates every 125 µs (once each microframe). Bits N to 3 are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the FLS (Frame List Size) field in the USBCMD register. This register must be written as a DWord. Byte writes produce undefined results. This register cannot be written unless the Host Controller is in the

halted state as indicated by the HCH (HCHalted) bit. A write to this register while the RS (Run/Stop) bit is set produces undefined results. Writes to this register also affect the SOF value. The bit allocation is given in Table 108.

Table 108: FRINDEX register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved		FRINDEX[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FRINDEX[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109: FRINDEX register: bit description

Bit	Symbol	Description
31 to 14	-	reserved
13 to 0	FRINDEX [13:0]	**Frame Index**: Bits in this register are used for the frame number in the SOF packet and as the index into the Frame List. The value in this register increments at the end of each time frame (for example, microframe). The bits used for the frame number in the SOF token are taken from bits 13 to 3 of this register. Bits N to 3 are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or microframes) before moving to the next index. The following illustrates values of N based on the value of the FLS (Frame List Size) field in the USBCMD register.

USBCMD [Frame List Size]	Number Elements	N
00B	(1024)	12
01B	(512)	11
10B	(256)	10
11B	(reserved)	-

11.4.5 CTRLDSSEGMENT register (address: value read from func2 of address 10H + 1CH)

The Control Data Structure Segment (CTRLDSSEGMENT) register corresponds to the most significant address bits (bits 63 to 32) for all EHCI data structures. If the 64AC (64-bit Addressing Capability) field in HCCPARAMS is cleared, then this register is not used and software cannot write to it (reading from this register returns zero).

If the 64AC (64-bit Addressing Capability) field in HCCPARAMS is set, this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address.

This register allows the host software to locate all control data structures within the same 4 Gigabyte memory segment.

11.4.6 PERIODICLISTBASE register (address: value read from func2 of address 10H + 20H)

The Periodic Frame List Base Address (PERIODLISTBASE) register contains the beginning address of the Periodic Frame List in the system memory. If the Host Controller is in the 64-bit mode (as indicated by a one in the 64AC (64-bit Addressing Capability) field in the HCCSPARAMS register), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4 kbyte aligned. The contents of this register are combined with the FRINDEX register to enable the Host Controller to step through the Periodic Frame List in sequence. The bit allocation is given in Table 110.

Table 110: PERIODICLISTBASE register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	BA[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BA[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BA[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Table 111: PERIODICLISTBASE register: bit description

Bit	Symbol	Description
31 to 12	BA[19:0]	**Base Address**: These bits correspond to memory address signals 31 to 12, respectively.
11 to 0	-	reserved

11.4.7 ASYNCLISTADDR register (address: value read from func2 of address 10H + 24H)

This 32-bit register (bit allocation: Table 112) contains the address of the next asynchronous queue head to be executed. If the Host Controller is in 64-bit mode (as indicated by a one in 64AC (64-bit Addressing Capability) field in the HCCPARAMS register), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. Bits 4 to 0 of this register always return zeros when read. The memory structure referenced by the physical memory pointer is assumed to be 32-byte (cache aligned).

Table 112: ASYNCLISTADDR register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	LPL[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	LPL[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	LPL[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Table 113: ASYNCLISTADDR register: bit description

Bit	Symbol	Description
31 to 12	LPL[19:0]	**Link Pointer List**: These bits correspond to memory address signals 31 to 12, respectively. This field may only reference a Queue Head (QH).
11 to 0	-	reserved

11.4.8 CONFIGFLAG register (address: value read from func2 of address 10H + 5CH)

The bit allocation of the Configure Flag (CONFIGFLAG) register is given in Table 114.

Table 114: CONFIGFLAG register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							CF
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	R/W

Table 115: CONFIGFLAG register: bit description

Bit	Symbol	Description
31 to 1	-	reserved
0	CF	**Configure Flag**: The host software sets this bit as the last action in its process of configuring the HC. This bit controls the default port-routing control logic. **0 —** Port routing control logic default-routes each port to an implementation dependent classic HC **1 —** Port routing control logic default-routes all ports to this HC

11.4.9 PORTSC registers 1, 2, 3, 4 (address: value read from func2 of address 10H + 50H + (4 x Port Number − 1)) where Port Number is 1, 2, 3,...N_Ports

The Port Status and Control (PORTSC) register (bit allocation: Table 116) is in the auxiliary power well. It is only reset by hardware when the auxiliary power is initially applied or in response to a Host Controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

If the port has power control, software cannot change the state of the port until it sets the port power bits. Software must not attempt to change the state of the port until the power is stable on the port (max. delay is 20 ms from the transition).

Table 116: PORTSC 1, 2, 3, 4 register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	-	-	-	-	-	-	-	-

Bit	23	22	21	20	19	18	17	16
Symbol	reserved	WKOC_E	WKDS CNNT_E	WKCNNT_ E	PTC[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	PIC[1:0]		PO	PP	LS[1:0]		reserved	PR
Reset	0	0	1	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	-	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SUSP	FPR	OCC	OCA	PEDC	PED	ECSC	ECCS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R/W	R/W	R/W	R

Table 117: PORTSC 1, 2, 3, 4 register: bit description

Bit	Symbol	Description
31 to 23	-	reserved
22	WKOC_E	**Wake on Overcurrent Enable**: Default = 0. Setting this bit enables the port to be sensitive to overcurrent conditions as wake-up events.[1]
21	WKDS CNNT_E	**Wake on Disconnect Enable**: Default = 0. Setting this bit enables the port to be sensitive to device disconnects as wake-up events.[1]
20	WKCNNT _E	**Wake on Connect Enable**: Default = 0. Setting this bit enables the port to be sensitive to device connects as wake-up events.[1]
19 to 16	PTC[3:0]	**Port Test Contro**l: Default = 0000B. When this field is zero, the port is not operating in a test mode. A non-zero value indicates that it is operating in test mode and the test mode is indicated by the value. The encoding of the test mode bits are (0110B to 1111B are reserved): **0000B —** test mode disabled **0001B —** test J_STATE **0010B —** test K_STATE **0011B —** test SE0_NAK **0100B —** test Packet **0101B —** test FORCE_ENABLE
15 to 14	PIC[1:0]	**Port Indicator Control**. Default = 0. Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If P_INDICATOR bit is a one, then the bit encoding is: **00B —** Port indicators are OFF **01B —** amber **10B —** green **11B —** undefined Refer to the *Universal Serial Bus Specification Rev. 2.0* for a description on how these bits are implemented. [1]

Table 117: PORTSC 1, 2, 3, 4 register: bit description...*continued*

Bit	Symbol	Description
13	PO	**Port Owner**: Default = 1. This bit unconditionally goes to a 0 when the Configured bit in the CONFIGFLAG register makes a 0 to 1 transition. This bit unconditionally goes to 1 whenever the Configured bit is zero. System software uses this field to release ownership of the port to a selected Host Controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion Host Controller owns and controls the port.
12	PP	**Port Power**: The function of this bit depends on the value of the Port Power Control (PPC) field in the HCSPARAMS register. **If PPC = 0 and PP = 1 —** The Host Controller does not have port power control switches. Each port is hardwired to power. **If PPC = 1 and PP = 1 or 0 —** The Host Controller has port power control switches. This bit represents the current setting of the switch (logic 0 = OFF, logic 1 = ON). When PP is logic 0, the port is non-functional and will not report any status When an overcurrent condition is detected on a powered port and PPC is a logic 1, the PP bit in each affected port may be changed by the Host Controller from a logic 1 to a logic 0 (removing power from the port).
11 to 10	LS[1:0]	**Line Status**: This field reflect the current logical levels of the DP (bit 11) and DM (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the Port Enable bit is zero and the current connect status bit is set to one. **00B —** SE0: Not low-speed device, perform EHCI reset **01B —** J-state: Not low-speed device, perform EHCI reset **10B —** K-state: Low-speed device, release ownership of port **11B —** undefined: Not low-speed device, perform EHCI reset. If Port Power (PP) is zero, this field is undefined.
9	-	reserved

Table 117: PORTSC 1, 2, 3, 4 register: bit description...*continued*

Bit	Symbol	Description
8	PR	**Port Reset**: logic 1 means the Port is in Reset. A logic 0 means the Port is not in Reset. Default = 0. When software sets this bit (from a logic 0), the bus reset sequence as defined in the *Universal Serial Bus Specification Rev. 2.0* is started. Software clears this bit to terminate the bus reset sequence. Software must hold this bit at logic 1 until the reset sequence, as specified in the *Universal Serial Bus Specification Rev. 2.0*, is completed. **Remark:** When software sets this bit, it must also clear the Port Enable bit. **Remark:** When software clears this bit, there may be a delay before the bit status changes to logic 0, because it will not read Logic 0 until the reset is completed. If the port is in the high-speed mode after reset is completed, the Host Controller will automatically enable this port (it can set the Port Enable bit). A Host Controller must terminate the reset and stabilize the state of the port within 2 ms of software changing this bit from a logic 1 to a logic 0. For example, if the port detects that the attached device is high-speed during a reset, then the Host Controller must enable the port within 2 ms of software clearing this bit. The HCH (HCHalted) bit in the USBSTS register must be a logic 0 before software attempts to use this bit. The Host Controller may hold Port Reset asserted when the HCH (HCHalted) bit is set.[1]
7	SUSP	**Suspend**: Default = 0. A logic 1 means the Port is in the suspend state. A logic 0 means the Port is not suspended. The Port Enabled bit and the Suspend bit of this register define the port states as follows: **PED = 0 and SUSP = x —** port is disabled **PED = 1 and SUSP = 0 —** port is enabled **PED = 1 and SUSP = 1 —** port is suspended When in the suspend state, downstream propagation of data is blocked on this port, except for the port reset. If a transaction was in progress when this bit was set, he blocking occurs at the end of the current transaction. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. Attempts to clear this bit are ignored by the Host Controller. The Host Controller will unconditionally set this bit to a logic 0 when: • Software changes the FPR (Force Port Resume) bit to logic 0. • Software changes the PR (Port Reset) bit to logic 1. If the host software sets this bit when the Port Enabled bit is a logic 0, the results are undefined.[1]

Table 117: PORTSC 1, 2, 3, 4 register: bit description...*continued*

Bit	Symbol	Description
6	FPR	**Force Port Resume**: A logic 1 means Resume detected or driven on the port. A logic 0 means no resume (K-state) detected or driven on the port. Default = 0. Software sets this bit to drive the resume signaling. The Host Controller sets this bit if a J-to-K transition is detected while the port is in the suspend state. When this bit changes to a logic 1 because a J-to-K transition is detected, the PCD (Port Change Detect) bit in the USBSTS register is also set to a logic 1. If software sets this bit to a logic 1, the Host Controller must not set the PCD (Port Change Detect) bit. Note that when the EHCI controller owns the port, the resume sequence follows the sequence documented in the *USB Specification Rev. 2.0*. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set. Software must time the Resume and clear this bit after the correct amount of time has elapsed. Clearing this bit causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain at one until the port has switched to the high-speed idle. The Host Controller must complete this transition within 2 ms of software clearing this bit. [1]
5	OCC	**Overcurrent Change**: Default = 0. This bit is set to a logic 1 when there is a change in overcurrent active. Software clears this bit by setting this bit to a one.
4	OCA	**Overcurrent Active**: Default = 0. If set to logic 1, this port has an overcurrent condition. If set to logic 0, this port does not have an overcurrent condition. This bit will automatically change from a logic 1 to a logic 0 when the overcurrent condition is removed.
3	PEDC	**Port Enable/Disable Change**: A logic 1 means the Port enabled/disabled status has changed. A logic 0 means no change. Default = 0. For the root hub, this bit gets set only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the *USB Specification Rev. 2.0* for the definition of a Port Error). Software clears this bit by setting it. [1]

Table 117: PORTSC 1, 2, 3, 4 register: bit description...*continued*

Bit	Symbol	Description
2	PED	**Port Enabled/Disabled**: A logic 1 means enable. A logic 0 means disable. Default = 0. Ports can only be enabled by the Host Controller as a part of the reset and enable sequence. Software cannot enable a port by writing a logic 1 to this field. The Host Controller will only set this bit when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition or by host software. Note that the bit status does not change until the port state has actually changed. There may be a delay in disabling or enabling a port due to other Host Controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port, except for reset. [1]
1	ECSC	**Connect Status Change**: A logic 1 means Change in ECCS (Current Connect Status). A logic 0 means no change. Default = 0. This bit indicates a change has occurred in the port's ECCS (Current Connect Status). The Host Controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (that is, the bit will remain set). Software clears this bit setting it. [1]
0	ECCS	**Current Connect Status**: logic 1 indicates a device is present on port. logic 0 indicates no device is present. Default = 0. This value reflects the current state of the port and may not correspond directly to the event that caused the ECSC (Connect Status Change) bit to be set. [1]

[1] These fields read logic 0, if the Port Power (PP) (bit 12 in register PORTSC 1,2,3,4) is logic 0.

12. Power consumption

Table 118 shows the power consumption when two ports are active, that is, the SEL2PORTS pin is connected to V_{DD}.

Table 118: Power consumption when SEL2PORTS is HIGH

Power pins group	Conditions	Typ	Unit
total power $V_{AUX} + AV_{AUX} + AV_{AUX\_PLL} + V_{DD}$	no devices connected to the ISP1561[1]	151	mA
	one high-speed device connected to the ISP1561	181	mA
	two high-speed devices connected to the ISP1561	209	mA
auxiliary power $V_{AUX} + AV_{AUX} + AV_{AUX\_PLL}$	no devices connected to the ISP1561[1]	98	mA
	one high-speed device connected to the ISP1561	124	mA
	two high-speed devices connected to the ISP1561	153	mA
V_{DD}	no devices connected to the ISP1561[1]	53	mA
	one high-speed device connected to the ISP1561	56	mA
	two high-speed devices connected to the ISP1561	56	mA

[1] When one or two full-speed or low-speed power devices are connected, the power consumption is comparable with the power consumption when no high-speed devices are connected (there is a difference of approximately 1 mA).

Table 119 shows the power consumption when four ports are active, that is, the SEL2PORTS pin is connected to ground.

Table 119: Power consumption when SEL2PORTS is LOW

Power pins group	Conditions	Typ	Unit
total power $V_{AUX} + AV_{AUX} + AV_{AUX\_PLL} + V_{DD}$	no devices connected to the ISP1561[1]	207	mA
	one high-speed device connected to the ISP1561	236	mA
	two high-speed devices connected to the ISP1561	261	mA
	three high-speed devices connected to the ISP1561	288	mA
	four high-speed devices connected to the ISP1561	314	mA
auxiliary power $V_{AUX} + AV_{AUX} + AV_{AUX\_PLL}$	no devices connected to the ISP1561[1]	151	mA
	one high-speed device connected to the ISP1561	178	mA
	two high-speed devices connected to the ISP1561	206	mA
	three high-speed devices connected to the ISP1561	232	mA
	four high-speed devices connected to the ISP1561	259	mA
AV_{AUX}	no devices connected to the ISP1561[1]	7	mA
	one high-speed device connected to the ISP1561	33	mA
	two high-speed devices connected to the ISP1561	58	mA
	three high-speed devices connected to the ISP1561	84	mA
	four high-speed devices connected to the ISP1561	108	mA
AV_{AUX_PLL}	no devices connected to the ISP1561	3	mA
	one high-speed device connected to the ISP1561	3	mA
	two high-speed devices connected to the ISP1561	3	mA
	three high-speed devices connected to the ISP1561	3	mA
	four high-speed devices connected to the ISP1561	3	mA

Table 119: Power consumption when SEL2PORTS is LOW *...continued*

Power pins group	Conditions	Typ	Unit
V_{DD}	no devices connected to the ISP1561	56	mA
	one high-speed device connected to the ISP1561	57	mA
	two high-speed devices connected to the ISP1561	57	mA
	three high-speed devices connected to the ISP1561	57	mA
	four high-speed devices connected to the ISP1561	57	mA

[1] When one to four full-speed or low-speed power devices are connected, the power consumption is comparable with the power consumption when no high-speed devices are connected (there is a difference of only about 3 mA).

Table 120: Power consumption: S1 and S3

Power state	Typ	Unit
S1	130	mA
S3	1.5[1]	mA
	0.52[2]	mA

[1] When I^2C-bus and legacy support are present.

[2] When I^2C-bus and legacy support are not present.

13. Limiting values

Table 121: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+4.6	V
V_{AUX}	auxiliary voltage		–0.5	+4.6	V
AV_{AUX}	analog auxiliary voltage (3.3 V); supply voltage		–0.5	+4.6	V
AV_{AUX_PLL}	analog auxiliary voltage (3.3 V); supply voltage for PLL		–0.5	+4.6	V
$V_{I(5V)}$	input voltage on 5 V buffers	3.0 V < V_{DD} < 3.6 V [1]	–0.5	+6.0	V
$V_{I(3.3V)}$	input voltage on 3.3 V buffers	3.0 V < V_{DD} < 3.6 V	–0.5	+4.6	V
I_{lu}	latch-up current	V_I < 0 or V_I > V_{CC}	-	100	mA
V_{esd}	electrostatic discharge voltage	all pins (I_{LI} < 1 μA)	–1000	+1000	V
		on pins DM1 to DM4, DP1 to DP4, and all GND pins (I_{LI} < 1 μA) [2]	–4000	+4000	V
T_{stg}	storage temperature		–40	+125	°C

[1] Valid only when the supply voltage is present

[2] Test method available on request.

14. Recommended operating conditions

Table 122: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_{AUX}	auxiliary voltage		3.0	3.3	3.6	V
AV_{AUX}	analog auxiliary voltage (3.3 V); supply voltage		3.0	3.3	3.6	V
AV_{AUX_PLL}	analog auxiliary voltage (3.3 V); supply voltage for PLL		3.0	3.3	3.6	V
$V_{I(5V)}$	input voltage on 5 V buffers	[1]	0	-	5.5	V
$V_{I(3.3V)}$	input voltage on 3.3 V buffers		0	-	V_{DD}	V
T_{amb}	operating temperature		–40	-	+85	°C

[1] Valid only when the supply voltage is present

15. Static characteristics

Table 123: Static characteristics: analog I/O pins (SDA and SCL)

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.1	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.9	V
V_{hys}	hysteresis voltage		0.15	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V

Table 124: Static characteristics: digital pins[1]

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage		2.4	-	-	V

[1] All pins are 5 V tolerant.

Table 125: Static characteristics: PCI interface block[1]

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
V_{IL}	LOW-level input voltage		0	-	0.9	V
V_{IPU}	input pull-up voltage		2.1	-	-	V
I_{IL}	input leakage current	$0 < V_{IN} < V_{DD}$	–10	-	+10	µA
V_{OH}	HIGH-level output voltage	I_{OUT} = 500 µA	2.7	-	-	V
V_{OL}	LOW-level output voltage	I_{OUT} = 1500 µA	-	-	0.3	V
C_{IN}	input pin capacitance		-	-	10	pF
C_{CLK}	CLK pin capacitance		5	-	12	pF
C_{IDSEL}	IDSEL pin capacitance		-	-	8	pF

[1] All pins are 5 V tolerant.

Table 126: Static characteristics: USB interface block (pins DM1 to DM4 and DP1 to DP4)

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels for high-speed						
V_{HSSQ}	squelch detection threshold (differential signal amplitude)	squelch detected	-	-	100	mV
		no squelch detected	150	-	-	mV

Table 126: Static characteristics: USB interface block (pins DM1 to DM4 and DP1 to DP4) *...continued*

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSDSC}	disconnect detection threshold (differential signal amplitude)	disconnect detected	625	-	-	mV
		disconnect not detected	-	-	525	mV
V_{HSCM}	data signaling common mode voltage range		–50	-	+500	mV
Output levels for high-speed						
V_{HSOI}	idle state		–10	-	+10	mV
V_{HSOH}	data signaling HIGH		360	-	440	mV
V_{HSOL}	data signaling LOW		–10	-	+10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700[1]	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		–900[1]	-	–500	mV
Input levels for full-speed and low-speed						
V_{IH}	HIGH-level input voltage (drive)		2.0	-	-	V
V_{IHZ}	HIGH-level input voltage (floating)		2.7	-	3.6	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{DI}	differential input sensitivity	$\lvert V_{DP} - V_{DM} \rvert$	0.2	-	-	V
V_{CM}	differential common mode range		0.8	-	2.5	V
Output levels for full-speed and low-speed						
V_{OH}	HIGH-level output voltage		2.8	-	3.6	V
V_{OL}	LOW-level output voltage		0	-	0.3	V
V_{OSEI}	SEI		0.8	-	-	V
V_{CRS}	output signal crossover point voltage		1.3	-	2.0	V

[1] HS termination resistor disabled, pull-up resistor connected. Only during reset, when both hub and device are capable of high-speed operation.

16. Dynamic characteristics

Table 127: Dynamic characteristics: system clock timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal oscillator						
f_{clk}	clock frequency[1]	crystal[2]	-	12	-	MHz
		oscillator	-	48	-	MHz
External clock input						
δ	clock duty cycle		-	50	-	%

[1] Recommended accuracy of the clock frequency is 500 ppm for the crystal and oscillator. The oscillator should have 3.3 V power supply.

[2] Suggested values for external capacitors when using a crystal are 22 to 27 pF.

Table 128: Dynamic characteristics: analog I/O pins (SDA and SCL)[1]

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	output fall time V_{IH} to V_{IL}	$10 < C_B < 400$[2]	-	0	250	ns

[1] All pins are 5 V tolerant.

[2] The bus capacitance (C_B) is specified in pF. To meet the specification for V_{OL} and the maximum rise time (300 ns), use an external pull-up resistor with $R_{max} = 850/C_B$ kΩ and $R_{min} = (V_{DD} - 0.4)/3$ kΩ.

Table 129: Dynamic characteristics: PCI interface block[1]

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SR	output slew rate (rise, fall)	standard load[2]	1	-	4	V/ns

[1] All pins are 5 V tolerant.

[2] Standard load is 10 pF together with a pull-up and pull-down resistor of 10 kΩ.

Table 130: Dynamic characteristics: high-speed source electrical characteristics

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{HSR}	high-speed differential rise time	10% to 90%	500	-	-	ps
t_{HSF}	high-speed differential fall time	90% to 10%	500	-	-	ps
Z_{HSDRV}	drive output resistance (this also serves as a high-speed termination)	includes the R_S resistor	40.5	45	49.5	Ω
Clock timing						
t_{HSDRAT}	data rate		479.76	-	480.24	Mb/s
t_{HSFRAM}	microframe interval		124.9375	-	125.0625	µs
t_{HSRFI}	consecutive microframe interval difference		1	-	four high-speed bit times	ns

Table 131: Dynamic characteristics: full-speed source electrical characteristics

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10% to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90% to 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching		90	-	111.1	%
Z_{DRV}	driver output resistance for the driver that is not high-speed capable		28	-	44	Ω
Data timing: see Figure 8						
t_{FDEOP}	source jitter for differential transition to SEO transition	full-speed timing	–2	-	5	ns
t_{FEOPT}	source SE0 interval of EOP		160	-	175	ns
t_{FEOPR}	receiver SE0 interval of EOP		82	-	-	ns
t_{LDEOP}	source jitter for differential transition to SEO transition	low-speed timing	–40	-	100	ns
t_{LEOPT}	source SE0 interval of EOP		1.25	-	1.5	µs
t_{LEOPR}	receiver SE0 interval of EOP		670	-	-	ns
t_{FST}	width of SE0 interval during the differential transaction		-	-	14	ns

Table 132: Dynamic characteristics: low-speed source electrical characteristics

V_{DD} = 3.0 to 3.6 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{LR}	rise time		75	-	300	ns
t_{LF}	fall time		75	-	300	ns
t_{LRFM}	differential rise and fall time matching		90	-	125	%

17. Timing

Table 133: PCI clock and IO timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PCI clock timing; see Figure 5						
T_{cyc}	CLK cycle time		30	-	-	ns
t_{high}	CLK HIGH time		11	-	-	ns
t_{low}	CLK LOW time		11	-	-	ns
SR_{CLK}	CLK slew rate		1	-	4	V/ns
$SR_{RST\#}$	RST# slew rate		50	-	-	mV/ns
PCI input timing; see Figure 6						
t_{su}	input setup time to CLK (bus signal)		7	-	-	ns
$t_{su(ptp)}$	input setup time to CLK (point-to-point)[1]		10	-	-	ns
t_h	input hold time for CLK		10	-	-	ns
PCI output timing; see Figure 7						
t_{val}	CLK to signal valid delay (bus signal)		2	-	11	ns
$t_{val(ptp)}$	CLK to signal valid delay (point-to-point)[1]		2	-	12	ns
t_{on}	float to active delay		2	-	-	ns
t_{off}	active to float delay		-	-	28	ns
PCI reset timing						
$t_{rst-clk}$	reset active time after CLK stable		100	-	-	µs
t_{rst}	reset active time after CLK stable		1	-	-	ms

[1] REQ# and GNT# are point-to-point signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All others are bus signals.

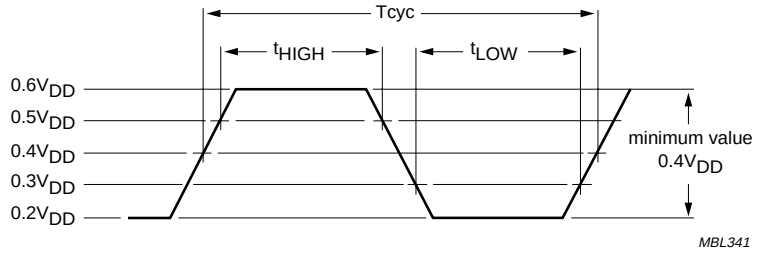


Fig 5. PCI clock.

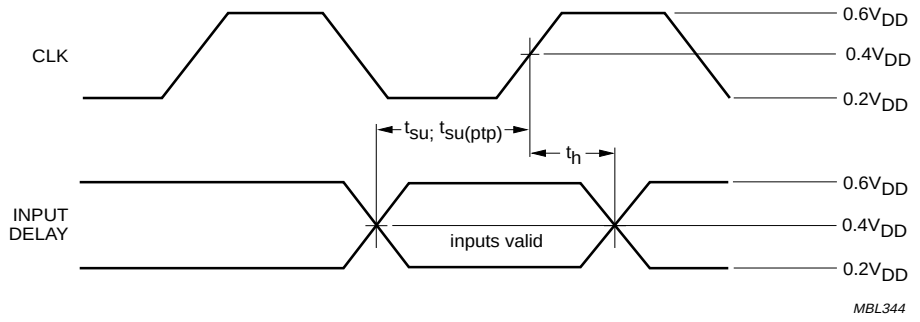


Fig 6. PCI input timing.

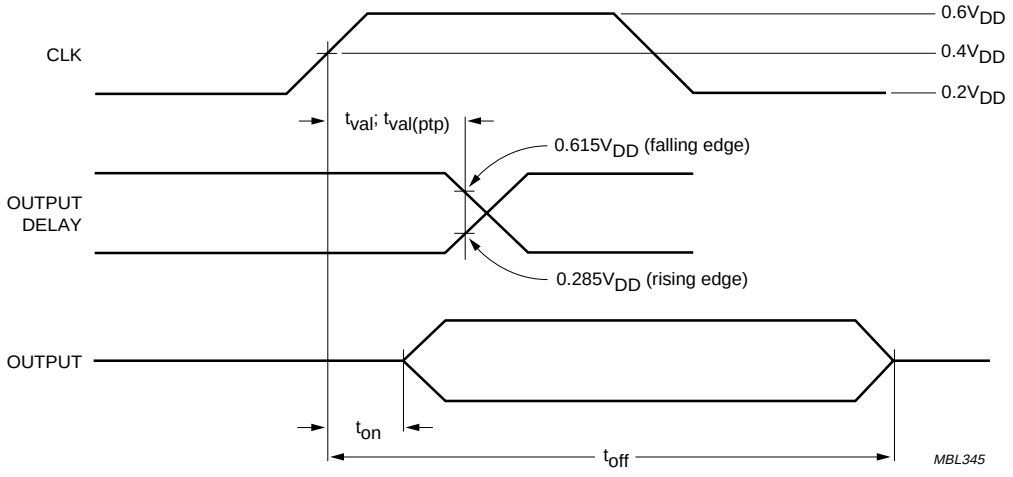
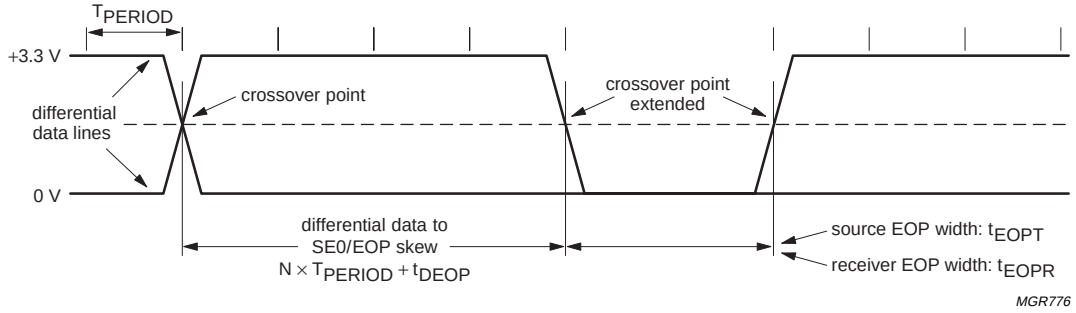


Fig 7. PCI output timing.



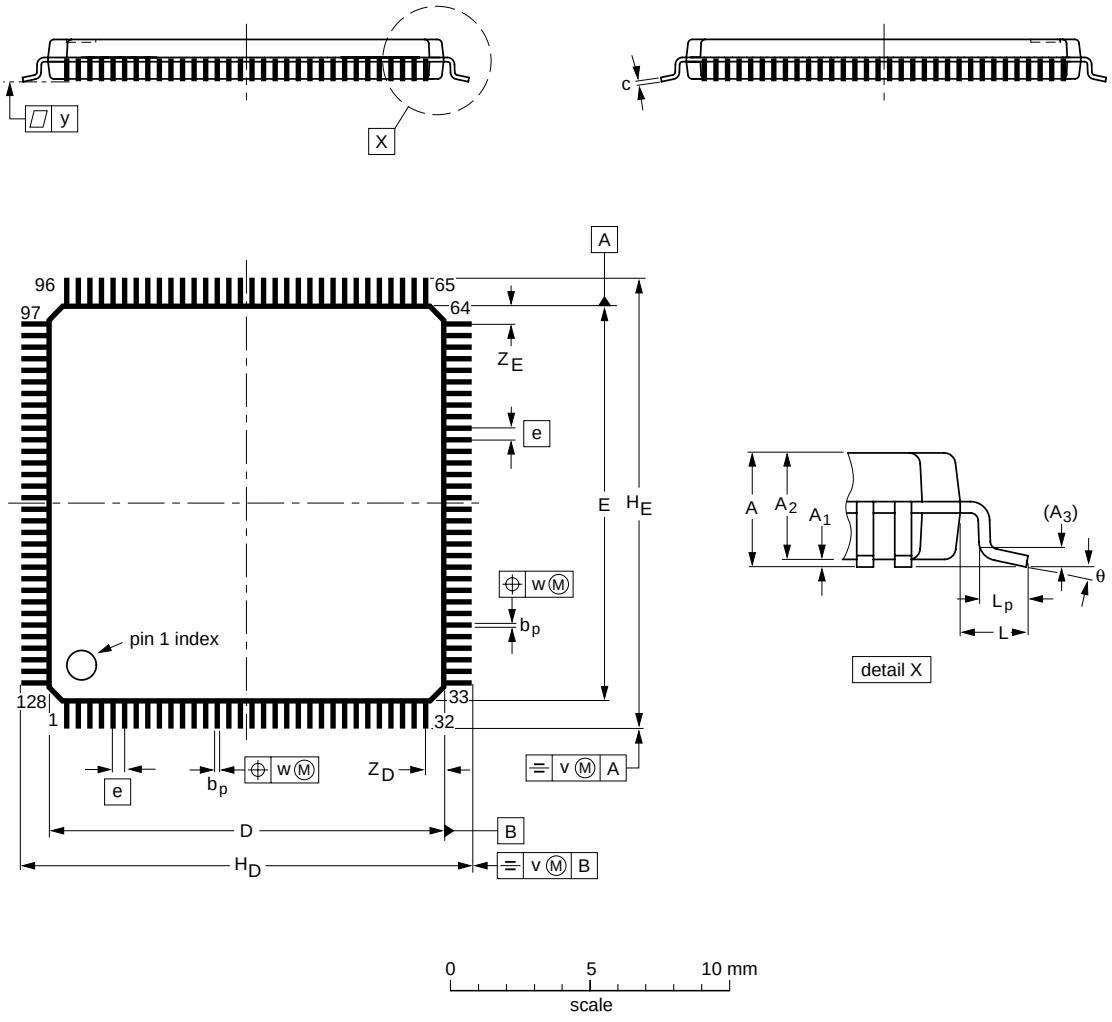
T_{PERIOD} is the bit duration corresponding with the USB data rate.

Full-speed timing symbols have a subscript prefix ‘F’, low-speed timings a prefix ‘L’.

Fig 8. USB source differential data-to-EOP transition skew and EOP width.

18. Package outline

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 14 x 1.4 mm **SOT420-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	14.1 13.9	14.1 13.9	0.4	16.15 15.85	16.15 15.85	1.0	0.75 0.45	0.2	0.07	0.08	0.95 0.65	0.95 0.65	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT420-1		MS-026				~~97-08-14~~ 99-11-03

Fig 9. LQFP128 package outline.

19. Soldering

19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19.5 Package related soldering information

Table 134: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

20. Revision history

Table 135: Revision history

Rev	Date	CPCN	Description
01	20030206		Product data (9397 75010015)

21. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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