

3875081 G E SOLID STATE

01E 11027 D

T-37-25

IT100, IT101 P-Channel JFET Switch

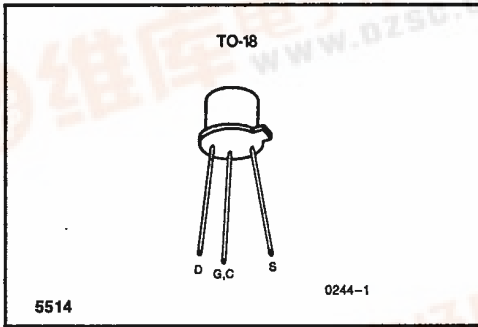


IT100, IT101

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with TTL logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of $\pm 15V$ can be switched. The FET is OFF for hi level inputs ($+5V$ or $+15V$) and ON for low level inputs ($<0.5 V$ for IT100, $<1.5V$ for IT101).

PIN CONFIGURATION



FEATURES

- Interfaces Directly w/TTL Logic Elements
- $r_{DS(on)} < 75\Omega$ for 5V Logic Drive
- $I_{D(off)} < 100pA$

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise noted)

Gate-Source Voltage	35V
Gate-Drain Voltage	35V
Gate Current	50mA
Storage Temperature Range	$-65^\circ C$ to $+200^\circ C$
Operating Temperature Range	$-55^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10sec)	$+300^\circ C$
Power Dissipation	300mW
Derate above $25^\circ C$	$2.4mW/^\circ C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
IT100
IT101

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT100		IT101		Units
			Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = 20V, V_{DS} = 0$		200		200	pA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu A, V_{DS} = 0$	35		35		V
V_P	Pinch Off Voltage	$I_D = 1nA, V_{DS} = -15V$	2	4.5	4	10	
I_{DSS}	Drain Current	$V_{GS} = 0, V_{DS} = -15V$	-10		-20		mA
g_{fs}	Transconductance	$V_{GS} = 0, V_{DS} = -15V$	8		8		mS
g_{os}	Output Conductance			1		1	
$I_{D(off)}$	Drain (OFF) Leakage	$V_{DS} = -10V, V_{GS} = 15V$		-100		-100	pA
$r_{DS(on)}$	Drain-Source "ON" Resistance	$V_{GS} = 0, V_{DS} = -0.1V$		75		60	Ω
C_{iss}	Input Capacitance	$V_{DG} = -20V, V_{GS} = 0$ (Note 1)		35		35	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DG} = -10V, I_S = 0$ (Note 1)		12		12	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

