IXYS

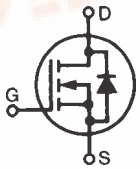
Advance Technical Information

PolarHT™ HiPerFET Power MOSFET

IXFC52N30P

V_{DSS} = 300 V
I_{D25} = 32 A
$R_{DS(on)}$ = 75 mΩ

N-Channel Enhancement Mode

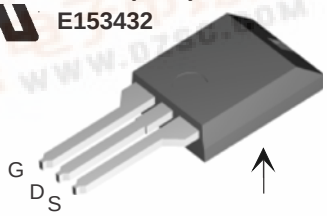


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	300	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	300	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	32	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	150	A
I_{AR}	T_C = 25°C	52	A
E_{AR}	T_C = 25°C	30	mJ
E_{AS}	T_C = 25°C	1.0	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 4 Ω	10	V/ns
P_D	T_C = 25°C	100	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, t = 1minute, leads-to-tab	2500	V~
F_C	Mounting Force	11..65/2.5..15	N/lb
Weight	ISOPLUS220	2.0	g

Symbol (T_J = 25°C, unless otherwise specified)	Test Conditions	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 µA	300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	µA
	T_J = 125°C			250	µA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5\ I_{D25}$, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %		65	75	mΩ

ISOPLUS220™(IXFC)

E153432



G = Gate D = Drain
S = Source TAB = Drain

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<30pF)

Advantages

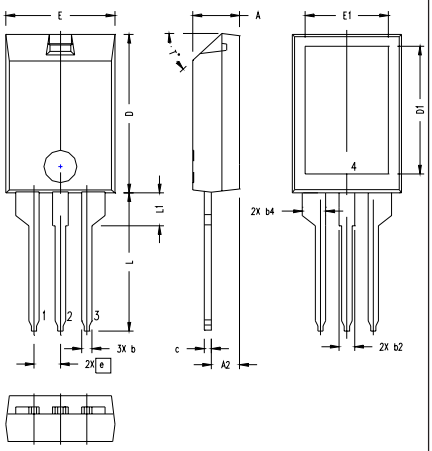
- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25}, pulse test	20	30		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3490		pF
C_{oss}			550		pF
C_{rss}			130		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_{D25} R_G = 4 Ω (External)		24		ns
t_r			22		ns
$t_{d(off)}$			60		ns
t_f			20		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		110		nC
Q_{gs}			25		nC
Q_{gd}			53		nC
R_{thJC}				1.25	K/W
R_{thCK}			0.21		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values min.	typ.	max.	
I_S	V_{GS} = 0 V			32	A
I_{SM}	Repetitive			150	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.5	V
T_{rr}	I_F = 25A -di/dt = 100 A/µs		250		ns
Q_{RM}	V_R = 100V		1.0		µC

ISOPLUS220 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T°			42.5°	47.5°

NOTE:
1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
2. This drawing will meet dimensional requirement of JEDEC SS Product Outl TO-273 except D and D1 dimension.

Fig. 1. Output Characteristics @ 25 Deg. C

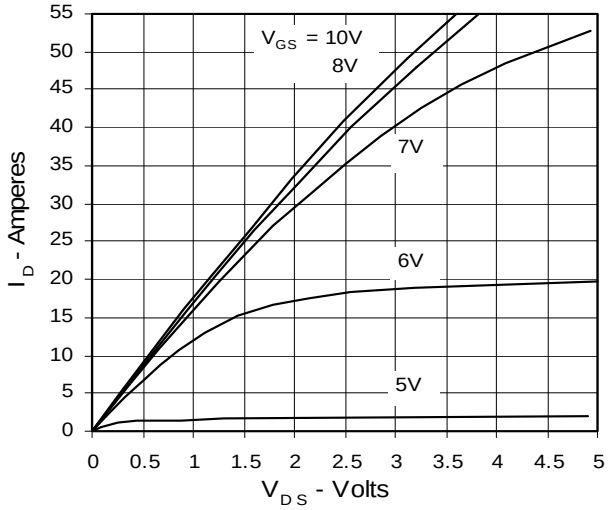


Fig. 2. Extended Output Characteristics @ 25 deg. C

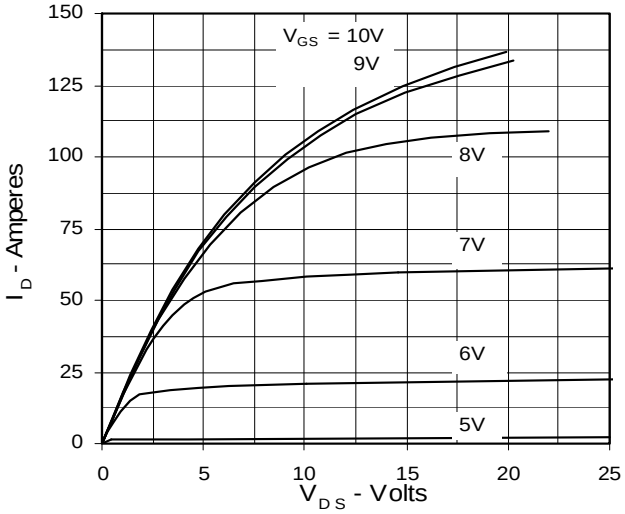


Fig. 3. Output Characteristics @ 125 Deg. C

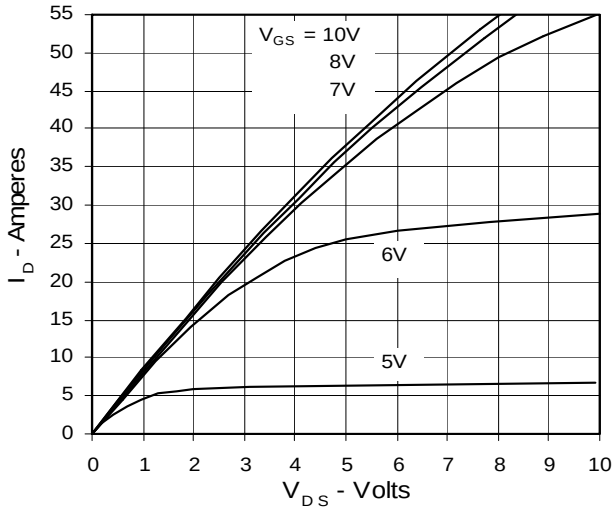


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

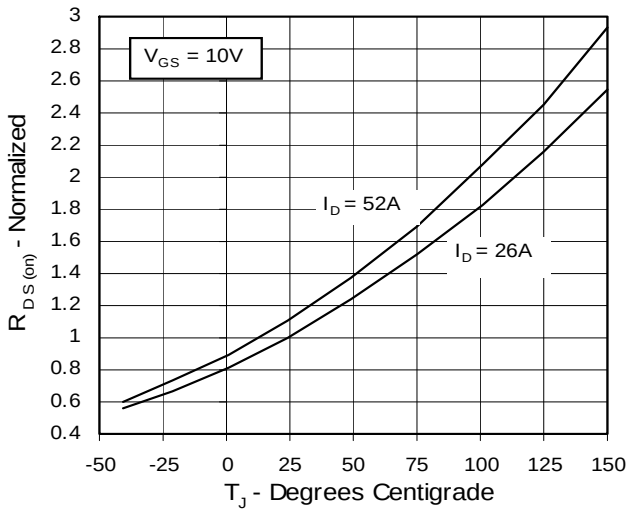


Fig. 5. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

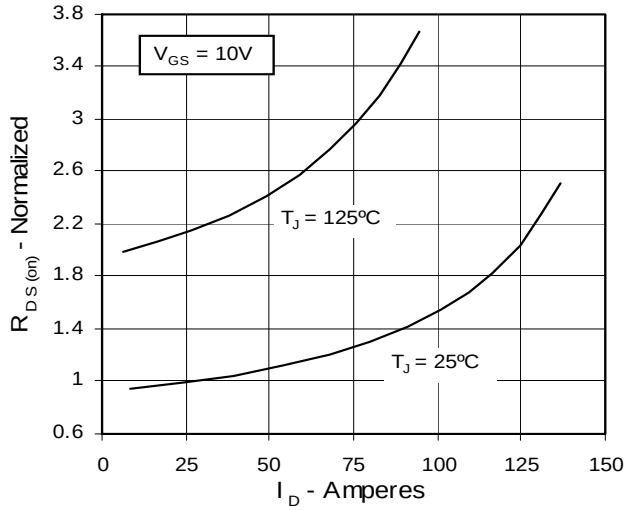


Fig. 6. Drain Current vs. Case Temperature

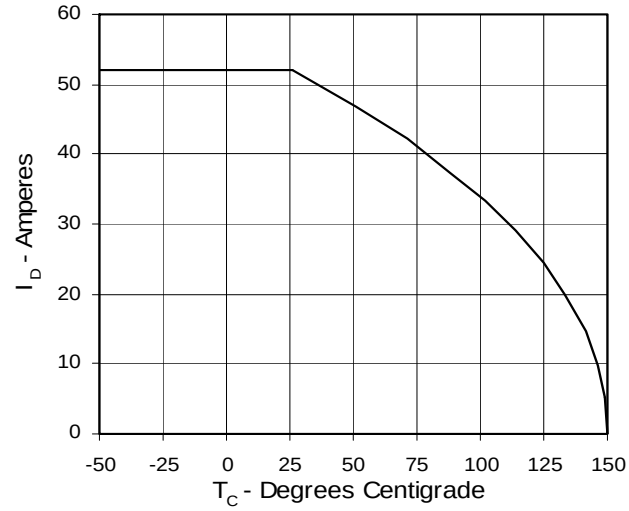


Fig. 7. Input Admittance

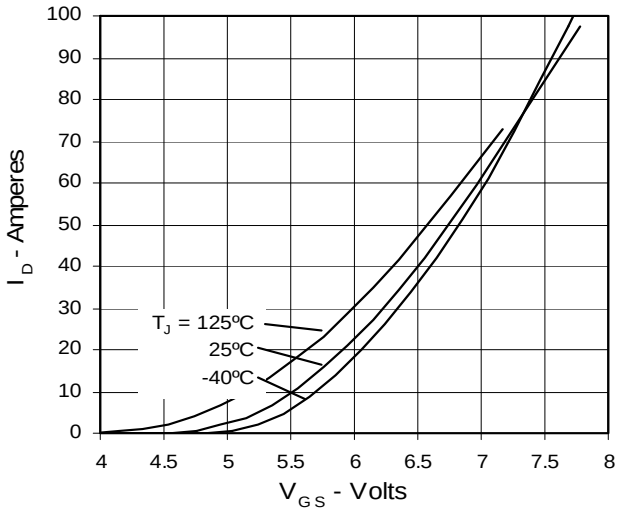


Fig. 8. Transconductance

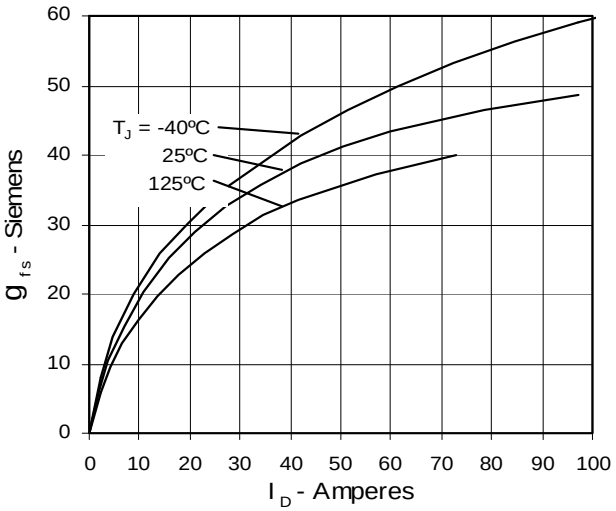


Fig. 9. Source Current vs. Source-To-Drain Voltage

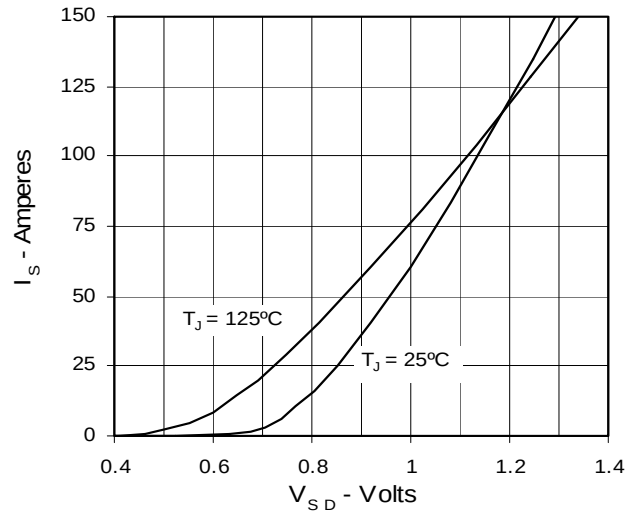


Fig. 10. Gate Charge

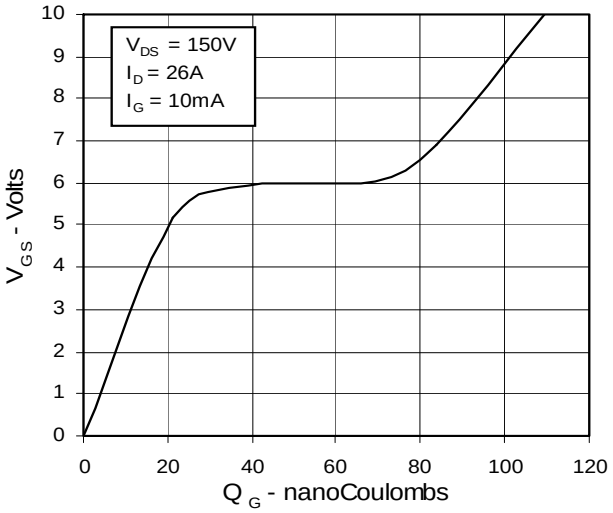


Fig. 11. Capacitance

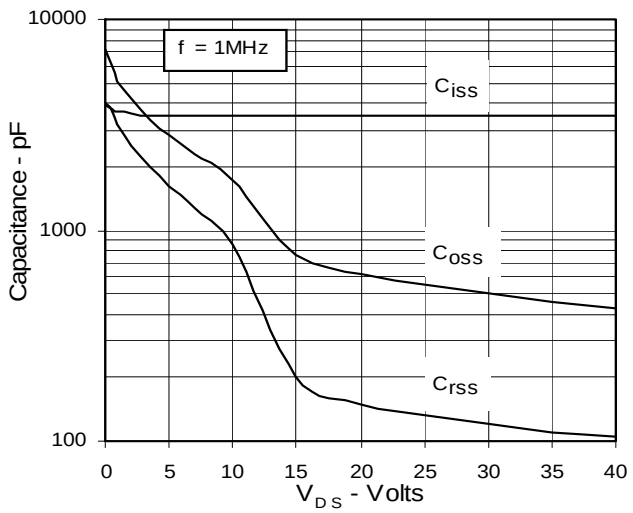


Fig. 12. Forward-Bias Safe Operating Area

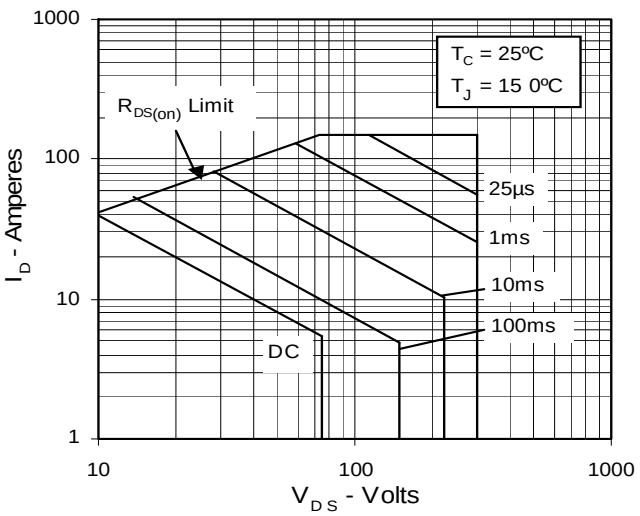


Fig. 6. Drain Current vs. Case Temperature

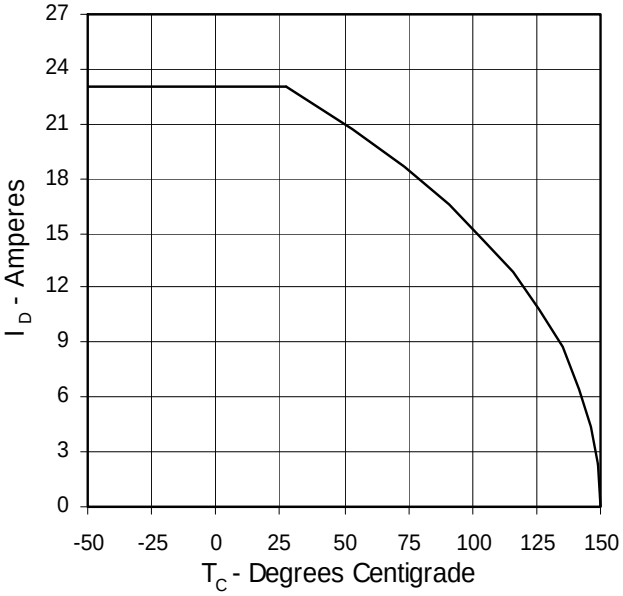


Fig. 12. Forward-Bias Safe Operating Area

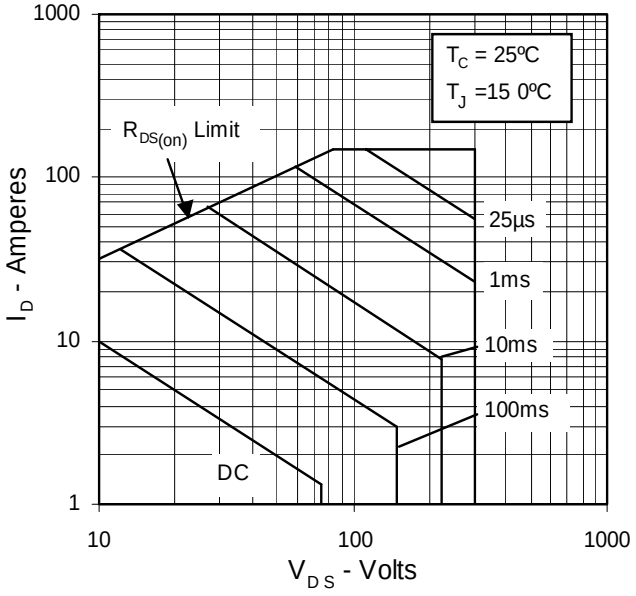


Fig. 13. Maximum Transient Thermal Resistance