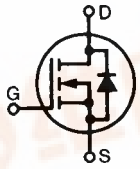
IXYS

MegaMOS™FET

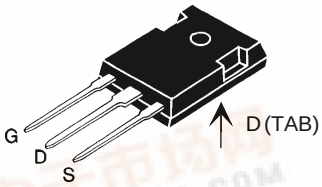
	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXTH 35N30	300 V	35 A	0.10 Ω
IXTH 40N30	300 V	40 A	0.085 Ω
IXTM 40N30	300 V	40 A	0.088 Ω

N-Channel Enhancement Mode

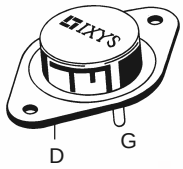


Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		300	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		300	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	35N30	35	A
		40N30	40	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	35N30	140	A
		40N30	160	A
P_D	T_C = 25°C		300	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
M_d	Mounting torque		1.13/10	Nm/lb.in.
Weight			TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s			300	°C

TO-247 AD (IXTH)



TO-204 AE (IXTM)



G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 µA		300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$	T_J = 25°C			200	µA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5\ I_{D25}$	IXTH35N30			0.10	Ω
		IXTH40N30			0.085	Ω
		IXTM40N30			0.088	Ω
	Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %					

Features

- International standard packages
- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Low package inductance (< 5 nH)
  - easy to drive and to protect
- Fast switching times

Applications

- Switch-mode and resonant-mode power supplies
- Motor controls
- Uninterruptible Power Supplies (UPS)
- DC choppers

Advantages

- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density

IXYS reserves the right to change limits, test conditions, and dimensions.

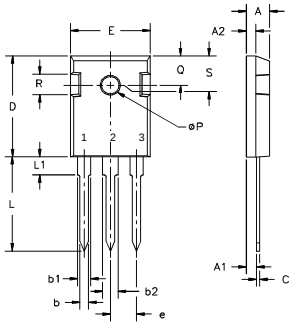
91535E(5/96)

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 • I_{D25}, pulse test	22	25		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4600		pF
C_{oss}			650		pF
C_{rss}			240		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 I_{D25} R_G = 2 Ω, (External)		24	30	ns
t_r			40	90	ns
$t_{d(off)}$			75	100	ns
t_f			40	90	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 I_{D25}		190	220	nC
Q_{gs}			28	50	nC
Q_{gd}			85	105	nC
R_{thJC}				0.42	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		min.	typ.	max.	
I_S	V_{GS} = 0 V	35N30			35	A
		40N30			40	A
I_{SM}	Repetitive; pulse width limited by T_{JM}	35N30			140	A
		40N30			160	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				1.5	V
t_{rr}	I_F = I_S, -di/dt = 100 A/µs, V_R = 100 V			400		ns

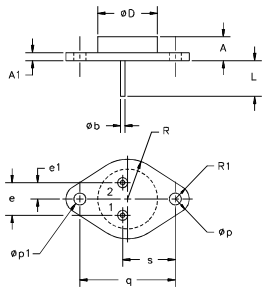
TO-247 AD (IXTH) Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

TO-204AE (IXTM) Outline



Pins 1 - Gate 2 - Source
Case - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	6.4	11.4	.250	.450
A1	1.53	3.42	.060	.135
∅b	1.45	1.60	.057	.063
∅D		22.22		.875
e	10.67	11.17	.420	.440
e1	5.21	5.71	.205	.225
L	11.18	12.19	.440	.480
∅p	3.84	4.19	.151	.165
∅p1	3.84	4.19	.151	.165
q	30.15 BSC		1.187 BSC	
R	12.58	13.33	.495	.525
R1	3.33	4.77	.131	.188
s	16.64	17.14	.655	.675

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:
4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Fig. 1 Output Characteristics

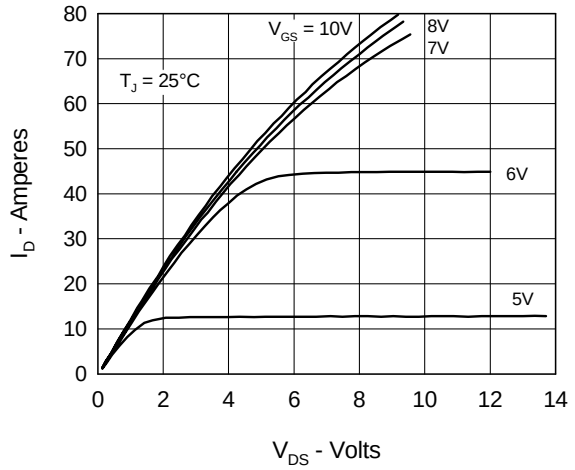


Fig. 2 Input Admittance

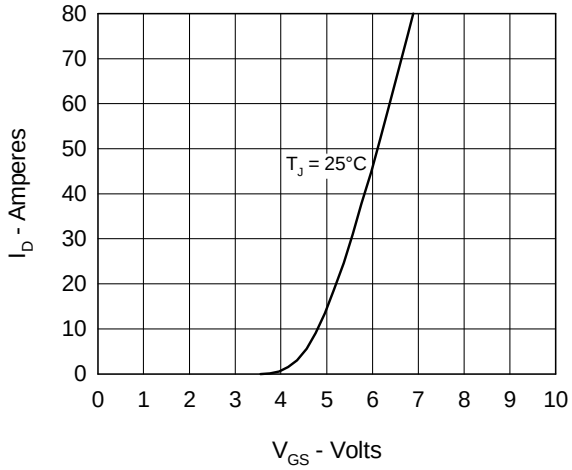


Fig. 3 $R_{DS(on)}$ vs. Drain Current

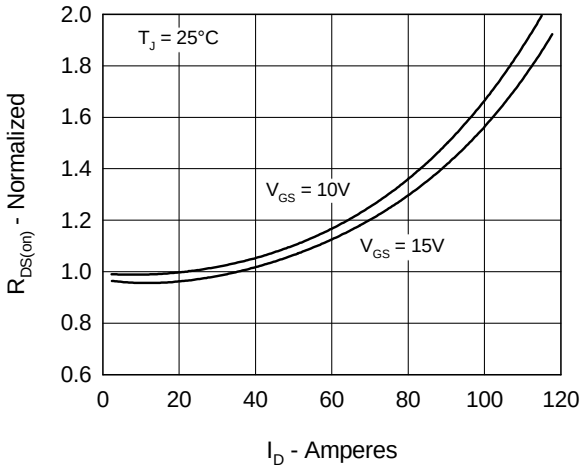


Fig. 4 Temperature Dependence of Drain to Source Resistance

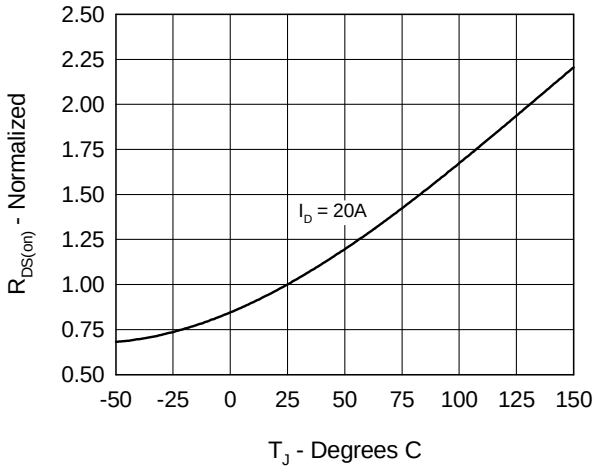


Fig. 5 Drain Current vs. Case Temperature

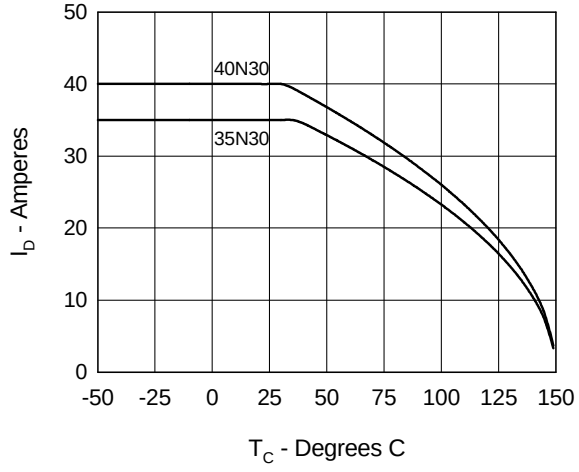


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

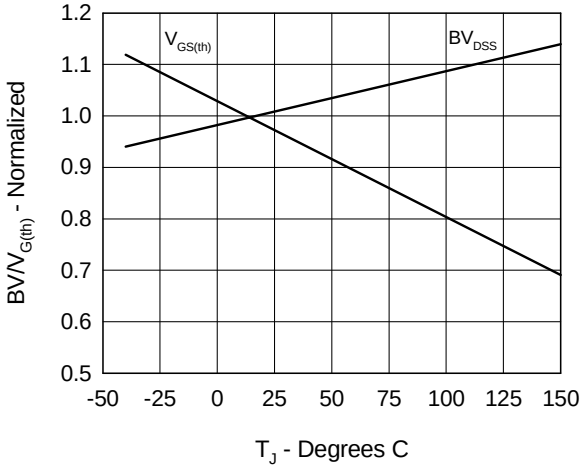


Fig.7 Gate Charge Characteristic Curve

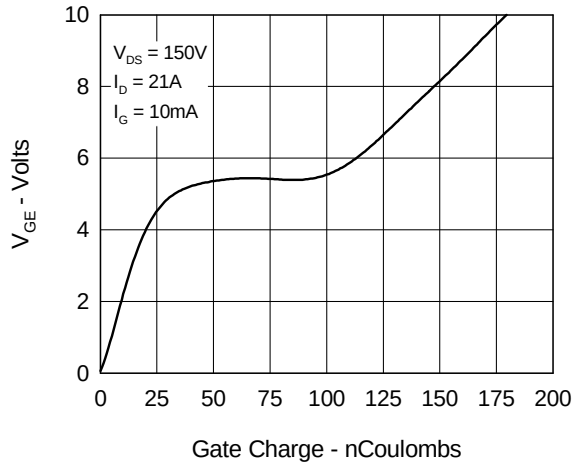


Fig.8 Forward Bias Safe Operating Area

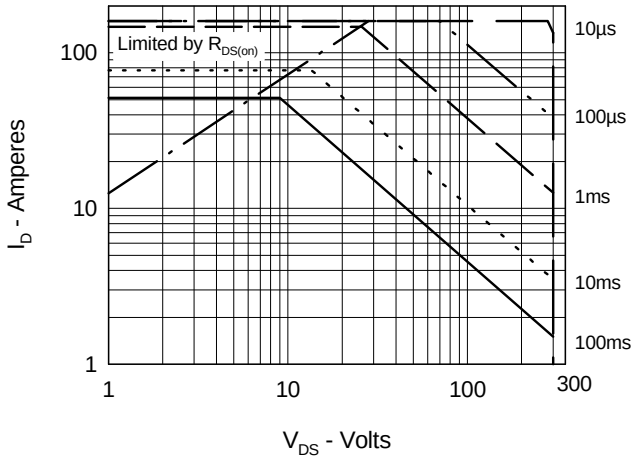


Fig.9 Capacitance Curves

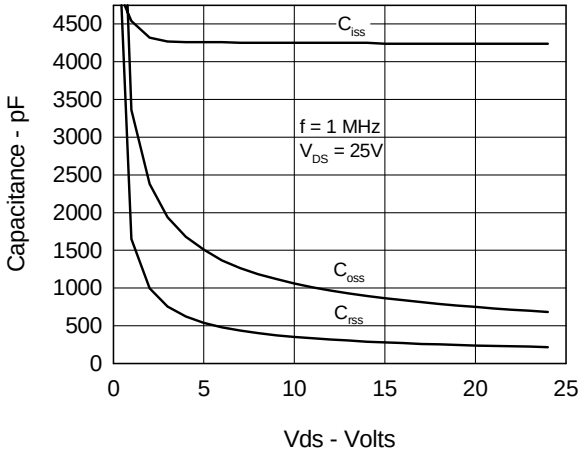


Fig.10 Source Current vs. Source to Drain Voltage

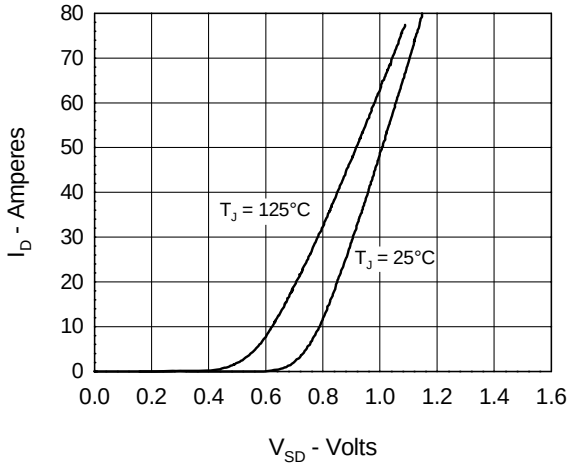


Fig.11 Transient Thermal Impedance