

TOSHIBA

TC55V1403J/FT-15,-20

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS
4,194,304-WORD BY 1-BIT/1,048,576-WORD BY 4-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V1403J/FT is a 4,194,304-bit high speed static random access memory (SRAM), it is possible to change the organization between 4,194,304 words by 1 bit and 1,048,576 words by 4 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable (\overline{CE}) can be used to place the device in a low-power mode, and output enable (\overline{OE}) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTTL compatible. The TC55V1403J/FT is available in a plastic 32-pin SOJ and TSOP package (400 mil width) for high density surface assembly.

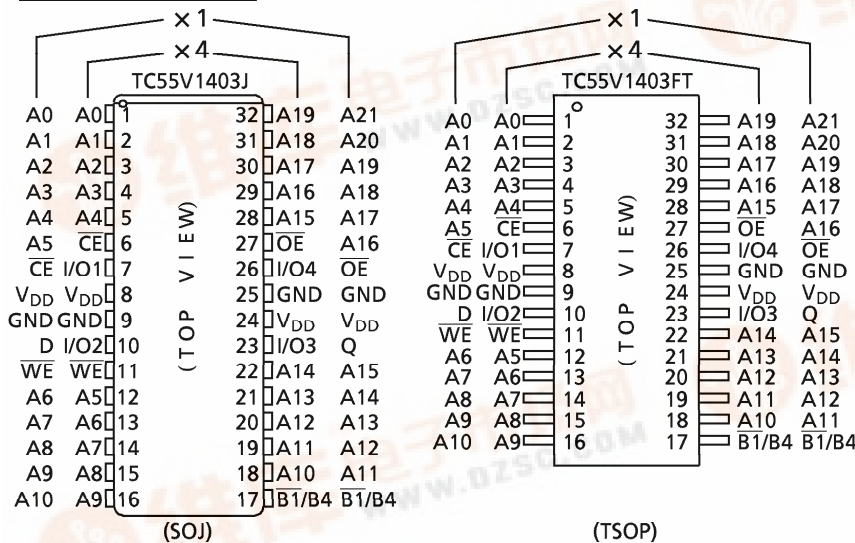
FEATURES

- Fast access time (the following are maximum values)
 - TC55V1403J/FT-15 : 15 ns
 - TC55V1403J/FT-20 : 20 ns
- Low-power dissipation (the following are maximum values)

Cycle Time	15	20	25	ns
Operation (max)	140	130	110	mA

Standby : 10mA (both devices)
- Single power supply voltage of 3.3V ± 0.3V
- Fully static operation
- All inputs and outputs are LVTTTL compatible
- Separate data input and output (×1 Mode), Common data input and output (×4 Mode)
- Output buffer control using \overline{OE}
- Package :
 - SOJ32-P-400-1.27A (J) (Weight : 1.22 g typ)
 - TSOP II 32-P-400-1.27 (FT) (Weight : 0.51 g typ)

PIN ASSIGNMENT



PIN NAMES

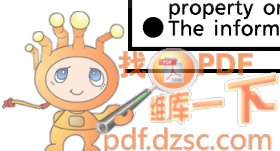
A0 to A21	Address Inputs
I/O1 to I/O4	Data Inputs/Outputs
D	Data Input
Q	Data Output
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+ 3.3 V)
GND	Ground
B1/B4	Bit Function

Note

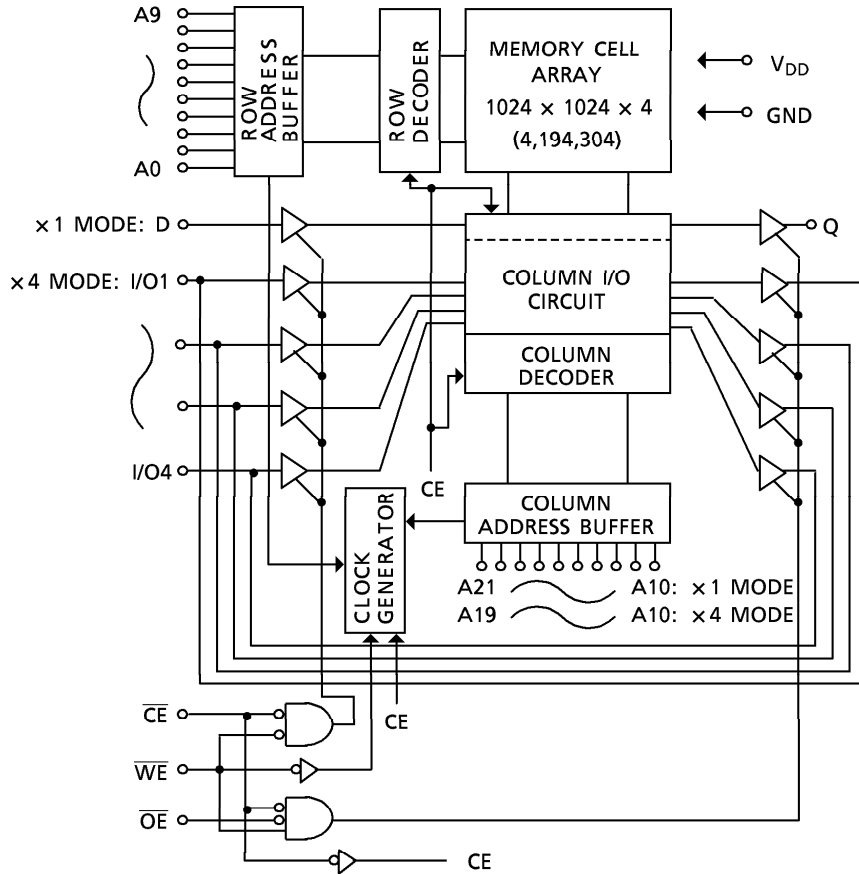
- ×1 mode : $\overline{B1/B4}$ = Low
- ×4 mode : $\overline{B1/B4}$ = High

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	- 0.5* to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	- 0.5* to $V_{DD} + 0.5^{**}$	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 65 to 150	°C
T_{opr}	Operating Temperature	- 10 to 85	°C

* : -1.5V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : $V_{DD} + 1.5V$ with a pulse width of 20% · t_{RC} min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	$V_{DD} + 0.3^{**}$	V
V_{IL}	Input Low Voltage	- 0.3*	-	0.8	V

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : $V_{DD} + 1.0V$ with a pulse width of 20% · t_{RC} min (4ns max)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT			
I _{IL}	Input Leakage Current (Except $\overline{B1/B4}$ pin)	V _{IN} = 0 to V _{DD}	-1	-	1	μA			
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 to V _{DD}	-1	-	1	μA			
I _I ($\overline{B1/B4}$)	Input Current ($\overline{B1/B4}$ pin)	V _{IN} = 0 to V _{DD}	-1	-	10	μA			
V _{OH}	Output High Voltage	I _{OH} = -2mA	2.4	-	-	V			
		I _{OH} = -100μA	V _{DD} - 0.2	-	-				
V _{OL}	Output Low Voltage	I _{OL} = 2mA	-	-	0.4	V			
		I _{OL} = 100μA	-	-	0.2				
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0mA	tcycle = 15ns	-	-	140			
		$\overline{OE} = V_{IH}$				tcycle = 20ns	-	-	130
		Other Inputs = V _{IH} / V _{IL}				tcycle = 25ns	-	-	110
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} or V _{IL}	-	-	55	mA			
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	-	-	10				

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O} , C _{OUT}	Input/Output, Output Capacitance	V _{I/O} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

TC55V1403J/FT is possible to change the organization of bit mode between 4M words by one bit and 1M words by four bits with input level of pin condition $\overline{B1/B4}$.

“4M × 1 Mode” is performed on when pin $\overline{B1/B4}$ is held on “GND level”. On the other hand “1M × 4 Mode” requires $\overline{B1/B4}$ be connected to “V_{DD} level”.

Input level of $\overline{B1/B4}$ condition must be set at the same time of power on. Any of change of input level $\overline{B1/B4}$, high or low, is prohibited after power on.

MODE		$\overline{B1/B4}$	\overline{CE}	\overline{OE}	\overline{WE}	I/O	POWER
× 1 MODE	Read	L	L	L	H	Output	I _{DDO}
	Write	L	L	×	L	Input	I _{DDO}
	Output Disabled	L	L	H	H	High Impedance	I _{DDO}
	Standby	L	H	×	×	High Impedance	I _{DDS}
× 4 MODE	Read	H	L	L	H	Output	I _{DDO}
	Write	H	L	×	L	Input	I _{DDO}
	Output Disabled	H	L	H	H	High Impedance	I _{DDO}
	Standby	H	H	×	×	High Impedance	I _{DDS}

× : Don't care

AC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C (Note 1), $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

READ CYCLE

SYMBOL	PARAMETER	TC55V1403J/FT-15		TC55V1403J/FT-20		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	15	-	20	-	ns
t_{ACC}	Address Access Time	-	15	-	20	
t_{CO}	Chip Enable Access Time	-	15	-	20	
t_{OE}	Output Enable Access Time	-	8	-	10	
t_{OH}	Output Data Hold Time from Address Change	4	-	5	-	
t_{COE}	Output Enable Time from Chip Enable	4	-	5	-	
t_{OEE}	Output Enable Time from Output Enable	1	-	1	-	
t_{COD}	Output Disable Time from Chip Enable	-	8	-	8	
t_{ODO}	Output Disable Time from Output Enable	-	8	-	8	

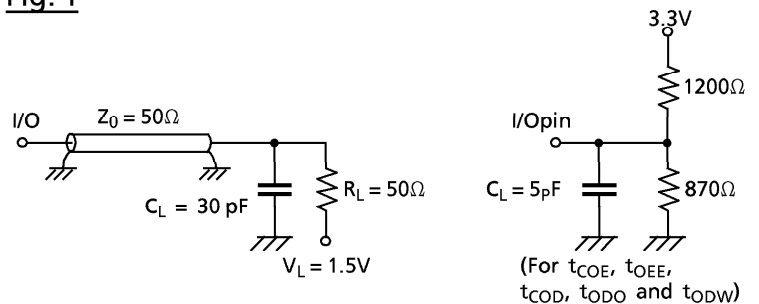
WRITE CYCLE

SYMBOL	PARAMETER	TC55V1403J/FT-15		TC55V1403J/FT-20		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	15	-	20	-	ns
t_{WP}	Write Pulse Width	9	-	11	-	
t_{CW}	Chip Enable to End of Write	12	-	13	-	
t_{AW}	Address Valid to End of Write	12	-	13	-	
t_{AS}	Address Setup Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{DS}	Data Setup Time	8	-	10	-	
t_{DH}	Data Hold Time	0	-	0	-	
t_{OEW}	Output Enable Time from Write Enable	1	-	1	-	
t_{ODW}	Output Disable Time from Write Enable	-	8	-	8	

AC TEST CONDITIONS

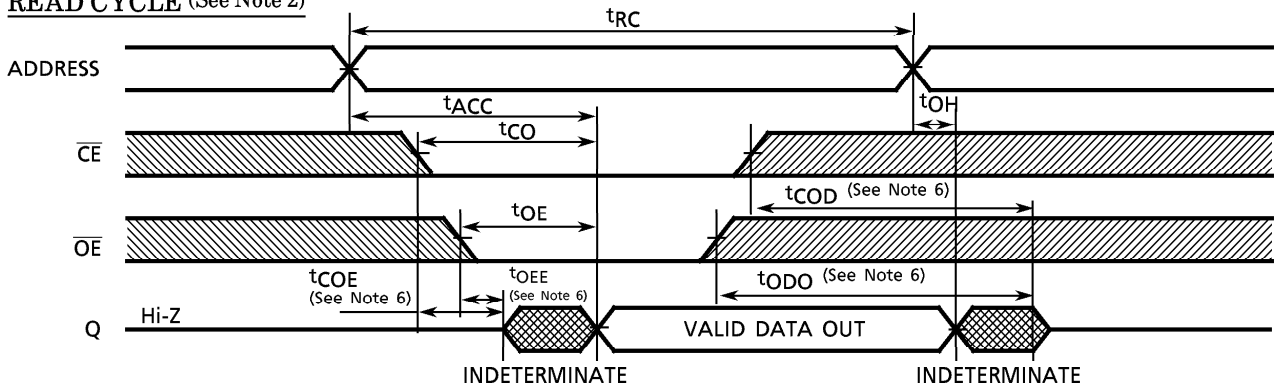
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

Fig. 1

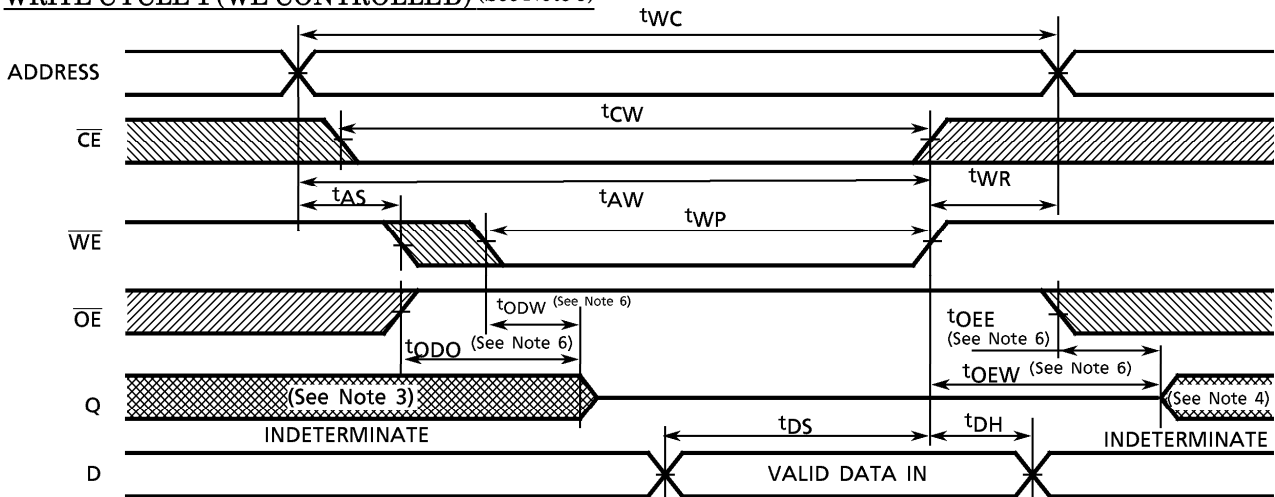


TIMING DIAGRAMS

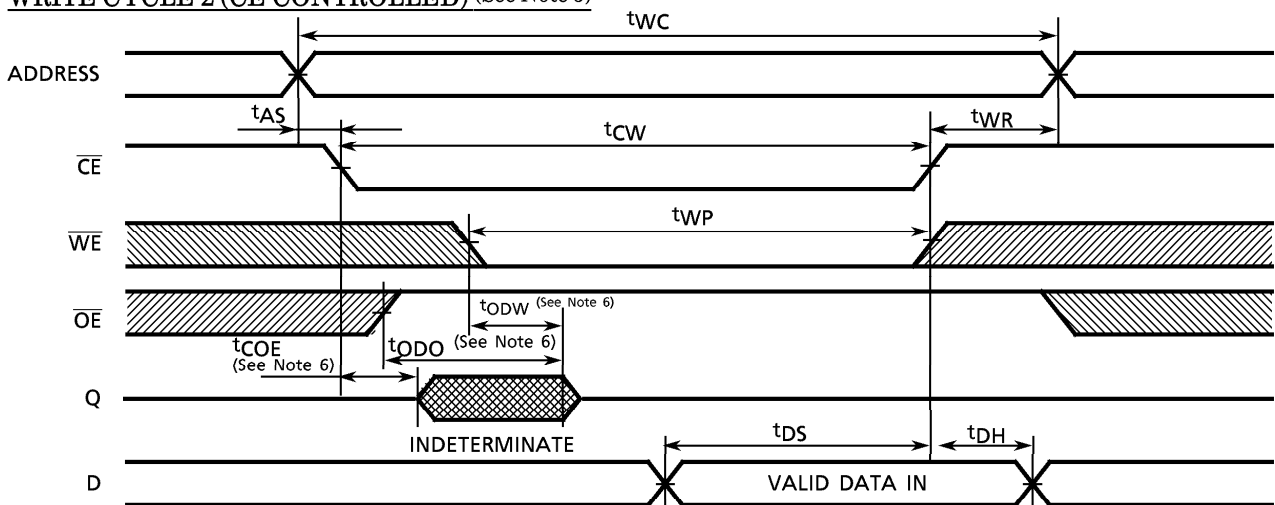
READ CYCLE (See Note 2)



WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 5)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 5)



Note: (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) \overline{WE} remains HIGH for Read Cycle.

(3) If \overline{CE} goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.

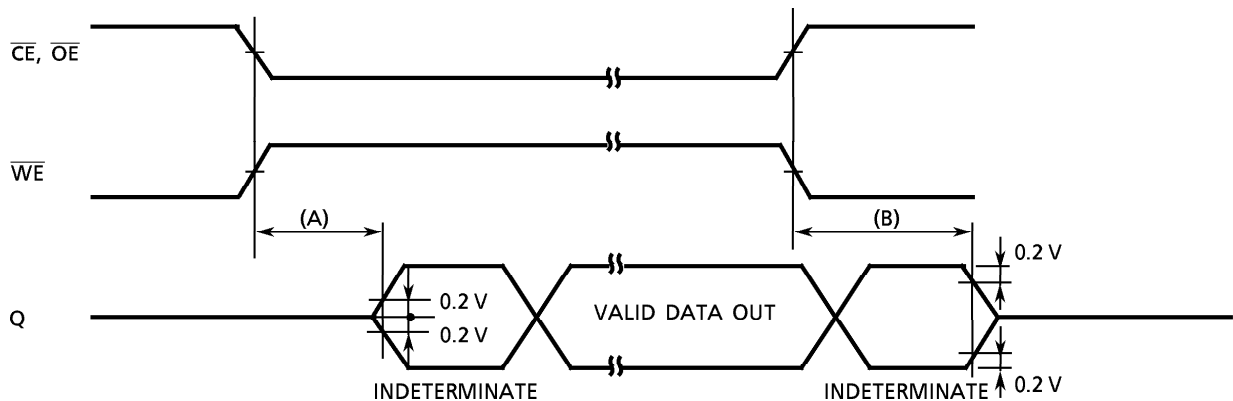
(4) If \overline{CE} goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.

(5) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{OE\overline{W}}$ Output Enable Time

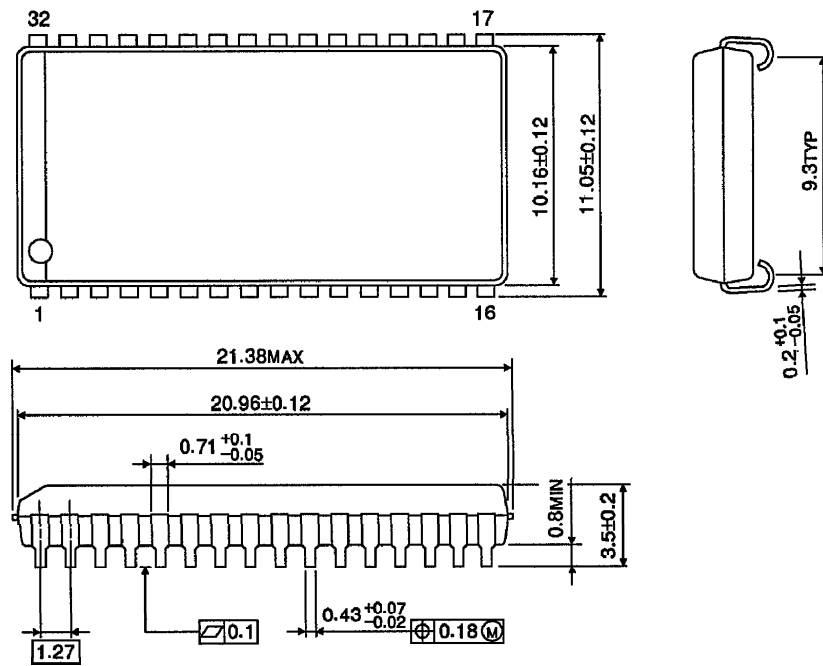
(B) $t_{COD}, t_{ODO}, t_{OD\overline{W}}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ32-P-400-1.27A)

Unit in mm

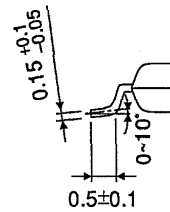
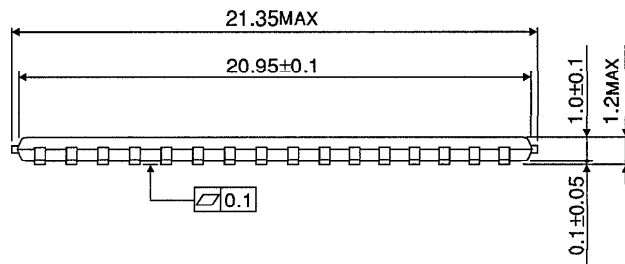
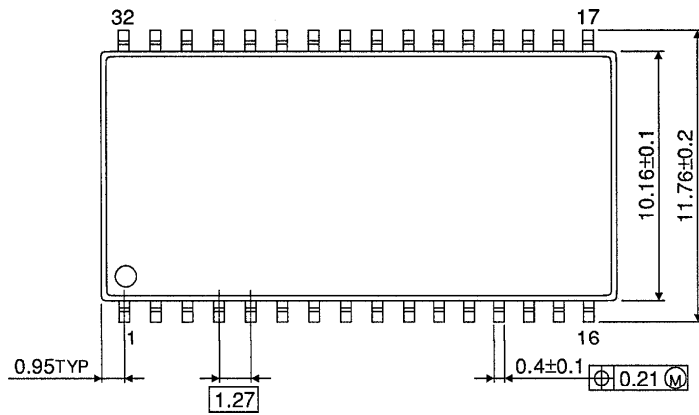


Weight: 1.22 g (typ)

PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 32-P-400-1.27)

Unit in mm



Weight: 0.51 g (typ)