calogic CORPORATION

N-Channel JFET Switch

J108 – J110 / SST108 – SST110

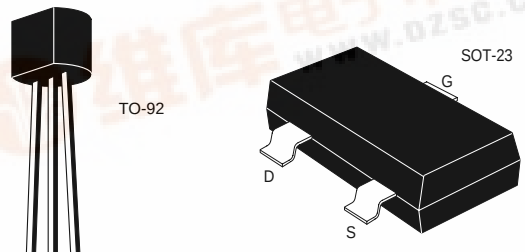
FEATURES

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Fast Switching
- Low Noise

APPLICATIONS

- Analog Switches
- Choppers
- Commutators
- Low-Noise Audio Amplifiers

PIN CONFIGURATION



5018

PRODUCT MARKING (SOT-23)	
SST108	I08
SST109	I09
SST110	I10

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage . . . . . -25V
Gate Current 50mA
Storage Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -55°C to +135°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation 360mW
Derate above 25°C . . . . . 3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
J108-110	Plastic TO-92	-55°C to +135°C
XJ108-110	Sorted Chips in Carriers	-55°C to +135°C
SST109-110	Plastic SOT-23	-55°C to +135°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	108			109			110			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0V, V_{GS} = -15V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	-2		-6	-0.5		-4	V	V_{DS} = 5V, I_D = 1µA	
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0V, I_G = -1µA	
I_{DSS}	Drain Saturation Current (Note 2)	80			40			10			mA	V_{DS} = 15V, V_{GS} = 0V	
$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5V, V_{GS} = -10V	
$r_{DS(on)}$	Drain-Source ON Resistance			8			12			18	Ω	V_{DS} ≤0.1V, V_{GS} = 0V	
$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	V_{DS} = 0, V_{GS} = -10V (Note 3)	f = 1MHz
$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15			
$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85		V_{DS} = V_{GS} = 0 (Note 3)	
$t_{d(on)}$	Turn On Delay Time		4			4			4		ns	Switching Time Test Conditions (Note 3)	
t_r	Rise Time		1			1			1				
$t_{d(off)}$	Turn OFF Delay Time		6			6			6				
t_f	Fall Time		30			30			30				

	J107	J109	J110
V_{DD}	1.5V	1.5V	1.5V
$V_{GS(off)}$	-12V	-7V	-5V
R_L	150Ω	150Ω	150Ω

NOTES: **1.** Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300µs; duty cycle ≤3%.
3. For design reference only, not 100% tested.