

MOS FIELD EFFECT TRANSISTOR **2SJ600**

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ600 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low on-state resistance:

 $R_{DS(on)1} = 50~m\Omega~MAX.~(V_{GS} = -10~V,~I_{D} = -13~A)$ $R_{DS(on)2} = 79~m\Omega~MAX.~(V_{GS} = -4.0~V,~I_{D} = -13~A)$

- Low Ciss: Ciss = 1900 pF TYP.
- · Built-in gate protection diode
- TO-251/TO-252 package

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SJ600	TO-251		
2SJ600-Z	TO-252		

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-60	V	
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V	
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓25	Α	
Drain Current (pulse) Note1	ID(pulse)	∓70	Α	
Total Power Dissipation (Tc = 25°C)	Рт	45	W	
Total Power Dissipation (T _A = 25°C)	Рт	1.0	W	
Channel Temperature	Tch	150	°C	
Storage Temperature	Tstg	-55 to +150	°C	
Single Avalanche Current Note2	las	-25	Α	
Single Avalanche Energy Note2	Eas	62.5	mJ	

(TO-251)



(TO-252)



Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = -20 V \rightarrow 0 V

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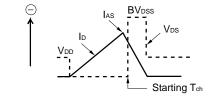


ELECTRICAL CHARACTERISTICS (TA = 25°C)

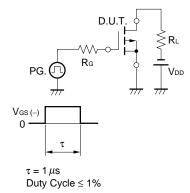
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	Vps = -60 V, Vgs = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = + 20 V, V _{DS} = 0 V			Ŧ10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, \text{ ID} = -1 \text{ mA}$	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = -10 V, I _D = -13 A	10	20		S
Drain to Source On-state Resistance	R _{DS(on)1}	Vgs = -10 V, ID = -13 A		41	50	mΩ
	RDS(on)2	Vgs = -4.0 V, ID = -13 A		55	79	mΩ
Input Capacitance	Ciss	V _{DS} = −10 V,		1900		pF
Output Capacitance	Coss	Vgs = 0 V,		350		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		140		pF
Turn-on Delay Time	td(on)	ID = −13 A,		9		ns
Rise Time	tr	$V_{GS(on)} = -10 V$,		10		ns
Turn-off Delay Time	td(off)	$V_{DD} = -30 V$,		67		ns
Fall Time	tf	$R_G = 0 \Omega$		19		ns
Total Gate Charge	QG	ID = −25 A,		38		nC
Gate to Source Charge	Qgs	V _{DD} = -48 V,		7		nC
Gate to Drain Charge	Q _{GD}	Vgs = -10 V		10	_	nC
Body Diode Forward Voltage	V _F (S-D)	IF = -25 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = -25 A, VGS = 0 V		49		ns
Reverse Recovery Charge	Qrr	$di/dt = -100 \text{ A}/\mu\text{s}$		100		nC

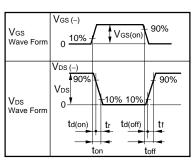
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c|c} \text{D.U.T.} \\ \text{RG} = 25 \ \Omega \\ \text{VGS} = -20 \ \text{V} \rightarrow 0 \ \text{V} \\ \end{array}$

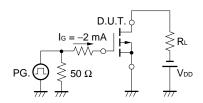


TEST CIRCUIT 2 SWITCHING TIME





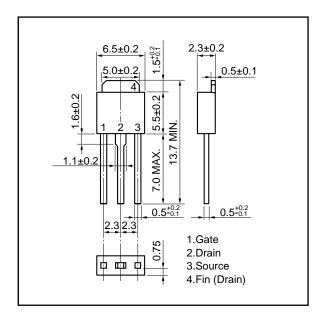
TEST CIRCUIT 3 GATE CHARGE



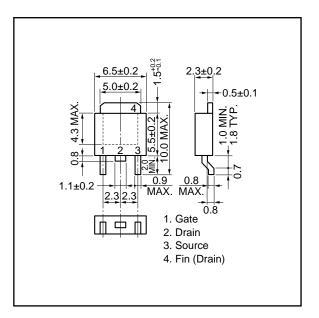


PACKAGE DRAWINGS (Unit: mm)

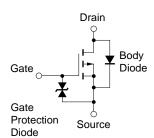
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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