MIC5254

Dual 150mA μCap LDO with Error Flag Outputs

General Description

The MIC5254 is an efficient, precise, dual CMOS voltage regulator. It offers better than 1% initial accuracy, extremely low dropout voltage (typically 135mV at 150mA) and low ground current (typically 90μA) over load. The MIC5254 features two independent LDOs with error flags that indicate an output fault condition such as overcurrent, thermal shutdown and dropout.

Designed specifically for handheld and battery-powered devices, the MIC5254 provides a TTL-logic-compatible enable pin. When disabled, power consumption drops nearly to zero.

The MIC5254 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in handheld wireless devices.

Key features include current limit, thermal shutdown, faster transient response, and an active clamp to speed up device turnoff. The MIC5254 is available in the MSOP-10 package and is rated over a –40°C to +125°C junction temperature range.

Features

- Input voltage range: 2.7V to 6.0V
- Dual, independent 150mA LDOs
- Error flags indicate fault condition
- Stable with ceramic output capacitor
- Ultra-low dropout: 135mV @ 150mA
- High output accuracy:
  - 1.0% initial accuracy
  - 2.0% over temperature
- Low quiescent current: 90μA each LDO
- Tight load and line regulation
- Thermal shutdown and current limit protection
- "Zero" off-mode current
- TTL logic-controlled enable input
- MSOP-10 package

Applications

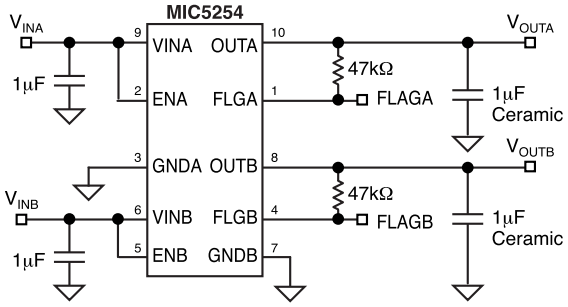
- Cellular phones and pagers
- Cellular accessories
- Battery-powered equipment
- Laptop, notebook, and palmtop computers
- Consumer/personal electronics

Ordering Information

Part Number	VOUTA	VOUTB	Junction Temp. Range	Package
MIC5254-SJBMM	3.3V	2.5V	–40°C to +125°C	MSOP-10

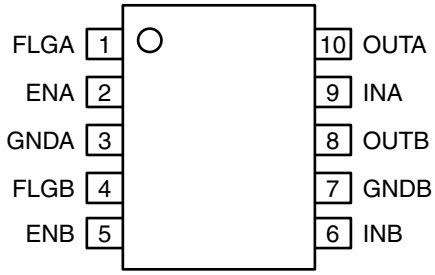
Other voltages available. Contact Micrel Marketing for details.

Typical Application



Dual Output LDO with Error Flags

Pin Configuration



MSOP-10 (BMM)

Pin Description

Pin Number	Pin Name	Channel	Pin Function
1	FLGA	A	Error Flag (Output): Open-drain output. Active low indicates an output undervoltage condition.
2	ENA	A	Enable/Shutdown (Input): CMOS compatible input. Logic high = enable; logic low = shutdown. Do not leave open.
3	GNDA	A	Ground.
9	INA	A	Supply Input.
10	OUTA	A	Regulator Output.
4	FLGB	B	Error Flag (Output): Open-drain output. Active low indicates an output undervoltage condition.
5	ENB	B	Enable/Shutdown (Input): CMOS compatible input. Logic high = enable; logic low = shutdown. Do not leave open.
7	GNDB	B	Ground.
6	INB	B	Supply Input.
8	OUTB	B	Regulator Output.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage (V_{IN}) ..... 0V to +7V
Enable Input Voltage (V_{EN}) ..... 0V to +7V
Power Dissipation (P_D) ..... Internally Limited, **Note 3**
Junction Temperature (T_J) ..... –40°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (soldering, 5 sec.) ..... 260°C
ESD, **Note 4** 2kV

Operating Ratings (Note 2)

Input Voltage (V_{IN}) ..... +2.7V to +6V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Thermal Resistance
MSOP-10 (θ_{JA}) ..... 200°C/W

Electrical Characteristics (Note 5)

$V_{IN} = V_{OUT} + 1V$, $V_{EN} = V_{IN}$; $I_{OUT} = 100\mu A$; $T_J = 25°C$, **bold** values indicate $–40°C \le T_J \le +125°C$; unless noted.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy	$I_{OUT} = 100\mu A$	–1 **–2**		+1 **+2**	% %
ΔV_{LNR}	Line Regulation	$V_{IN} = V_{OUT} + 1V$ to 6V		0.02	0.075	%/V
ΔV_{LDR}	Load Regulation	I_{OUT} = 0.1mA to 150mA, **Note 6**		1.5	2.5	%
$V_{IN} – V_{OUT}$	Dropout Voltage, **Note 7**	$I_{OUT} = 100\mu A$		0.1		mV
		I_{OUT} = 100mA		90	150	mV
		I_{OUT} = 150mA		135	200 **250**	mV mV
I_Q	Quiescent Current	$V_{EN} \le 0.4V$ (shutdown)		0.2	**1**	µA
I_{GND}	Ground Pin Current, **Note 8**	I_{OUT} = 0mA		90	150	µA
		I_{OUT} = 150mA		117		µA
PSRR	Power Supply Rejection	f = 10Hz, $V_{IN} = V_{OUT} + 1V$; $C_{OUT} = 1\mu F$		60		dB
		f = 100Hz, $V_{IN} = V_{OUT} + 0.5V$; $C_{OUT} = 1\mu F$		60		dB
		f = 10kHz, $V_{IN} = V_{OUT} + 0.5V$		45		dB
I_{LIM}	Current Limit	$V_{OUT} = 0V$	160	425		mA
e_n	Output Voltage Noise			30		µV(rms)
Enable Input						
V_{IL}	Enable Input Logic-Low Voltage	V_{IN} = 2.7V to 5.5V, regulator shutdown			**0.4**	V
V_{IH}	Enable Input Logic-High Voltage	V_{IN} = 2.7V to 5.5V, regulator enabled	**1.6**			V
I_{EN}	Enable Input Current	$V_{IL} \le 0.4V$, regulator shutdown		0.01		µA
		$V_{IH} \ge 1.6V$, regulator enabled		0.01		µA
	Shutdown Resistance Discharge			500		Ω
Error Flag						
V_{FLG}	Low Threshold High Threshold	% of V_{OUT} (Flag ON) % of V_{OUT} (Flag OFF)	90		 96	% %
V_{OL}	Output Logic-Low Voltage	$I_L = 100\mu A$, fault condition		0.02	**0.1**	V
I_{FL}	Flag Leakage Current	Flag OFF, V_{FLG} = 6V		0.01		µA
Thermal Protection						
	Thermal Shutdown Temperature			150		°C
	Thermal Shutdown Hysteresis			10		°C

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)}–T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JA} of the MIC5254-SJBMM is 200°C/W on a PC board (see *"Thermal Considerations"* section for further details).

Note 4. Devices are ESD sensitive. Handling precautions recommended.

Note 5. Specification for packaged product only.

Note 6. Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 0.1mA to 150mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

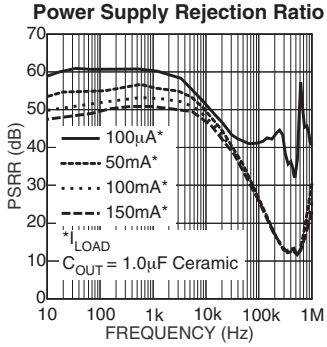
Note 7. Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. For outputs below 2.7V, dropout voltage is the input-to-output voltage differential with the minimum input voltage 2.7V. Minimum input operating voltage is 2.7V.

Note 8. Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

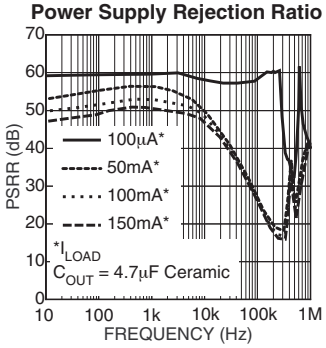
Typical Characteristics

For each LDO Channel.

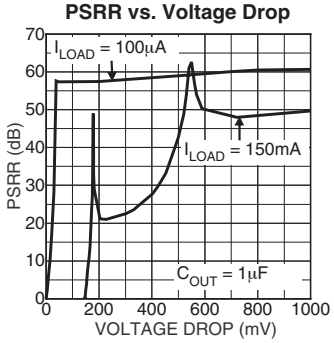
Power Supply Rejection Ratio



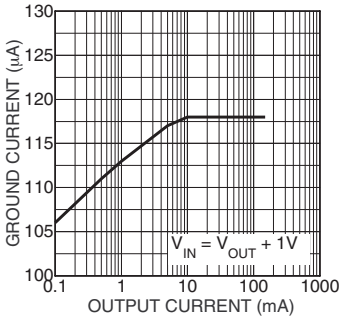
Power Supply Rejection Ratio



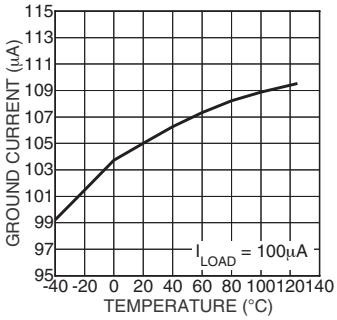
PSRR vs. Voltage Drop



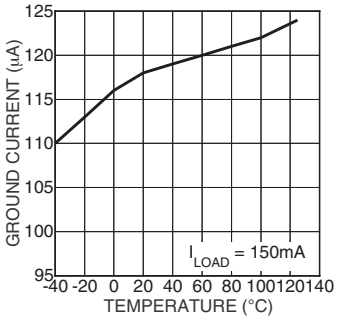
Ground Pin Current



Ground Pin Current



Ground Pin Current



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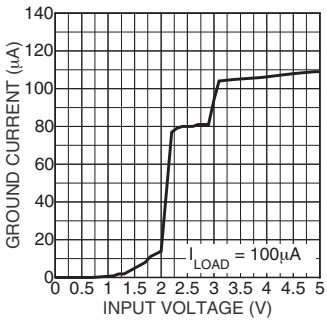
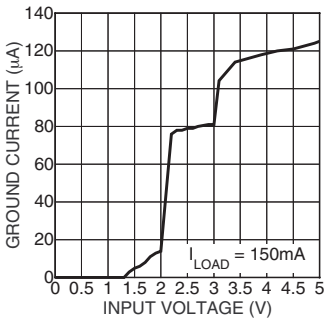
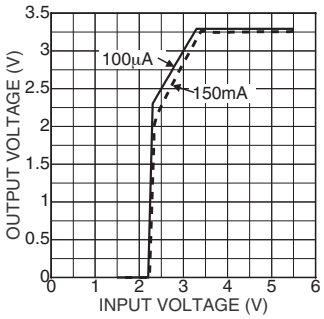


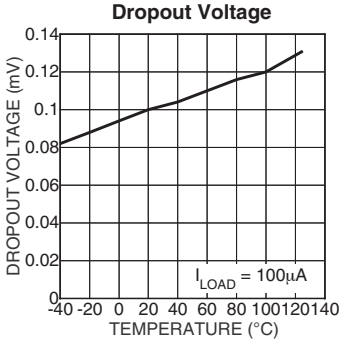
Ground Pin Current



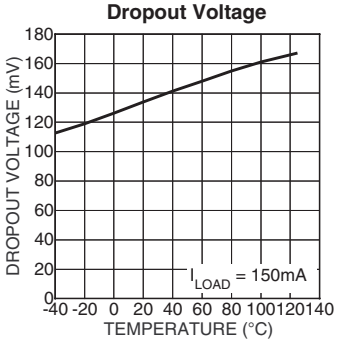
Dropout Characteristics



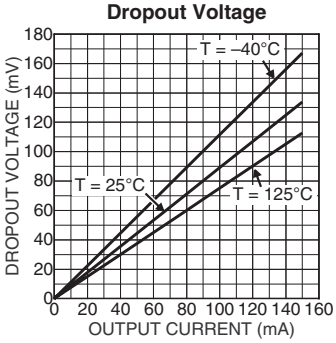
Dropout Voltage



Dropout Voltage

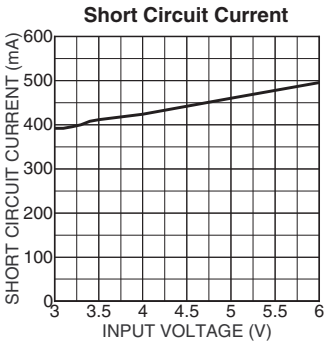


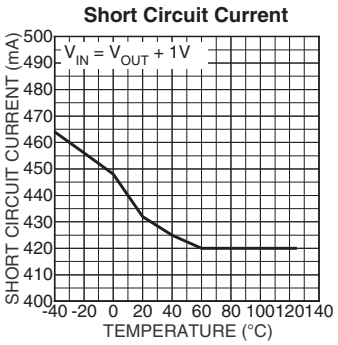
Dropout Voltage

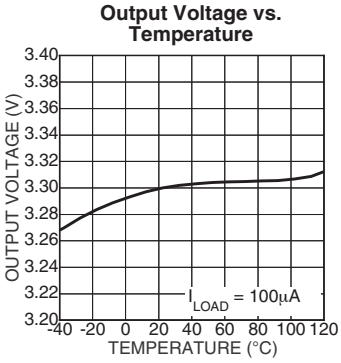


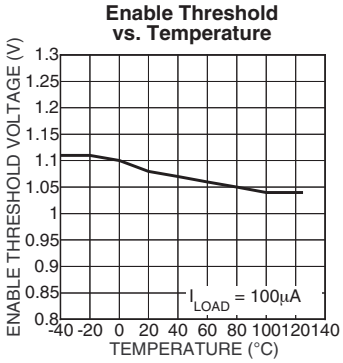
Typical Characteristics

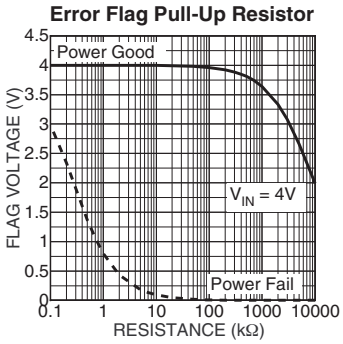
For each LDO Channel.



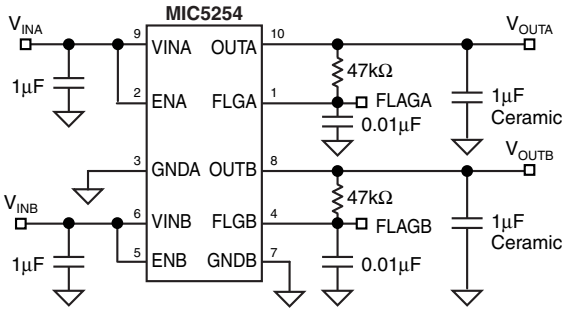








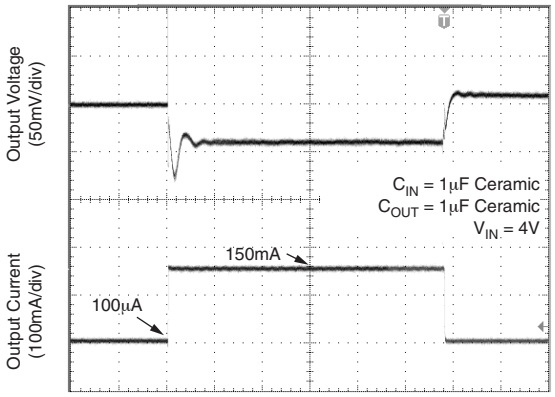
Test Circuit



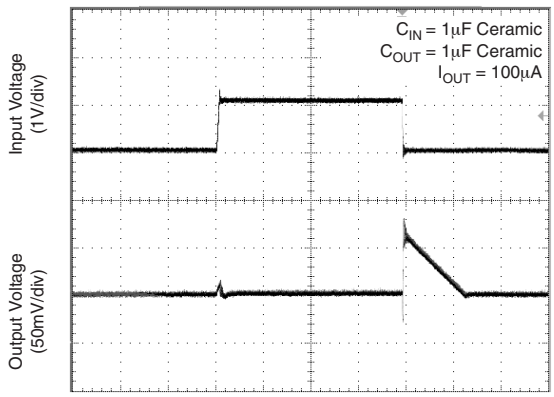
Functional Characteristics

For each LDO Channel

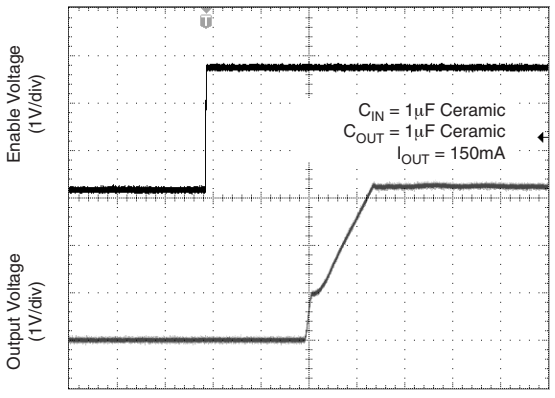
Load Transient Response



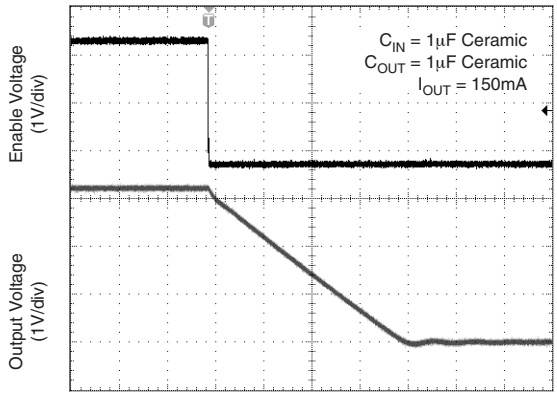
Line Transient Response



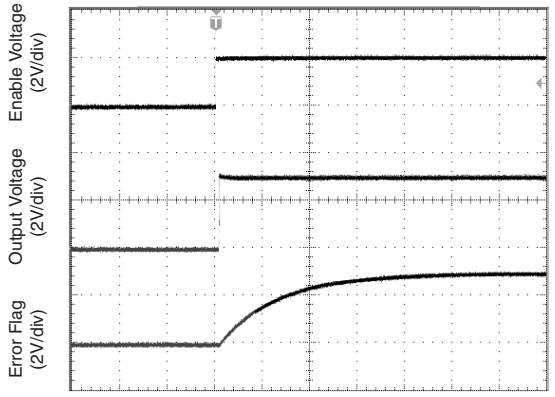
Enable Pin Delay



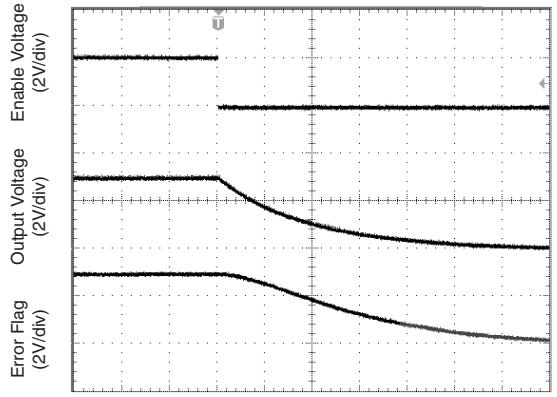
Shutdown Delay



Error Flag Start-up*



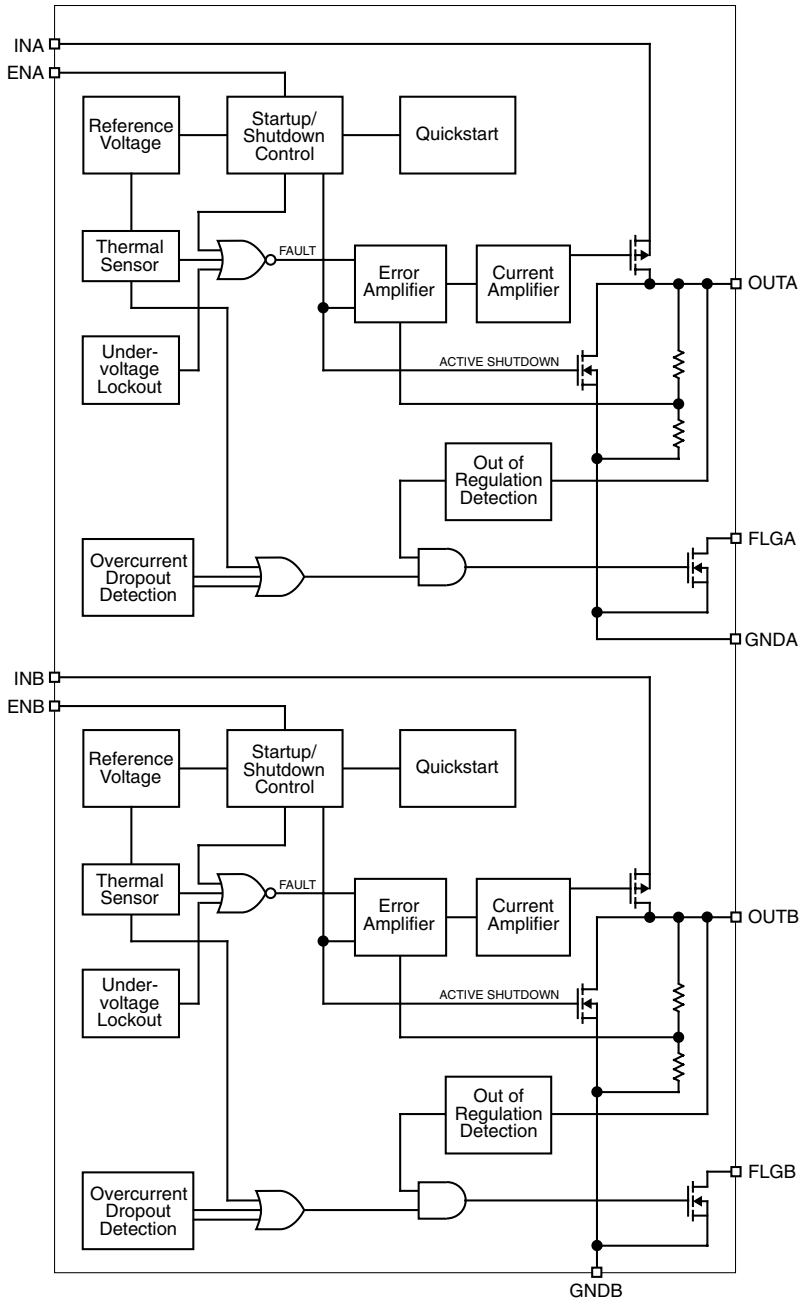
Error Flag Shutdown*



* See Test Circuit

* See Test Circuit

Functional Diagram



Applications Information

Enable/Shutdown

The MIC5254 comes with an active-high enable pin for each regulator that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a "zero" off-mode-current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. This part is CMOS and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

Input Capacitor

The MIC5254 is a high performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1μF capacitor is required from the input to ground to provide stability. Low ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small-valued NPO dielectric type capacitors, help filter out high frequency noise and are good practice in any RF based circuit.

Output capacitor

The MIC5254 requires an output capacitor for stability. The design requires 1μF or greater on the output to maintain stability. The design is optimized for use with low ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The maximum recommended ESR is 300mΩ. The output capacitor can be increased, but performance has been optimized for a 1μF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

Error Flag

The error flag output is an active-low, open-drain output that drives low when a fault condition AND an undervoltage detection occurs. Internal circuitry intelligently monitors overcurrent, overtemperature and dropout conditions and ORs these outputs together to indicate some fault condition. The output of that OR gate is ANDed with an output voltage monitor that detects an undervoltage condition. That output drives the open-drain transistor to indicate a fault. This prevents chattering or inadvertent triggering of the error flag. The error flag must be pulled-up using a resistor from the flag pin to either the input or the output.

The error flag circuit was designed essentially to work with a capacitor to ground to act as a power-on reset generator, signaling a power-good situation once the regulated voltage was up and/or out of a fault condition. This capacitor delays the error signal from pulling high, allowing the downstream circuits time to stabilize. When the error flag is pulled-up to the input without using a pull-down capacitor, there can be a glitch on the error flag upon start up of the device. This is due to the response time of the error flag circuit as the device starts up. When the device comes out of the "zero" off mode current state, all the various nodes of the circuit power up before the device begins supplying full current to the output capacitor. The error flag drives low immediately and then releases after a few microseconds. The intelligent circuit that triggers an error detects the output going into current limit AND the output being low while charging the output capacitor. The error output then pulls low for the duration of the turn-on time. A capacitor from the error flag to ground will filter out this glitch. The glitch does not occur if the error flag pulled up to the output.

Active Shutdown

The MIC5254 also features an active shutdown clamp, which is an N-Channel MOSFET that turns on when the device is disabled. This allows the output capacitor and load to discharge, de-energizing the load.

No Load Stability

The MIC5254 will remain stable and in regulation with no load unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

Thermal Considerations

The MIC5254 is a dual LDO voltage regulator designed to provide two output voltages from one package. Both regulator outputs are capable of sourcing 150mA of output current. Proper thermal evaluation needs to be done to ensure that the junction temperature does not exceed it's maximum value, 125°C. Maximum power dissipation can be calculated based on the output current and the voltage drop across each regulator. The sum of the power dissipation of each regulator determines the total power dissipation. The maximum power dissipation that this package is capable of handling can be determined using thermal resistance, junction to ambient, and the following basic equation:

$$P_{D(max)} = \left(\frac{T_{J(max)} - T_A}{\theta_{JA}} \right)$$

$T_{J(max)}$ is the maximum junction temperature of the die, 125°C and T_A is the ambient operating temperature of the die. θ_{JA} is layout dependent. Table 1 shows the typical thermal resistance for a minimum footprint layout for the MIC5254.

Package	θ_{JA} at Recommended Minimum Footprint
MSOP-10	200°C/W

Table 1. Thermal Resistance

The actual power dissipation of each regulator output can be calculated using the following simple equation:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}$$

Each regulator contributes power dissipation to the overall power dissipation of the package.

$$P_{D(total)} = P_{D(reg1)} + P_{D(reg2)}$$

Each output is rated for 150mA of output current, but the application may limit the amount of output current based on the total power dissipation and the ambient temperature. A typical application may call for one 3.3V output and one 2.5V output from a single Li-Ion battery input. This input can be as high as 4.2V.

When operating at high ambient temperatures, the output current may be limited. When operating at an ambient of 60°C, the maximum power dissipation of the package is calculated as follows:

$$P_{D(max)} = \left(\frac{125°C - 60°C}{200°C/W} \right)$$

$$P_D = 325mW$$

For the application mentioned above, if regulator 1 is sourcing 150mA, it contributes the following to the overall power dissipation:

$$P_{D(reg2)} = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}$$
$$P_{D(reg1)} = (4.2V - 3.3V)150mA + 4.2V \times 100\mu A$$
$$P_{D(reg1)} = 135.5mW$$

Since the total power dissipation allowable is 325mW, the maximum power dissipation of the second regulator is limited to:

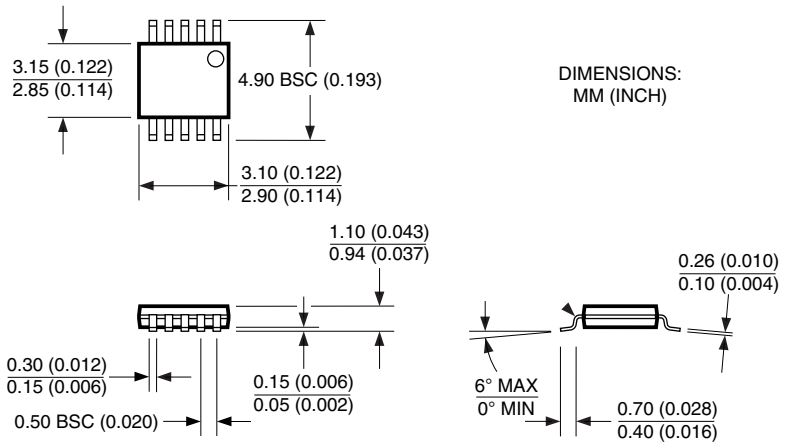
$$P_{D(max)} = P_{D(reg1)} + P_{D(reg2)}$$
$$325mW = 135.5mW + P_{D(reg2)}$$
$$P_{D(reg2)} = 189.5mW$$

The maximum output current of the second regulator can be calculated using the same equations but solving for the output current (ground current is constant over load and simplifies the equation):

$$P_{D(reg2)} = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}$$
$$189.5mW = (4.2V - 2.5V)I_{OUT} + 4.2V \times 100\mu A$$
$$I_{OUT} = 111.2mA$$

The second output is limited to 110mA due to the total power dissipation of the system when operating at 60°C ambient temperature.

Package Information



10-Pin MSOP (BMM)

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