



## QUINT 2-INPUT AND/NAND GATE

**SY10E104**  
**SY100E104**

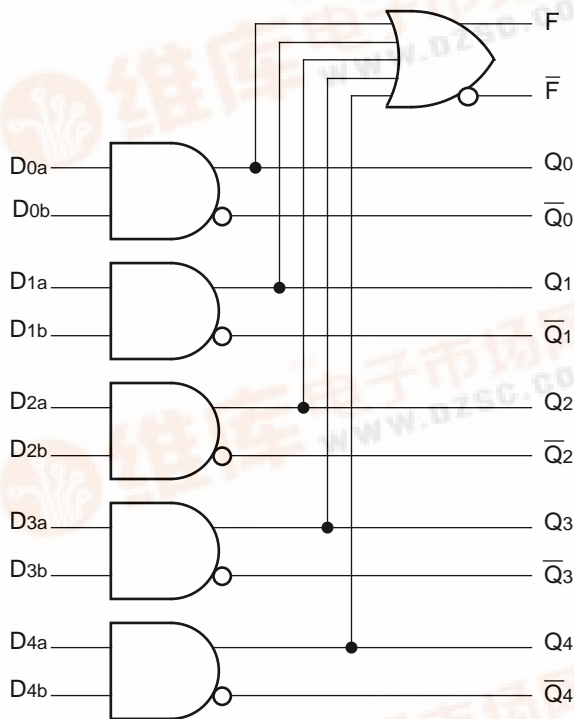
### FEATURES

- 600ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- True and complementary outputs
- OR/NOR function outputs
- Fully compatible with Industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E104
- Available in 28-pin PLCC package

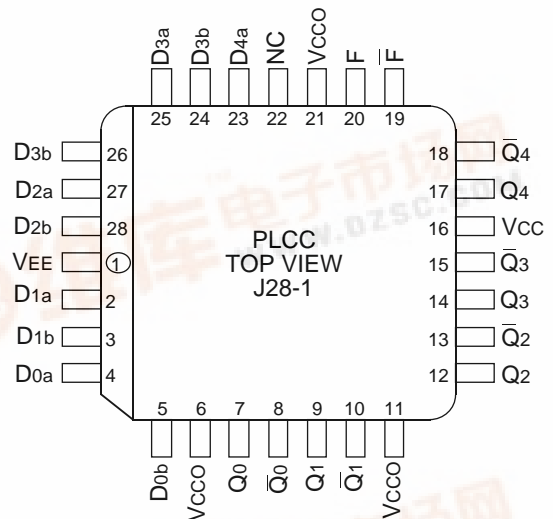
### DESCRIPTION

The SY10/100E104 are quint 2-input AND/NAND gates designed for use in new, high-performance ECL systems. The E104 also features a function output, F, which is the OR of all five AND gate outputs, while  $\bar{F}$  is the NOR. Both true and complementary outputs are provided.

### BLOCK DIAGRAM



### PIN CONFIGURATION



### PIN NAMES

Pin	Function
Dna, Dnb	Data Inputs
Q0-Q4	AND Outputs
$\bar{Q}0-\bar{Q}4$	NAND Outputs
F	OR Output
$\bar{F}$	NOR Output
Vcco	Vcc to Output

**LOGIC EQUATION**

$$F = (D_{0a} \cdot D_{0b}) + (D_{1a} \cdot D_{1b}) + (D_{2a} \cdot D_{2b}) + (D_{3a} \cdot D_{3b}) + (D_{4a} \cdot D_{4b})$$

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE} (\text{Min.})$  to  $V_{EE} (\text{Max.})$ ;  $V_{CC} = V_{CC0} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I <sub>IH</sub>	Input HIGH Current	—	—	200	—	—	200	—	—	200	—	—	200	μA
I <sub>EE</sub>	Power Supply Current	—	—	—	—	—	—	—	—	—	—	—	—	mA
		10E	38	46	38	46	38	46	38	46	38	46		
		100E	38	46	38	46	38	46	38	46	44	53		

**AC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE} (\text{Min.})$  to  $V_{EE} (\text{Max.})$ ;  $V_{CC} = V_{CC0} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output D to Q D to F	225 500	385 725	600 1000	225 500	385 725	600 1000	225 500	385 725	600 1000	225 500	385 725	600 1000	ps
t <sub>skew</sub>	Within-Device Skew, D to Q <sup>(1)</sup>	—	75	—	—	75	—	—	75	—	—	75	—	ps
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80% Q F	275 300	425 475	700 700	275 300	425 475	700 700	275 300	425 475	700 700	275 300	425 475	700 700	ps

**NOTE:**

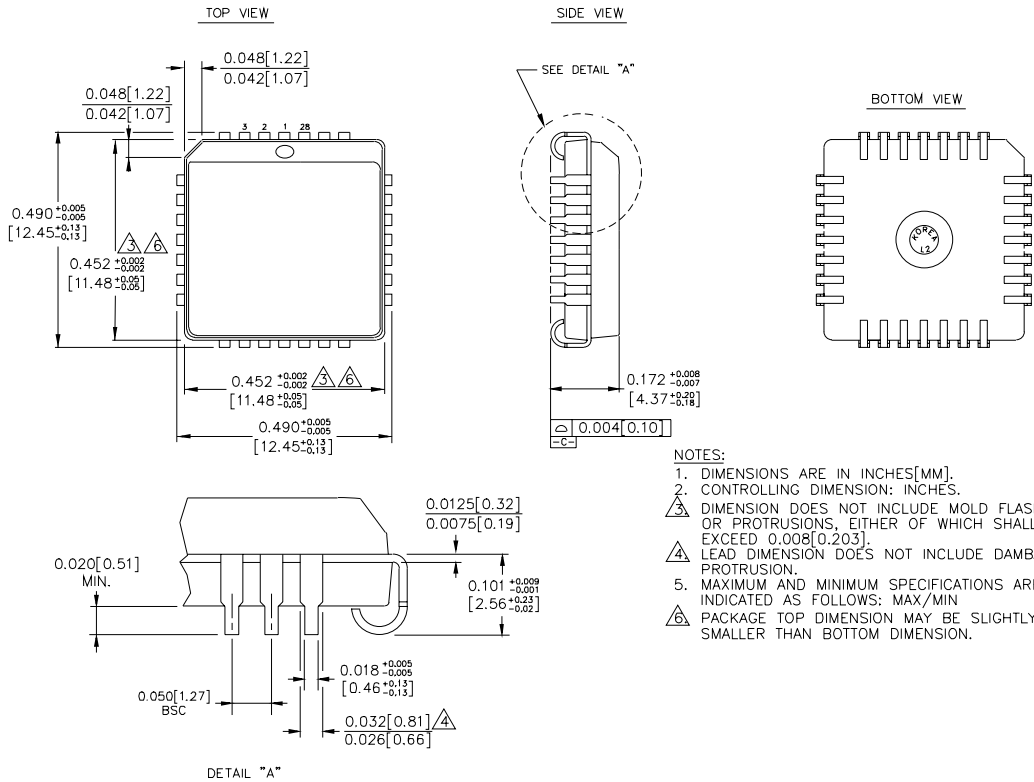
1. Within-device skew is defined as identical transitions on similar paths through a device.

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY10E104JC	J28-1	Commercial
SY10E104JCTR	J28-1	Commercial
SY100E104JC	J28-1	Commercial
SY100E104JCTR	J28-1	Commercial

Ordering Code	Package Type	Operating Range
SY10E104JI	J28-1	Industrial
SY10E104JITR	J28-1	Industrial
SY100E104JI	J28-1	Industrial
SY100E104JITR	J28-1	Industrial

**28 LEAD PLCC (J28-1)**



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
  2. CONTROLLING DIMENSION: INCHES.
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
  4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
  5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
  6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

