



6-BIT 2:1 MUX-REGISTER

SY10E167
SY100E167

FEATURES

- 1000MHz min. operating frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 800ps max. clock to output
- Single-ended outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E167
- Available in 28-pin PLCC package

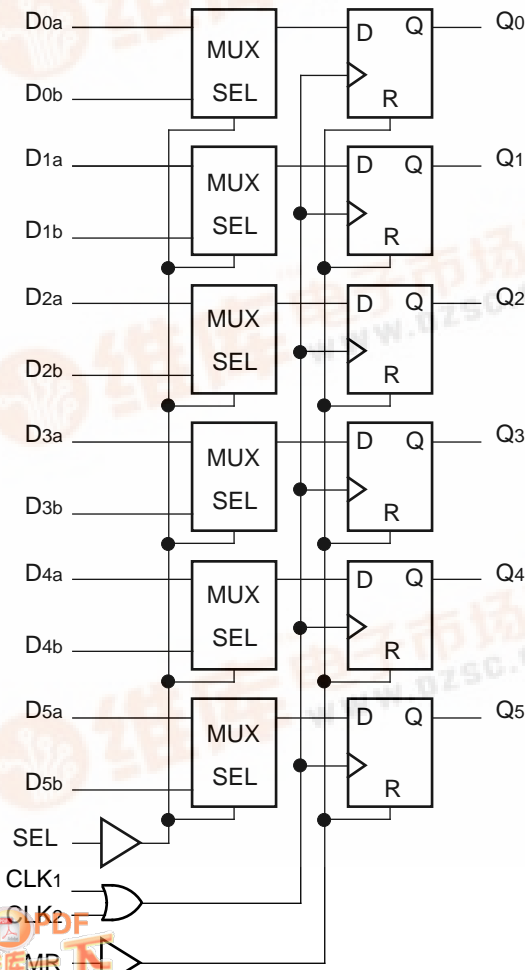
DESCRIPTION

The SY10/100E167 offer six 2:1 multiplexers followed by D flip-flops with single-ended outputs, designed for use in new, high-performance ECL systems. The Select (SEL) control allows one of the two data inputs to the multiplexer to pass through. The two external clock signals (CLK1, CLK2) are gated through a logical OR operation before use as control for the six flip-flops. The selected data are transferred to the flip-flops on the rising edge of CLK1 or CLK2 (or both).

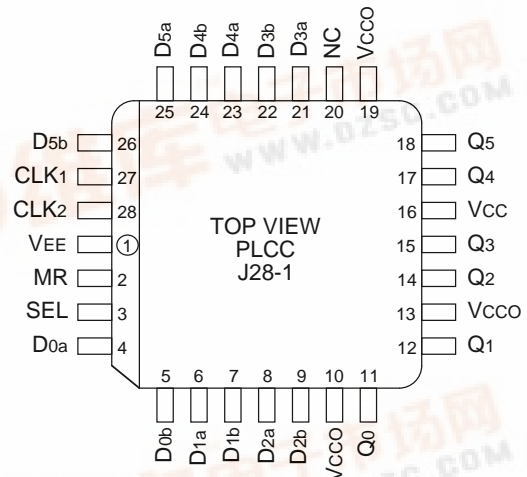
The multiplexer operation is controlled by the Select (SEL) signal which selects one of the two bits of input data at each mux to be passed through.

When a logic HIGH is applied to the Master Reset (MR) signal, it operates asynchronously to take all outputs Q to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0a-D5a	Input Data a
D0b-D5b	Input Data b
SEL	Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q5	Data Outputs
Vcco	Vcc to Output



TRUTH TABLE

SEL	Data
H	a
L	b

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	94	113	—	94	113	—	94	113		
	100E	—	94	113	—	94	113	—	108	130		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{MAX}	Max. Toggle Frequency	1000	1400	—	1000	1400	—	1000	1400	—	MHz	—
t _{PLH} t _{PHL}	Propagation Delay to Output CLK MR	450 450	650 650	800 850	450 450	650 650	800 850	450 450	650 650	800 850	ps	—
t _S	Set-up Time D	100	–50	—	100	–50	—	100	–50	—	ps	—
	SEL	275	125	—	275	125	—	275	125	—		
t _H	Hold Time D	300	50	—	300	50	—	300	50	—	ps	—
	SEL	75	–125	—	75	–125	—	75	–125	—		
t _{RR}	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

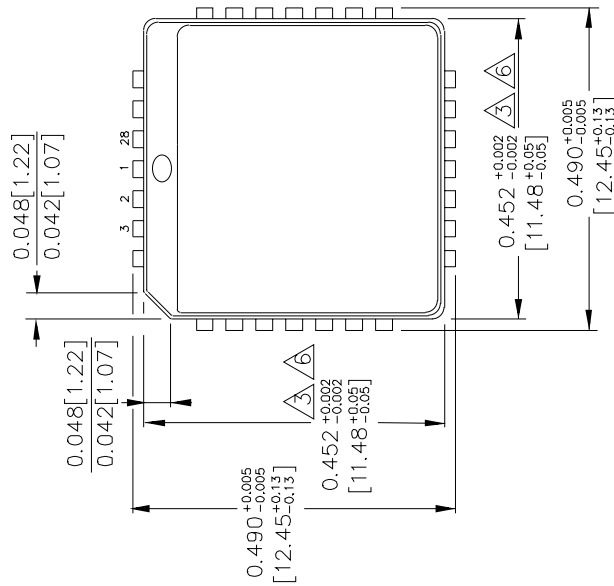
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E167JC	J28-1	Commercial
SY10E167JCTR	J28-1	Commercial
SY100E167JC	J28-1	Commercial
SY100E167JCTR	J28-1	Commercial

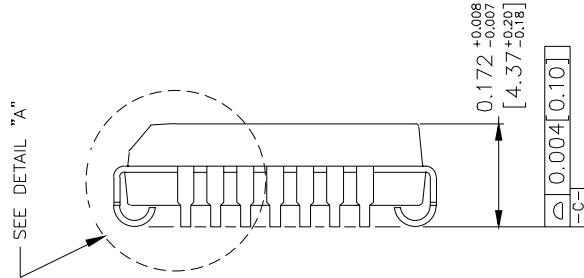
28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT, ADD COVER PAGE TO SPEC, CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25], TYPOGRAPHICAL ERRORS.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12, REFERENCE ANKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

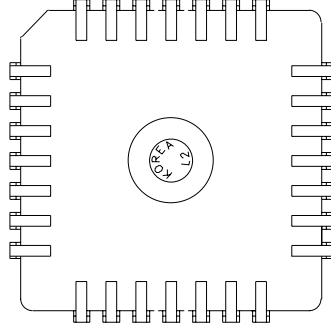
TOP VIEW



SIDE VIEW

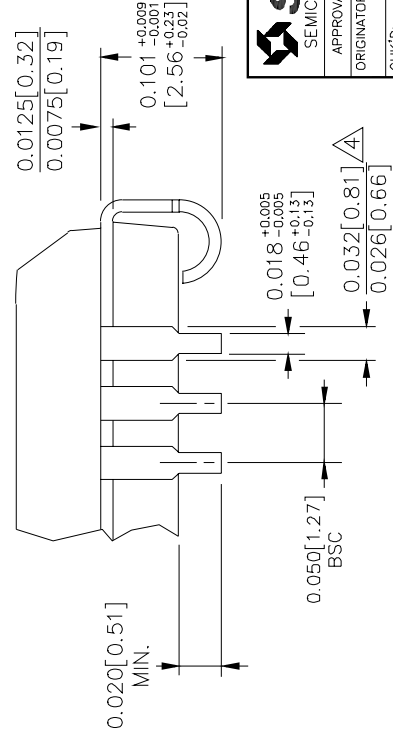


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



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APPROVALS	DATE	APPROVALS	DATE	SIZE	PACKAGE OUTLINE
ORIGINATOR:	02/23/98	QUALITY:		A	28 LEAD PLCC
CHK'D:		DOCUMENT CONTROL:			
RELEASE DATE:					

SCALE: N/A
REVISION: 03

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DETAIL "A"