



6-BIT REGISTER DIFFERENTIAL DATA CLOCK

**SY10E451
SY100E451**

FEATURES

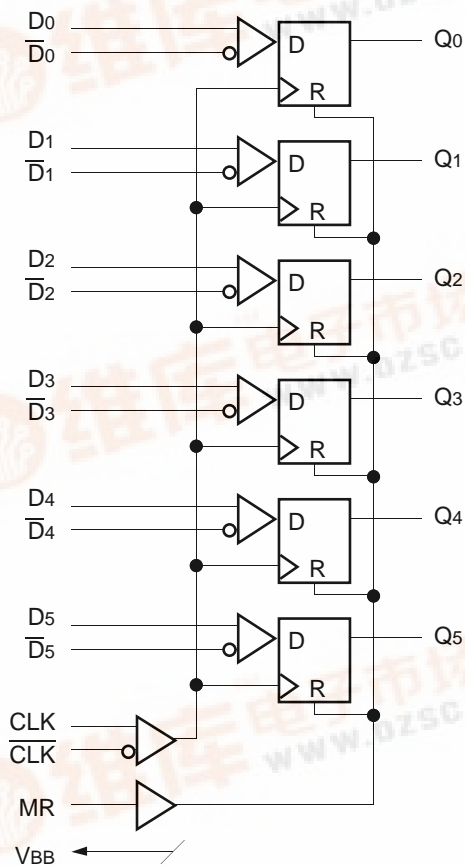
- 1100MHz min. toggle frequency
- Extended 100E VEE range of -4.2V to -5.5V
- Differential inputs: data and clock
- VBB output for single-ended use
- Asynchronous Master Reset
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E451
- Available in 28-pin PLCC package

DESCRIPTION

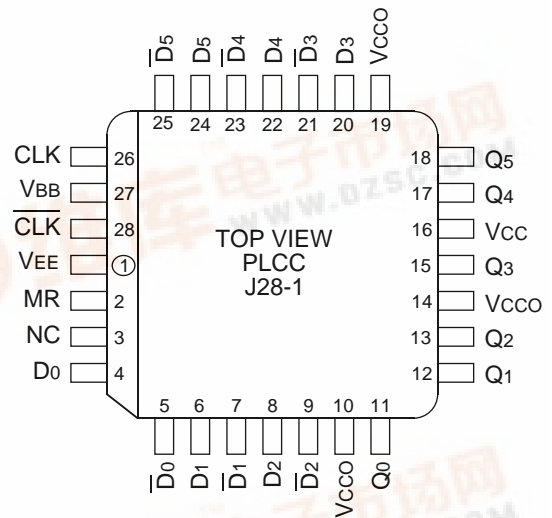
The SY10/100E451 offer six D-type flip-flops with single-ended outputs and differential data and clock inputs, designed for use in new, high-performance ECL systems. The registers are triggered by the rising edge of the CLK input.

A logic HIGH on the Master Reset (MR) input resets all outputs to a logic LOW. The VBB output is provided for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01μF capacitor.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0-D5	+ Data Input
D̄0-D̄5	- Data Input
CLK	+ Clock Input
CLK̄	- Clock Input
MR	Master Reset Input
VBB	VBB Output
Q0-Q5	Data Outputs
VCC0	Vcc to Output



DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = 25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V _{BB}	Output Reference Voltage										V	—
	10E	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19		
	100E	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current										mA	—
	10E	—	84	101	—	84	101	—	84	101		
	100E	—	84	101	—	84	101	—	97	116		
V _{CMR}	Common Mode Range	-2.0	—	-0.4	-2.0	—	-0.4	-2.0	—	-0.4	V	1

NOTE:

- V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PP(min)} and < 1V.

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t _{PLH} t _{PHL}	Propagation Delay to Output CLK (Diff) CLK (SE) MR	475 425 425	650 650 600	800 850 850	475 425 425	650 650 600	800 850 850	475 425 425	650 650 600	800 850 850	ps	—
t _s	Set-up Time, D	150	-100	—	150	-100	—	150	-100	—	ps	—
t _H	Hold Time, D	250	100	—	250	100	—	250	100	—	ps	—
V _{PP (AC)}	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	1
t _{RR}	Reset Recovery Time	750	600	—	750	600	—	750	600	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	2
t _r t _f	Rise/Fall Time 20% to 80%	275	450	800	275	450	800	275	450	800	ps	—

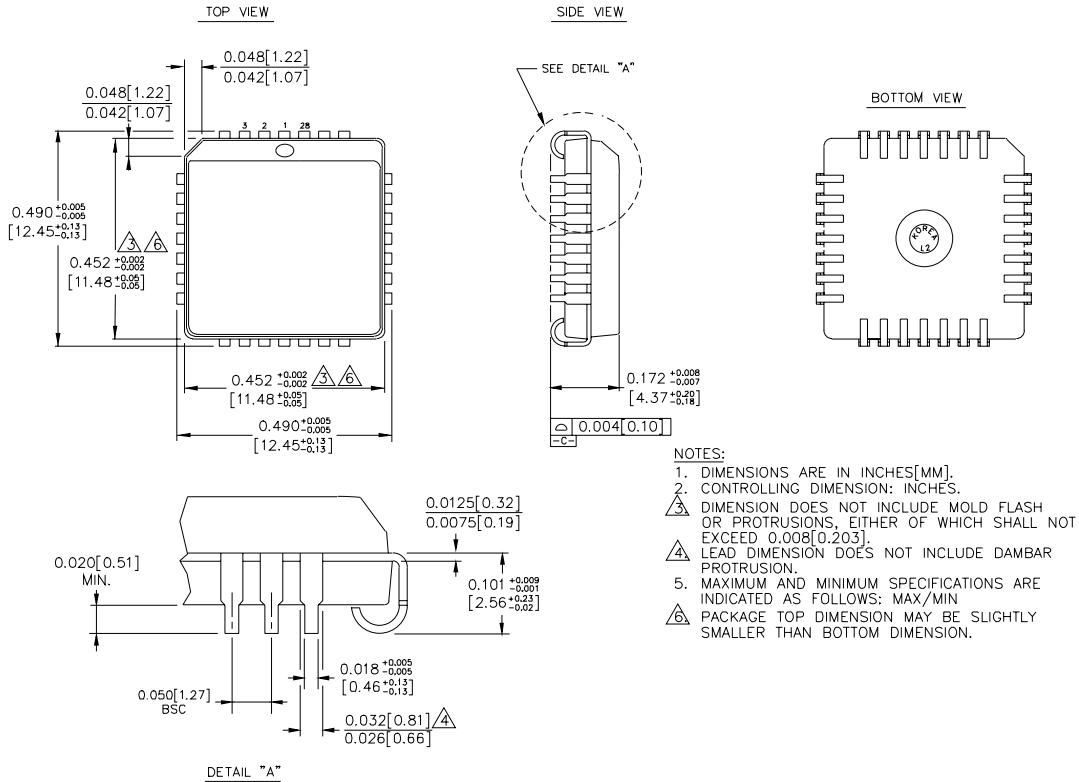
NOTES:

- Minimum input voltage for which AC parameters are guaranteed.
- Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E451JC	J28-1	Commercial
SY10E451JCTR	J28-1	Commercial
SY100E451JC	J28-1	Commercial
SY100E451JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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