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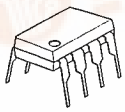
DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM4558/4559 integrated circuit are a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

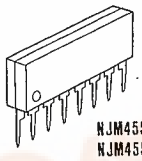
Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

■ PACKAGE OUTLINE



NJM4558D
NJM4559D

NJM4558M
NJM4559M



NJM4558L
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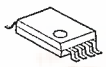
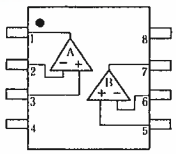


NJM4558V
NJM4559V

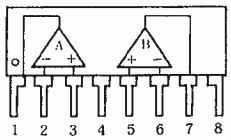
■ FEATURES

- Operating Voltage (±4V～±18V)
- High Voltage Gain (100dB typ.)
- High Input Resistance (5MΩ typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



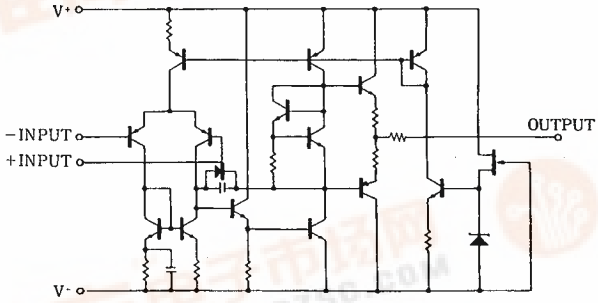
NJM4558D, NJM4558M, NJM4558V
NJM4559D, NJM4559M, NJM4559V



NJM4558L
NJM4559L

PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



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■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+/V^-	±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage	V_{IC}	±15 (note)	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−40～+85	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

(note) For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

■ ELECTRICAL CHARACTERISTICS

(V^+/V^-=±15V Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	$R_S \leqq 10k\Omega$	—	0.5	6	mV
Input Offset Current	I_{IO}		—	5	200	nA
Input Bias Current	I_B		—	25	500	nA
Input Resistance	R_{IN}		0.3	5	—	MΩ
Large Signal Voltage Gain	A_V	$R_L \geqq 2k\Omega$, V_O=±10V	86	100	—	dB
Maximum Output Voltage Swing 1	V_{OM1}	$R_L \geqq 10k\Omega$	±12	±14	—	V
Maximum Output Voltage Swing 2	V_{OM2}	$R_L \geqq 2\Omega$	±10	±13	—	V
Input Common Mode Voltage Range	V_{ICM}		±12	14	—	V
Common Mode Rejection Ratio	CMR	$R_S \leqq 10k\Omega$	70	90	—	dB
Supply Voltage Rejection Ratio	SVR	$R_S \leqq 10k\Omega$	76.5	90	—	dB
Operating Current	I_{CC}		—	3.5	5.7	mA
Slew Rate						
NJM4558	SR		—	1	—	V/μS
NJM4559	SR		—	2	—	V/μS
Equivalent Input Noise Voltage	V_{NI}	RIAA, R_S=1kΩ, 30kHz LPF	—	1.4	—	μVrms
Gain Bandwidth Product	GB					
NJM4558				3		MHz
NJM4559				6		MHz