VFD CONTROLLER DRIVER

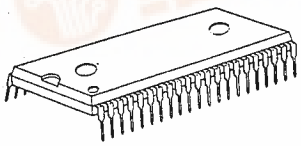
■ GENERAL DESCRIPTION

The NJU3421A is a VFD (Vacuum Fluorescent Display) Controller Driver with key scan function.

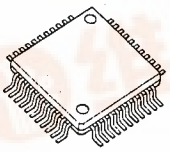
It contains display data RAM, address counter, command register, high voltage drivers, and serial interface circuit.

The display data, the command data and the key scanning data can be transmitted with the serial interface circuit, and VFD driving voltage can operate up to 45V. The NJU3421A is useful for car audio, VCR and other VFD application items.

■ PACKAGE OUTLINE



NJU3421AL

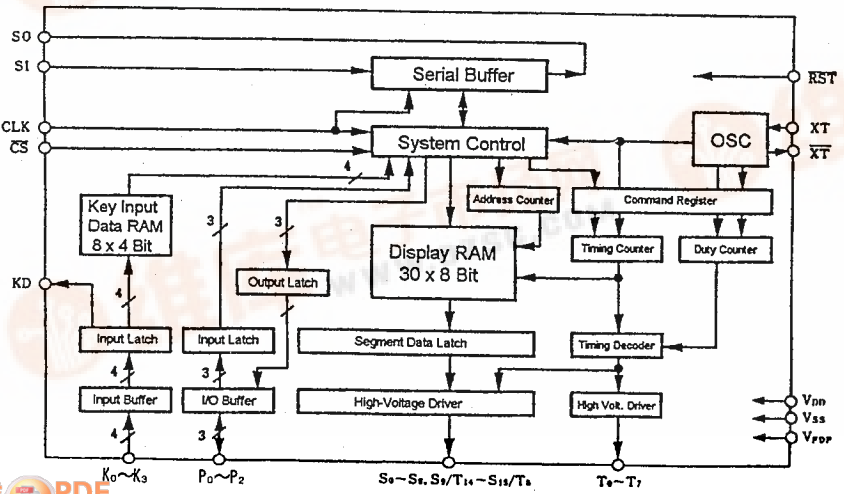


NJU3421AF

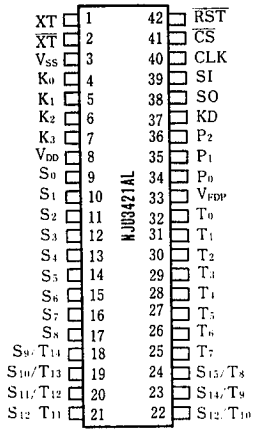
■ FEATURES

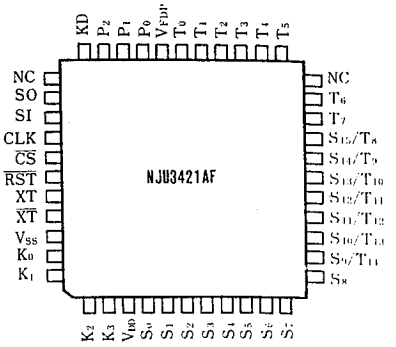
- VFD Driving Voltage | V_{DD}-V_{FDP} | ≦45V
- Display Mode 9 Segments Display × 15 Digits
  16 Segments Display × 8 Digits
- Serial Interface
- Display ON/OFF Function
- Key Scan Function 8 × 4 Keys max.
- Display Data RAM 30 × 8 Bits
- key Input Data RAM 8 × 4 Bits
- Key Input Detecting Function
- High Driving Current(I/O Ports)Io=10mA max.
- Oscillation Circuit on-chip
- Power On Initialization
- Operating Voltage 5V±10%
- Package Outline SDIP 42 / QFP 44-A1
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION





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■ TERMINAL DESCRIPTION

NO.		SYMBOL	FUNCTION
SDIP42	QFP44-A1		
8 3 33	3 42 29	V_{DD} V_{SS} V_{FDP}	POWER SOURCE GND VFD Driving Voltage
1, 2	40, 41	XT, $\overline{XT}$	Oscillation Terminals. For external clock operation, The clock should be input on XT terminal.
4～7	43, 44, 1, 2	K_0～K_3	Key Input Terminals(Pull-Down Resistance)
37	33	KD	Key Input Detecting Terminal. When key input, "H" level is output from this terminal.
9～17 18～24 25～32	4～12 13～19 20, 21, 23～28	S_0～S_8 S_9/T_{14}～S_{15}/T_8 T_7～T_0	Segment Output Terminals(Pull-Down Resistance) Segment/Timing Output Terminals(Pull-Down Resistance) Timing Output Terminals(Pull-Down Resistance)
42	39	$\overline{RST}$	Reset Terminal(Pull-UP Resistance) "L":Reset
34～36	30～32	P_0～P_2	I/O Ports (Pull-Up Resistance) Output:High current Output(LED Display is available) Input:Available by all "H" output setting.
38	35	SO	Serial Data Output Terminal. The key scan data or the I/O port output data is output.
39	36	SI	Serial Data (Address, I/O Ports, Command, Display) input Terminal.
40	37	CLK	Shift Clock Input Terminal.
41	38	$\overline{CS}$	Chip Select Input Terminal. "L":Activated.
-	22, 34	NC	Non Connection.

■ FUNCTION DESCRIPTION

(1) Address Counter

The address counter addresses the display data RAM which data are sent by the serial data transmission. When the first word of the serial data is recognized as the address of the display data RAM (The upper two bits of a byte must be "00" .) , the lower 5bits are set up into the address counter as the address of the display data RAM. The data of the display data RAM which are input sequentially are set into the specified address and the address counter increments.

Though the address counter consists of the 5-bit counter, the effective range is from "00000" (00_H) to "11101" ($1D_H$) and the invalid range is from "11110" ($1E_H$) and "11111" ($1F_H$). The address of "11111"($1F_H$) is incremented to "00000"(00_H).

The Address Data

B7	B6	B5	B4	B3	B2	B1	B0
0	0	*	AD4	AD3	AD2	AD1	AD0

* : Don't care

Recognization bits

The address of the display data RAM

The mapping of the display data RAM

	B7	B6	B5	B4	B3	B2	B1	B0		B7	B6	B5	B4	B3	B2	B1	B0	
00_H									01_H									T_0
02_H									03_H									T_1
04_H									05_H									T_2
06_H									07_H									T_3
08_H									09_H									T_4
$0A_H$									$0B_H$									T_5
$0C_H$									$0D_H$									T_6
$0E_H$									$0F_H$									T_7
10_H									11_H									T_8
12_H									13_H									T_9
14_H									15_H									T_{10}
16_H									17_H									T_{11}
18_H									19_H									T_{12}
$1A_H$									$1B_H$									T_{13}
$1C_H$									$1D_H$									T_{14}
$1E_H$	*	*	*	*	*	*	*	*	$1F_H$	*	*	*	*	*	*	*	*	T_{15}
	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0		S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	

[*] Don't Care

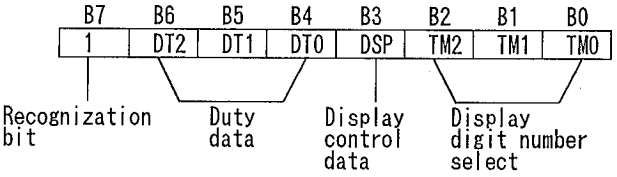
(2) COMMAND REGISTER

The Command Register is the register for setting the status of Display Duty, Display Digit Number and Display ON/OFF.

When the first word of serial transmmitted data is recognized as the command data (The upper one bit of a byte must be "1".), the lower 7 bits are set into the command register. After the command data are received the timing counter is initialized and then the input command is executed. During the initialization of the timing counter and the command execution, the display can be off. Therefore ,the frequent command transmission causes the flicker of the display.

The default status of the display mode is display-off by the power on initialization function.

The command data



(2-1) Duty set

DT2	DT1	DT0	Timing signal Duty
0	0	0	2/16
0	0	1	4/16
0	1	0	6/16
0	1	1	8/16
1	0	0	10/16
1	0	1	12/16
1	1	0	14/16
1	1	1	15/16

(2-2) Display contorol set

DSP	Display
0	OFF
1	ON

(2-3) Display digit number set

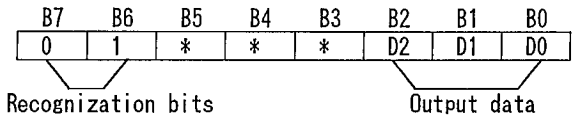
TM2	TM1	TM0	Digits
0	0	0	8
0	0	1	9
0	1	0	10
0	1	1	11
1	0	0	12
1	0	1	13
1	1	0	14
1	1	1	15

(3) I/O Port

The NJU3421A incorporates three I/O ports. As the output type of these three ports is the constructed by the N-channel and open-drain type FET of the low on-resistance and the pull-up resistor , the output driver can drive the LED. When "H" level is set with the I/O port output data, these I/O ports can be used as the input mode.

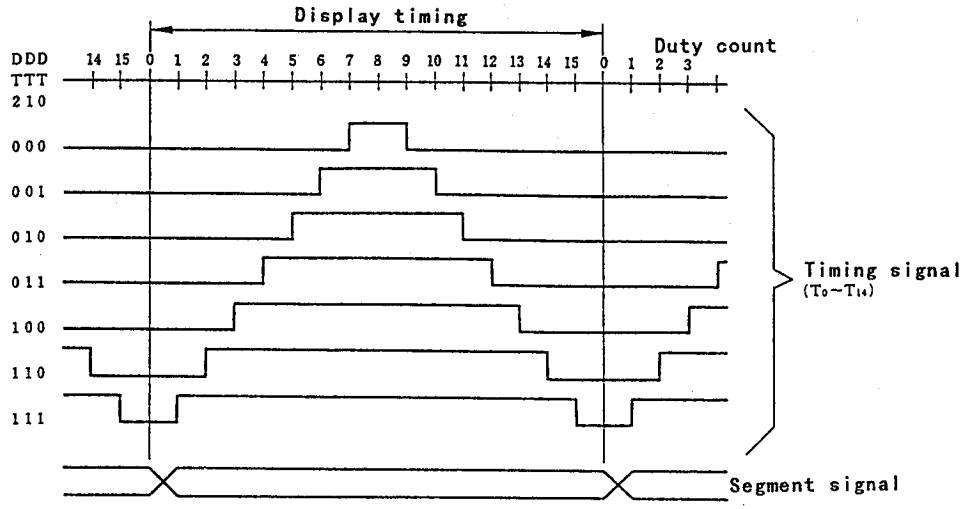
When the first word of serial data is recognized as the I/O port output data (the upper two bits of a byte must be "01"),The status of the data of the lower three bits are output from the I/O port.

The I/O port output data

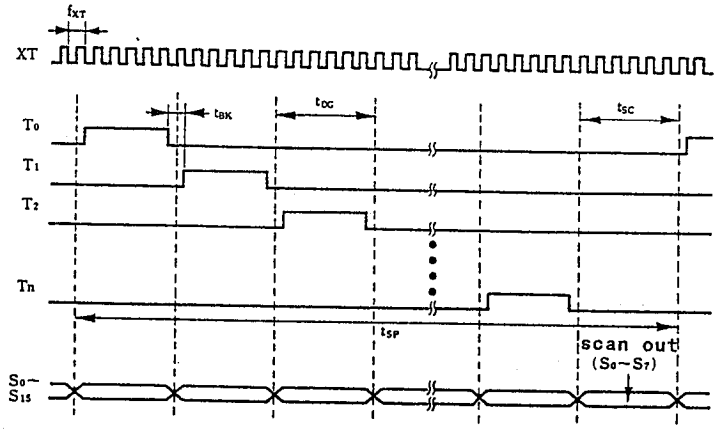


* : Don't care

■ TIMING SIGNAL / DUTY CHANGE WAVEFORM



■ DISPLAY TIMING CHART



Oscillation frequency	:	f_{XT}
Minimum blanking time (Duty 15/16)	:	$t_{BK} = (1/f_{XT}) \times 96$
1character display time	:	$t_{DG} = t_{BK} \times 16$
key scanning time	:	$t_{SC} = t_{DG}$
1cycle display time	:	$t_{SP} = t_{DG} \times$ character $+ t_{SC}$

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(4) KEY INPUT CIRCUIT

The key input circuit is constructed with the key scanning outputs (8 outputs) which are appropriated from the segment output (S_0 to S_7) for the display , the key input terminals (4 terminals) and the key switches as shown below. When the key scanning signal is output during the key pushed , the key input terminal receives the same level ("H") of the key scanning signal. If the keys are not pushed , the key input terminal receives "L" level at any time because of its pull-down resistor.

The received key data are stored in the key data RAM in sequence and the data can be get by the serial data transmmition .

The key input detecting function lets the key input detecting output terminal goes to "H" level when any key pushes. The "H" level output of the key input detecting output terminal is continued during the key pushed.

(4-1) Key condition vs Key input terminal level

key condition	input level
key pushed	"H"
not key pushed	"L"

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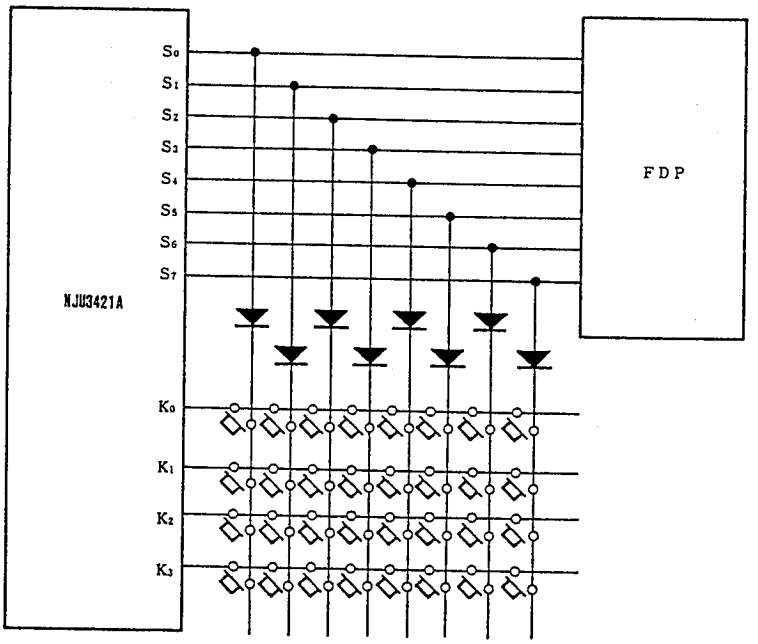
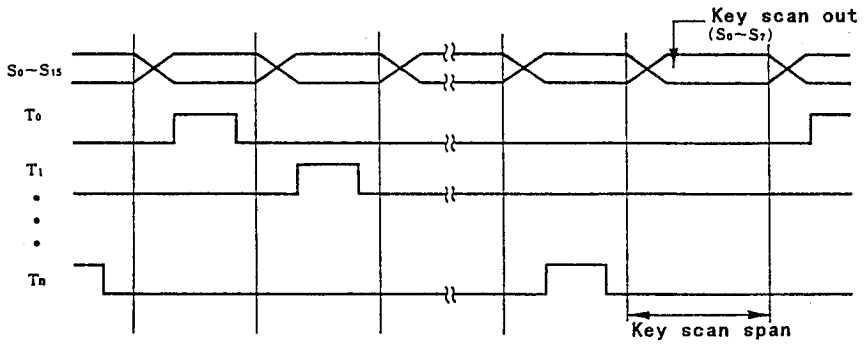
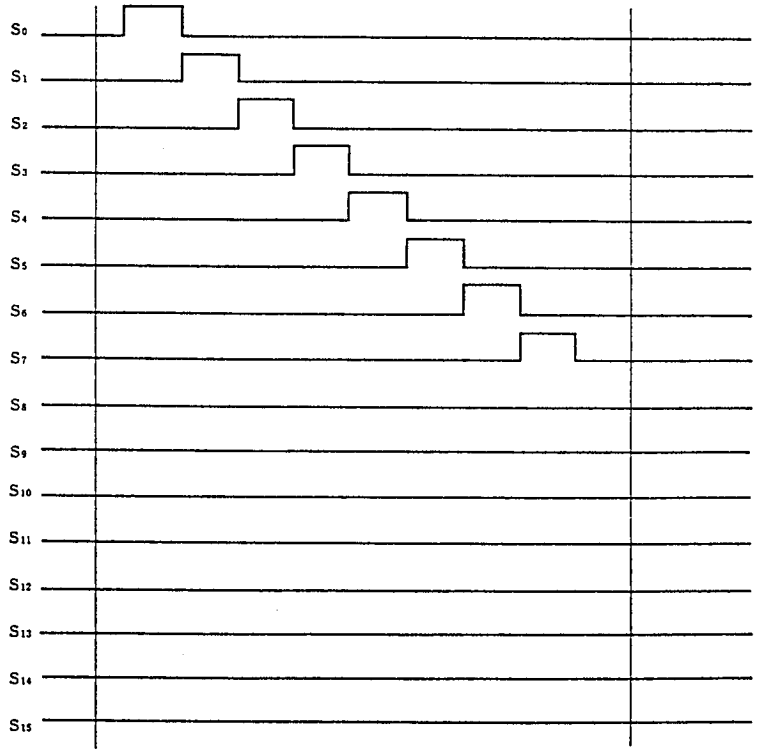


key matrix

■ FDP DISPLAY OUTPUT WAVEFORM



■ ENLARGED KEY SCAN SPAN



(5) SERIAL DATA TRANSMISSION

The data transmission with the external can be executed by the serial interface circuit only. This interface circuit requires the external shift clock input and can execute the bi-direction (input/output) action synchronously as shown below.

The serial data are grouped at a word which equalles to a byte (8 bits) for this device. The serial interface circuit is activated when the CS terminal is set to "L" level. While the CS is "L", the words of the serial data are able to transmitted using the shift clock (the CLK terminal) and the serial data input or output (the SI or SO terminal) synchronously.

On the data input status, the first transmitted word must be the address, the command or the I/O port output data. When the first word is the address data, the following words should be the display data. When the first word is the command or I/O port output data, the following words, if transmitted, are ineffective.

On the data output status, the transmitted word incorporates the key data corresponding to the lower 4 bits and the I/O port input data corresponding to the upper 4 bits (The MSB is invalid). The key data of the first word means the data by scanning the S_0, these of the second word means the data by scanning the S_1, ... finally, these of the 8th word means the data by scanning the S_7. The I/O port input data means the last status data. For getting all key matrix data (8 x 4 max.), the data transmission of the 8 words is required.

After the key data transmission is ignored at less than 8 words, the next key data transmission is reset to the first (S_0 scanning) word.

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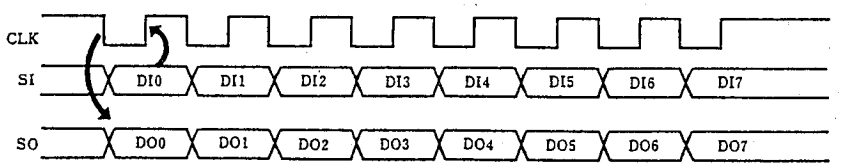
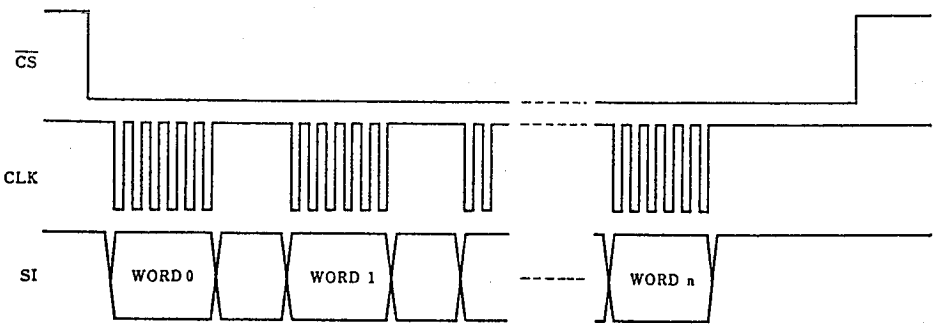
■ CLK and SI/SO TIMING CHART



Serial buffer shift timing

■ SERIAL TRANSMISSION FORMAT



(5-1) SERIAL INPUT DATA

The address data

B7	B6	B5	B4	B3	B2	B1	B0	
0	0	*	AD4	AD3	AD2	AD1	AD0	* : Don't care

WORD 0

The command data

B7	B6	B5	B4	B3	B2	B1	B0
1	DT2	DT1	DT0	DSP	TM2	TM1	TM0

The I/O port output data

B7	B6	B5	B4	B3	B2	B1	B0	
0	1	*	*	*	D2	D1	D0	* : Don't care

WORD 1～n Display data are required when WORD 0 = address data
Any data are become ineffective when WORD 0 = not address data

(5-2) SERIAL OUTPUT DATA

Serial output data

	B7	B6	B5	B4	B3	B2	B1	B0	
WORD 0～7	*	P2	P1	P0	K3	K2	K1	K0	* : Don't care

(Key scanning data:S_0～S_7)

WORD 8～n Ineffective data

■ **ABSOLUTE MAXIMUM RATINGS**

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	CONDITIONS	UNIT
Operating Voltage	V_{DD}	-0.3 ～ +7.0		V
Input Voltage	V_{IN}	-0.3 ～ V_{DD}+0.3		V
Output Voltage	V_{OUT}	-0.3 ～ V_{DD}+0.3		V
VFD Driving Voltage	V_{FDP}	V_{DD}-45～V_{DD}+0.3		V
"H" level Output Current	I_{OH}	-5	For a terminal except the display terminals	mA
	I_{ODH1}	-15	For a terminal, S_0～S_7 Terminals only	
	I_{ODH2}	-35	For a terminal, T_0～T_7, S_8/T_{15}～S_{15}/T_8 Terminals only	
"H" level Total Output Current	ΣI_{OH}	-40	Sum of the output terminal except the display Terminals	mA
	ΣI_{ODH}	-100	Sum of the Display Terminals	
"L" level Output Current	I_{OLC}	20	For a terminal, P_0～P_1 Terminals only	mA
"L" level Total Output Current	ΣI_{OL}	100	Sum of the Output terminals	mA
Power Dissipation	P_D	SDIP:250 QFP:300		mW
Operating Temperature Range	Topr	-30 ～ +80		°C
Storage Temperature Range	Tstg	-55 ～ +125		°C

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■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}	V_{DD} Terminal	4.5		5.5	V
"H" Level Input Voltage	V_{IH1}	XT, $\overline{RST}$, $\overline{CS}$, SI, CLK, P_0~P_2 Terminals	0.8V_{DD}			V
	V_{IH2}	K_0~K_3 Terminals	0.4V_{DD}			V
"L" Level Input Voltage	V_{IL1}	XT, $\overline{RST}$, $\overline{CS}$, SI, CLK, P_0~P_2 Terminals			0.2V_{DD}	V
	V_{IL2}	K_0~K_3 Terminals			0.16V_{DD}	V
"H" Level Output Voltage	V_{OH1}	KD, SO Terminals V_{DD}=4.5V, I_{OH1}=-0.5mA	4.0			V
	V_{OH2}	KD, SO Terminals V_{DD}=4.5V, I_{OH2}=-1.2mA	3.5			
"L" Level Output Voltage	V_{OL1}	KD, SO Terminals V_{DD}=4.5V, I_{OL1}=+1.8mA			0.4	V
	V_{OL2}	KD, SO Terminals V_{DD}=4.5V, I_{OL2}=+3.6mA			0.6	
	V_{OL3}	P_0~P_2 Terminals V_{DD}=4.5V, I_{OL3}=+10mA			0.4	
Input Off Leak Current	I_{IZ}	$\overline{CS}$, CLK, SI Terminals V_{DD}=5.5V, V_I=0 or 5.5V			±1	uA
Display Output Current	I_{OH}	S_0~S_8 Terminals V_{DD}=4.5V, V_{OH}=V_{DD}-2.5V	-7			mA
		S_9/T_{14}~S_{15}/T_8, T_0~T_7 Term. V_{DD}=4.5V, V_{OH}=V_{DD}-2.5V	-15			
Pull-Up Resistance	R_{UR}	$\overline{RST}$ Terminal V_{DD}=5.0V, V_I=V_{SS}	140		260	kΩ
	R_{UP}	P_0~P_2 Terminals V_{DD}=5.0V, V_I=V_{SS}	10		20	
Pull-Down resistance	R_{DK}	K_0~K_3 Terminals V_{DD}=5.0V, V_I=V_{SS}	20		50	kΩ
	R_{DST}	S_0~S_8, S_9/T_{14}~S_{15}/T_8, T_0~T_7 V_{DD}=5.0V, V_O=V_{SS}, V_{FDP}=V_{DD}-40V	70		200	
Logic Operating Current	I_{DD1}	V_{SS} Terminal, V_{DD}=5.0V, 4MHz Ceramic resonator, C_1=C_2=27pF Output Open, All Segment or Timing Output is OFF		1	2	mA
Display Operating Current	I_{DD2}	V_{FDP} Terminal, V_{DD}=5.0V, Output Open except S0~S8, T0~T7 S_9/T_{14}~S_{15}/T_8 All Segment or Timing Output is ON		7	10	mA

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■ AC Characteristics

(Ta=25°C, V_{DD}=5V±10%, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillation Frequency External Clock Input	f_{XT} f_{CL}	Fig. 1	1	4	5	MHz
External Clock Rise Time	t_{CLH}				20	ns
External Clock Fall Time	t_{CLL}				20	ns
Serial Input Setup Time	t_{SIS}	Fig. 2	60			ns
Serial Input Hold Time	t_{SIH}		10			ns
Serial Output Delay Time	t_{SOD}	Fig. 2, Load=50pF			120	ns
Shift Clock Frequency	f_{CLK}	Fig. 3			$f_{XT}/3$	MHz
Shift Clock Interval Time	t_{CLK}		10			us
Minimum Blanking Time	t_{BK}	Fig. 4, @f_{XT}=4MHz	20		30	us
"L" level Time	t_{KSL}	Fig. 5, @f_{XT}=4MHz, Key scan	20			us
"H" level Time	t_{KSH}		20		30	us
Power Rise Time	t_R	Fig. 6	0.05		50	ms
Reset Pulse Width	t_{RST}		10			us

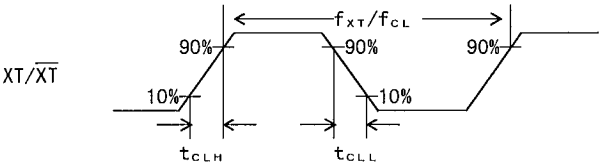

Fig. 1

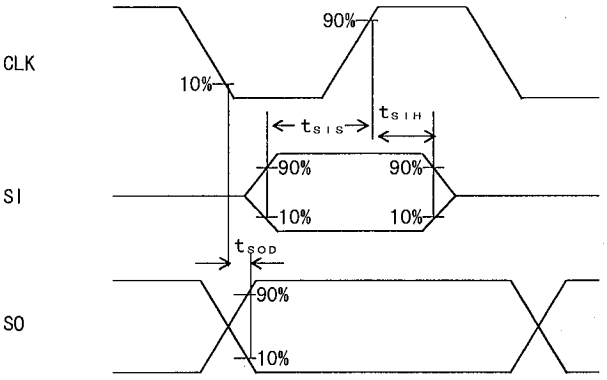

Fig. 2

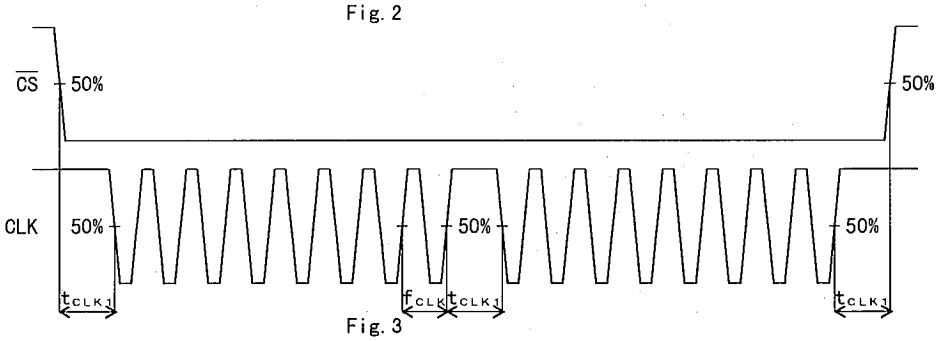

Fig. 3

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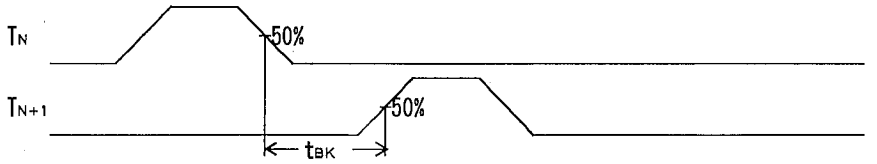

FIG.4

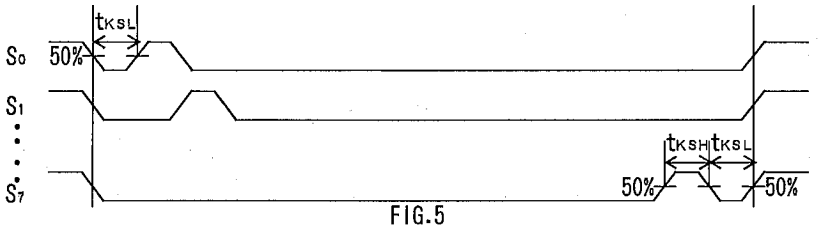

FIG.5

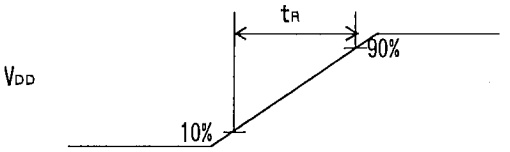

FIG.6

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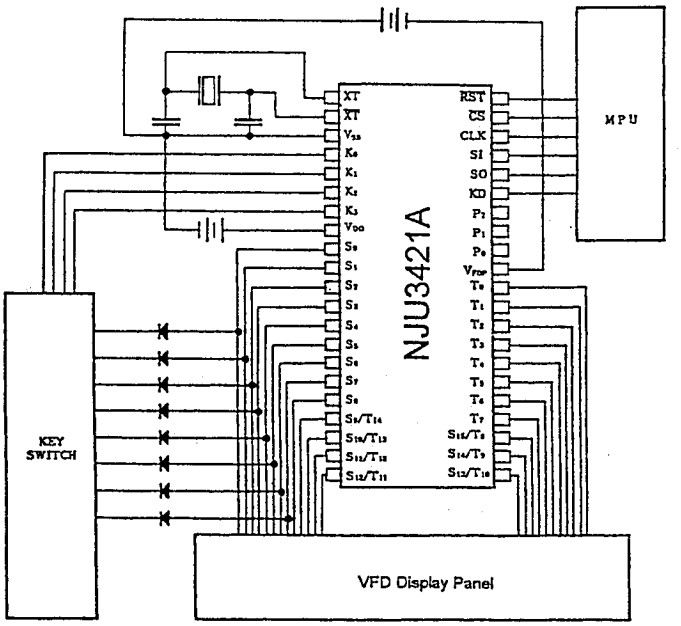
■ APPLICATION CIRCUIT



MEMO