



**NJU7042**

## INPUT/OUTPUT FULL-SWING TINY SINGLE C-MOS OPERATIONAL AMPLIFIER

### ■GENERAL DESCRIPTION

The **NJU7042** is a single C-MOS operational amplifier permitting input and output in full swing.

The operating voltage is 2.7V to 5.5V and the input and output stage permits signal to swing between both of the supply rails.

The input offset voltage is lower than 5mV, and the input bias current is as low as than 1pA, consequently very small signal around the ground level can be amplified.

Furthermore, The **NJU7042** is packaged with very small MTP-5, therefore it can be especially applied to portable items.

### ■PACKAGE INFORMATION



NJU7042F

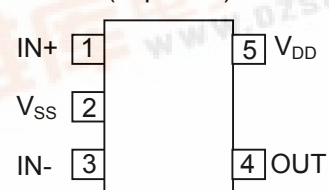
### ■FEATURES

- Input Full-Swing
- Output Full-Swing
- Low Input Offset Voltage
- Single-Power-Supply
- Low Operating Current
- High Load Current
- Low Bias Current
- Compensation Capacitor Incorporated
- Package Outline MTP-5
- C-MOS Technology

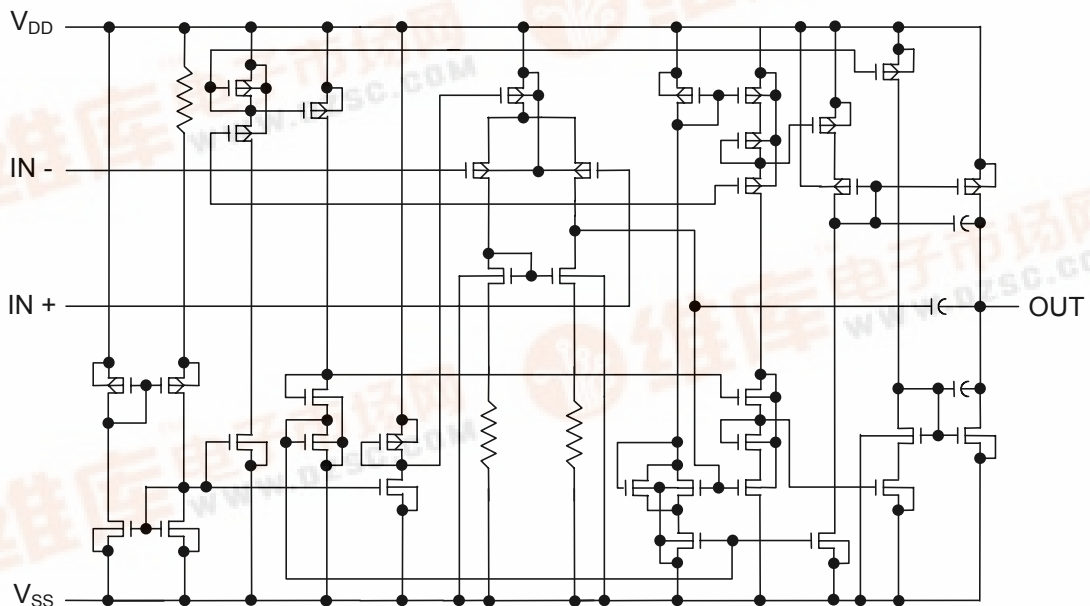
$V_{IN}=V_{SS}$  to  $V_{DD}$   
 $V_{OM} \geq 2.7V$  min  
 $V_{IO}=5mV$  max  
 $V_{DD}=2.7$  to  $5.5V$   
 $I_{DD}=15\mu A$  typ  
 $I_{OH}/I_{OL}=200\mu A$  typ  
 $I_{IB}=1pA$  typ  
 MTP-5

### ■PIN CONFIGURATION

(Top View)



### ■EQUIVALENT CIRCUIT



## ■ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{DD}$	7.0	V
Differential Input Voltage	$V_{ID}$	$\pm 7.0$ (Note1)	V
Common Mode Input Voltage	$V_{IC}$	-0.3~7.0	V
Power Dissipation	$P_D$	200	mW
Operating Temperature	$T_{opr}$	-40~+85	°C
Storage Temperature	$T_{stg}$	-55~+125	°C

Note1) If the supply voltage ( $V_{DD}$ ) is less than 7.0V, the input voltage must not over the  $V_{DD}$  level though 7.0V is limit specified.

Note2) Decoupling capacitor should be connected between  $V_{DD}$  and  $V_{SS}$  due to the stabilized operation for the circuit.

## ■ELECTRICAL CHARACTERISTICS

( $V_{DD}=3.0V, R_L=\infty, T_a=25^\circ C$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	$V_{DD}$		2.7	-	5.5	V
Input Offset Voltage	$V_{IO}$	$V_{IN}=V_{DD}/2$	-	-	5	mV
Input Offset Current	$I_{IO}$		-	1	-	pA
Input Bias Current	$I_{IB}$		-	1	-	pA
Input Impedance	$R_{IN}$		-	1	-	TΩ
Large Signal Voltage Gain	$A_{VD}$		60	70	-	dB
Input Common Mode Voltage Range	$V_{ICM}$		$V_{SS}$ to $V_{DD}$	-	-	V
Maximum Output Swing Voltage	$V_{OM1}$	$R_L=30k\Omega$	$V_{DD}-0.3$	-	-	V
	$V_{OM2}$	$R_L=30k\Omega$	-	-	$V_{SS}+0.3$	
Output Source Current	$I_{OH}$	$V_{OH}=V_{DD}-0.3$	100	200	-	uA
Output Sink Current	$I_{OH}$	$V_{OL}=V_{DD}+0.3$	100	200	-	
Common Mode Rejection Ratio	CMR	$V_{IN}=V_{DD}/2$	60	70	-	dB
Supply Voltage Rejection Ratio	SVR	$V_{DD}=2.7\sim 5.5V$	60	70	-	dB
Operating Current	$I_{DD}$		-	15	30	uA
Slew Rate	SR		-	0.03	-	V/us
Unity Gain Bandwidth	Ft	$A_V=40dB, C_L=10pF$	-	47	-	kHz

Note3) The load capacitance (CL) should be used less than 200pF

### [CAUTION]

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