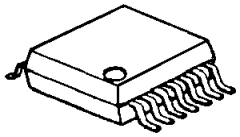
2V Operation Switching Driver for Class D Amplifier

■ GENERAL DESCRIPTION

The **NJU8713** is a Switching Driver for a class D Amplifier including Separated Power Source terminals between Input and Output, BEEP and BPZ (Bipolar Zero) output circuits. It converts 1bit digital signal input, such as PWM or PDM signal, to an analog signal output through a simple external LC low-pass filter.

The **NJU8713** realizes very high power-efficiency because of the class D operation. Therefore, it is suitable for portable audio set and others.

■ PACKAGE OUTLINE

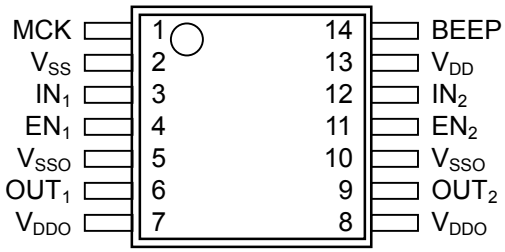


NJU8713V

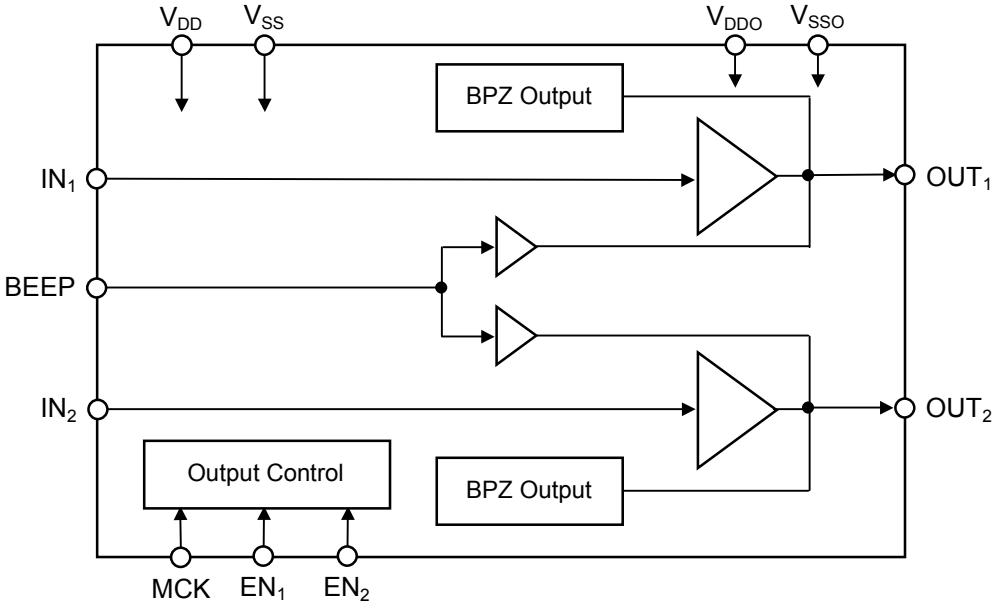
■ FEATURES

- 2-channel 1bit Audio Signal Input
- Standby(Hi-Z), BPZ Control
- Internal BPZ Charger
- Beep Function
- Operating Voltage : 1.7V to 2.7V
- Driving Voltage : 1.7V to V_{DD}
- CMOS Technology
- Package Outline : SSOP14

■ PIN CONFIGURATION



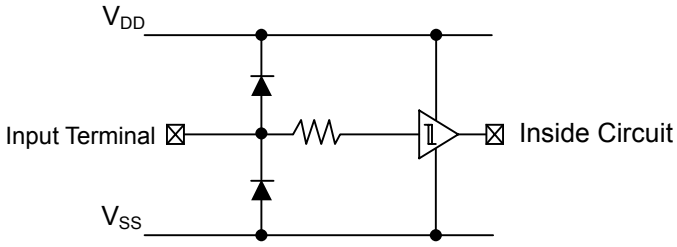
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
13	V_{DD}	-	Operation Power Supply, V_{DD}=2V
2	V_{SS}	-	Operation Power GND, V_{SS}=0V
7 8	V_{DDO}	-	Driving Power Supply, V_{DDO}=2V Terminal No.7 and No.8 should be connected to the same electric potential.
5 10	V_{SSO}	-	Driving Power GND, V_{SSO}=0V Terminal No.5 and No.10 should be connected to the same electric potential.
1	MCK	I	Master Clock Input Terminal The condition of the data input terminal is fetched with the rising edge of this signal.
4 11	EN_1 EN_2	I	Output Control Terminal Output circuit is selected by the condition of this terminal.
3 12	IN_1 IN_2	I	Audio Signal Input Terminal 1-bit Audio Signal inputs into this terminal.
14	BEEP	I	Beep Signal Input Terminal Beep signal inputs into this terminal.
6 9	OUT_1 OUT_2	O	Output Terminal • When Output Terminal selects Audio Signal, IN_1 terminal input data outputs from OUT_1 terminal and IN_2 terminal input data outputs from OUT_2 terminal. • When Output Terminal selects Beep Signal, BEEP terminal input data outputs from OUT_1 and OUT_2 terminals.

■ INPUT TERMINAL STRUCTURE



■ FUNCTIONAL DESCRIPTION

(1) Signal Output

PWM signals of L channel and R output from OUT_1 and OUT_2 terminals respectively. These signals are converted to analog signal by external 2nd-order or over LC filter. The output driver power supplied from V_{DDO} and V_{SSO} are required high response power supply against voltage fluctuation like as switching regulator because Output T.H.D is effected by power supply stability.

(2) Master Clock

Master clock (MCK) synchronizes the Audio signal inputs (IN_1 and IN_2). The setup time and the hold time should be kept in the AC characteristics because IN_1 and IN_2 are fetched with the rising edge of MCK. MCK requires jitter-free or jitter as small as possible because the jitter downs S/N ratio.

OUT_1 and OUT_2 occur the pop noise when MCK is stopped in operation without standby mode. Therefore, the standby mode should be set before MCK stop.

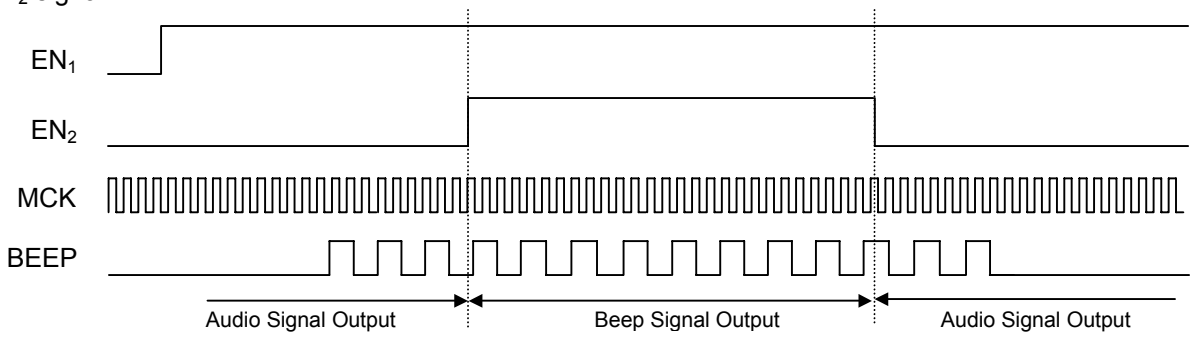
(3) Output Control

Output circuit is selected by the conditions of EN_1 and EN_2 terminals.

EN_2	EN_1	Output State of OUT_1 & OUT_2
0	0	Standby(High impedance)
0	1	Audio Signal Output
1	0	BPZ Output
1	1	Beep Signal Output

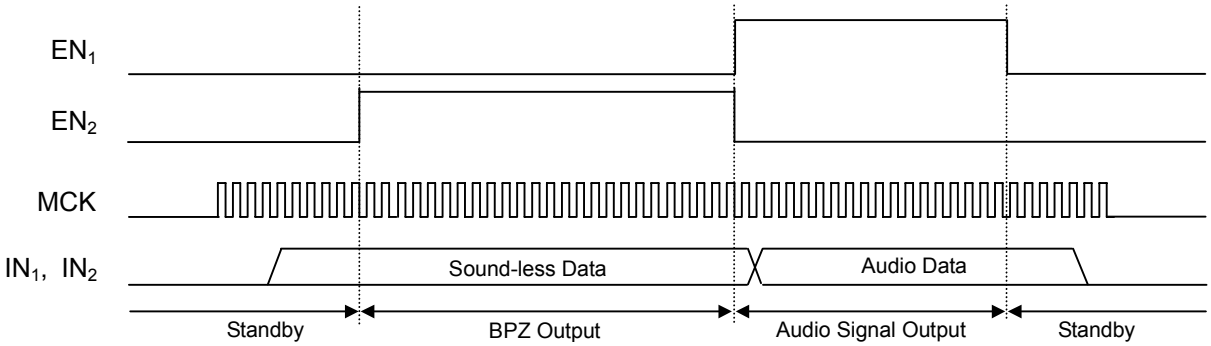
(4) Beep Function

The beep signal must be input before the rising edge of EN_2 signal and must be stopped after the falling edge of EN_2 signal.



(5) BPZ Function

BPZ Function operates to charge the external AC coupling capacitor for the BPZ level which is a point of the analog signal common. Be sure to input sound-less data to IN_1 and IN_2 in busy of the BPZ function. At this time, the sound-less signal must be input before the rising edge of EN_2 signal and must be continue after the falling edge of EN_2 signal. The charging time is in proportion to the capacity value of the external AC coupling capacitor.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Operation Supply Voltage		V_{DD}	-0.3 to +4.0	V
Driving Supply Voltage		V_{DDO}	-0.3 to +2.7	V
Input Voltage		Vin	-0.3 to V_{DD}+0.3	V
Operating Temperature		Topr	-40 to +85	°C
Storage Temperature		Tstg	-40 to +125	°C
Power Dissipation	SSOP14	P_D	300	mW
Power Supply Voltage Condition		-	$V_{DD} \geq V_{DDO}$	V

Note 1) All voltage values are specified as V_{SS}=V_{SSO}=0V.
Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.
Note 3) Decoupling capacitors should be connected between V_{DD}-V_{SS} and V_{DDO}-V_{SSO} due to the stabilized operation.

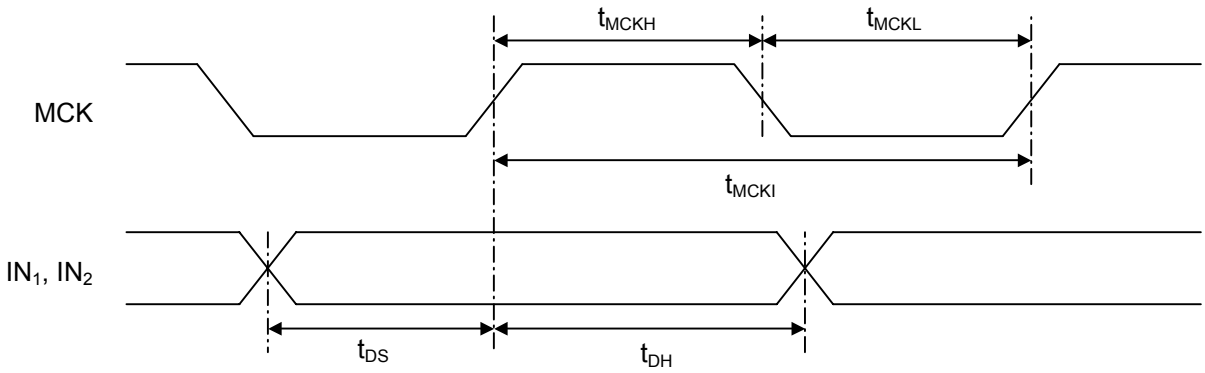
■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=V_{SSO}=0.0V, Load Impedance=32Ω, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} Supply Voltage	V_{DD}		1.7	2.0	2.7	V
V_{DDO} Supply Voltage	V_{DDO}		1.7	2.0	V_{DD}	V
BPZ Driving Voltage	V_{BPZ}	load operating MCK=256f_S IN_1, IN_2=32f_S Duty50%	V_{DDO} /2-0.2	V_{DDO} /2	V_{DDO} /2+0.2	V
Output Driver High side Resistance	R_H	V_{OUT}=V_{DDO}-0.1V	-	1.5	2	Ω
Output Driver Low side Resistance	R_L	V_{OUT}=0.1V	-	1.5	2	Ω
Beep High side Current	I_{BH}	V_{OUT}=V_{DDO}-1V	20	50	150	uA
Beep Low side Current	I_{BL}	V_{OUT}=1V	20	50	150	uA
Operating Current At Standby	I_{ST}	Stopping MCK, IN_1, IN_2, BEEP	-	-	1	uA
Operating Current At no input signal	I_{DD}	No-load operating IN_1, IN_2=32f_S MCK=256f_S	-	0.05	0.1	mA
	I_{DDO}		-	0.6	1.2	
Input Voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
Input Leakage Current	I_{LK}		-	-	±1	uA

■ TIMING CHARACTERISTICS

- Audio Signal Input

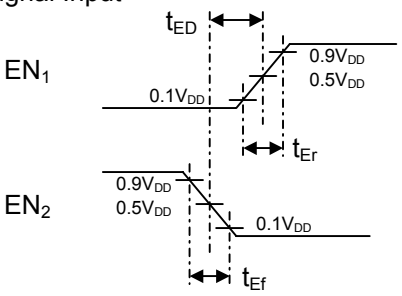


(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=V_{SSO}=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCK Frequency	f_{MCKI}		8	-	25	MHz
MCK Pulse Width (H)	t_{MCKH}		12	-	-	ns
MCK Pulse Width (L)	t_{MCKL}		12	-	-	ns
IN_1,IN_2 Setup Time	t_{DS}		20	-	-	ns
IN_1,IN_2 Hold Time	t_{DH}		20	-	-	ns
BEEP Frequency	f_{BEEP}		0.1	-	20	kHz

Note 4) t_{MCKI} shows the cycle of the MCK signal.

- Output Control Signal Input



(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=V_{SSO}=0.0V, unless otherwise noted)

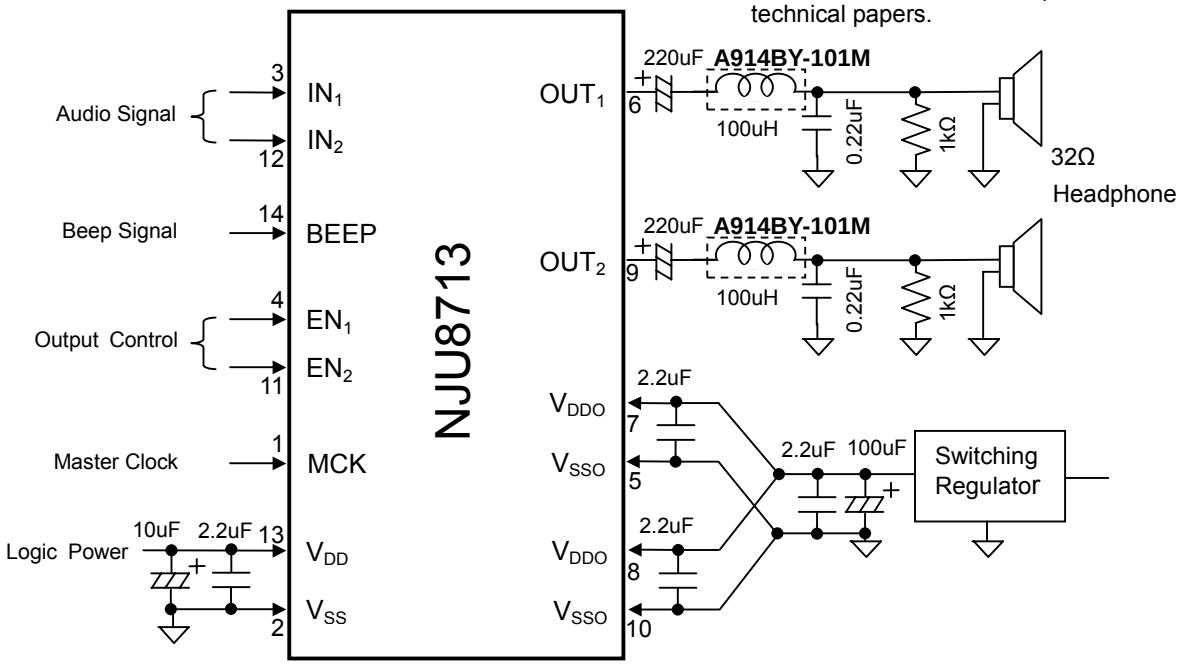
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	t_{Er}		-	-	50	ns
Fall Time	t_{Ef}		-	-	50	ns
Switching Time	t_{ED}				100	ns

Note 5) All timings are based on 30% and 70% voltage level of V_{DD}.

■ APPLICATION CIRCUIT

• Stereo OTL application example

•A914BY-101M is manufactured by TOKO, INC. For further information, please refer to its technical papers.



• 1 channel BTL application example

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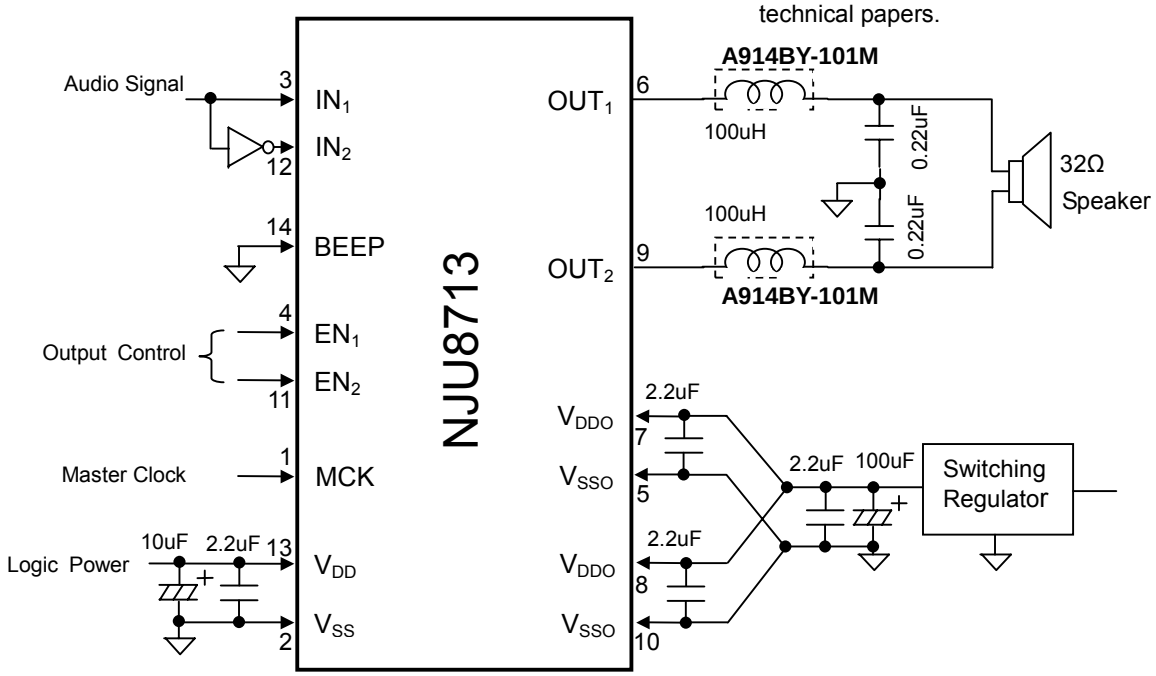

Note 6) De-coupling capacitors must be connected between each power supply pin and GND pin.

Note 7) The power supply for V_{DDO} requires fast driving response performance such as a switching regulator for T.H.D.

Note 8) The bigger capacitor value of external AC-coupling capacitors realize better low frequency response characteristics. In addition, ESR(Equivalent Series Resistance) should be low.

Note 9) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

[CAUTION]
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