16M x16 Mobile DDR SDRAM

FEATURES

- 1.8V power supply, 1.8V I/O power
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- MRS cycle with address key programs
  - CAS Latency (3)
  - Burst Length (2, 4, 8)
  - Burst Type (Sequential & Interleave)
  - Partial Self Refresh Type (Full, 1/2, 1/4 array)
  - Internal Temperature Compensated Self Refresh
  - Driver strength (1, 1/2, 1/4, 1/8)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK).
- Data I/O transactions on both edges of data strobe, DM for masking.
- Edge aligned data output, center aligned data input.
- No DLL; CK to DQS is not synchronized.
- LDM/UDM for write masking only.
- 7.8us auto refresh duty cycle.
- CSP package.

Operating Frequency

	DDR200	DDR133
Speed @CL3	100Mhz	66Mhz

*CL : CAS Latency

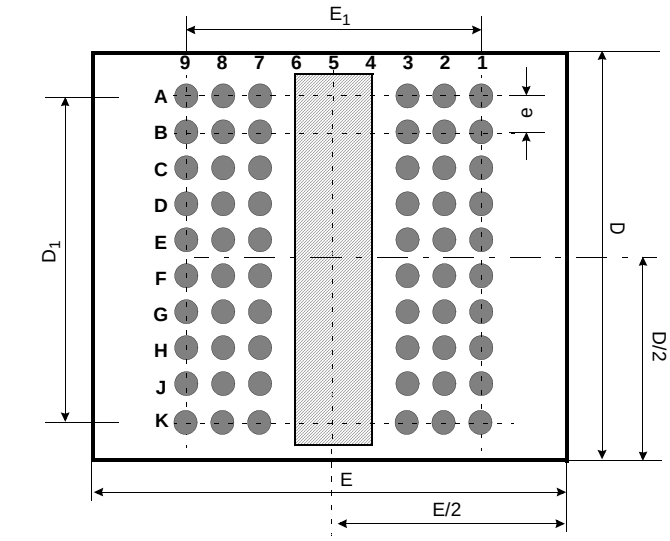
Column address configuration

Organization	Row Address	Column Address
16Mx16	A0 ~ A12	A0-A8

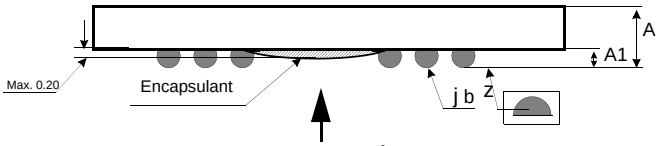
DM is internally loaded to match DQ and DQS identically.

Package Dimension and Pin Configuration

< Bottom View*1 >

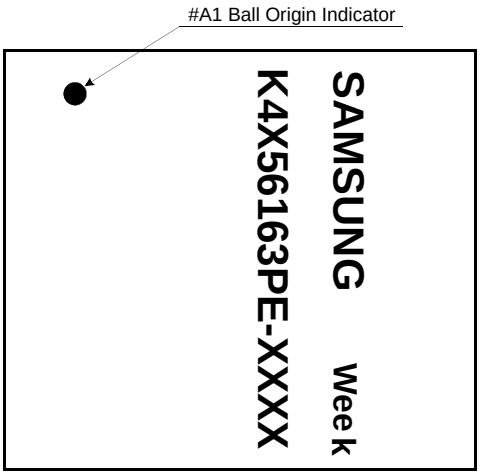


*2: Top View



*1: Bottom View

< Top View*2 >



< Top View*2 >

60Ball(6x10) CSP						
	1	**2**	**3**	**7**	**8**	**9**
A	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD
B	VDDQ	DQ13	DQ14	DQ1	DQ2	VSSQ
C	VSSQ	DQ11	DQ12	DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10	DQ5	DQ6	VSSQ
E	VSSQ	UDQS	DQ8	DQ7	LDQS	VDDQ
F	VSS	UDM	N.C.	N.C.	LDM	VDD
G	CKE	CK	$\overline{CK}$	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12	$\overline{CS}$	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	VSS	A4	A5	A2	A3	VDD

Ball Name	Ball Function
CK, $\overline{CK}$	*System Differential Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A0 ~ A12	*Address*
BA0 ~ BA1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
L(U)DM	*Data Input Mask*
L(U)DQS	*Data Strobe*
DQ0 ~ 15	*Data Input/Output*
VDD/VSS	*Power Supply/Ground*
VDDQ/VSSQ	*Data Output Power/Ground*

[Unit:mm]

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
A_1	0.30	0.35	0.40
E	-	11.0	-
E_1	-	6.4	-
D	-	9.0	-
D_1	-	7.2	-
e	-	0.80	-
jb	0.40	0.45	0.50
z	-	-	0.10

Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Internal clock signals are derived from CK/$\overline{CK}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE , are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select : $\overline{CS}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
*1LDM,UDM	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM corresponds to the data on DQ8-DQ15.
BA0, BA1	Input	Bank Address Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 determines which mode register (mode register or extended mode register) is loaded during the MODE REGISTER SET command.
*1DQ	I/O	Data Input/Output : Data bus
*1LDQS,UDQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. it is used to fetch write data. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : 1.7V to 1.95V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : 1.7V to 1.95V..
VSS	Supply	Ground.

Functional Description

Simplified State Diagram

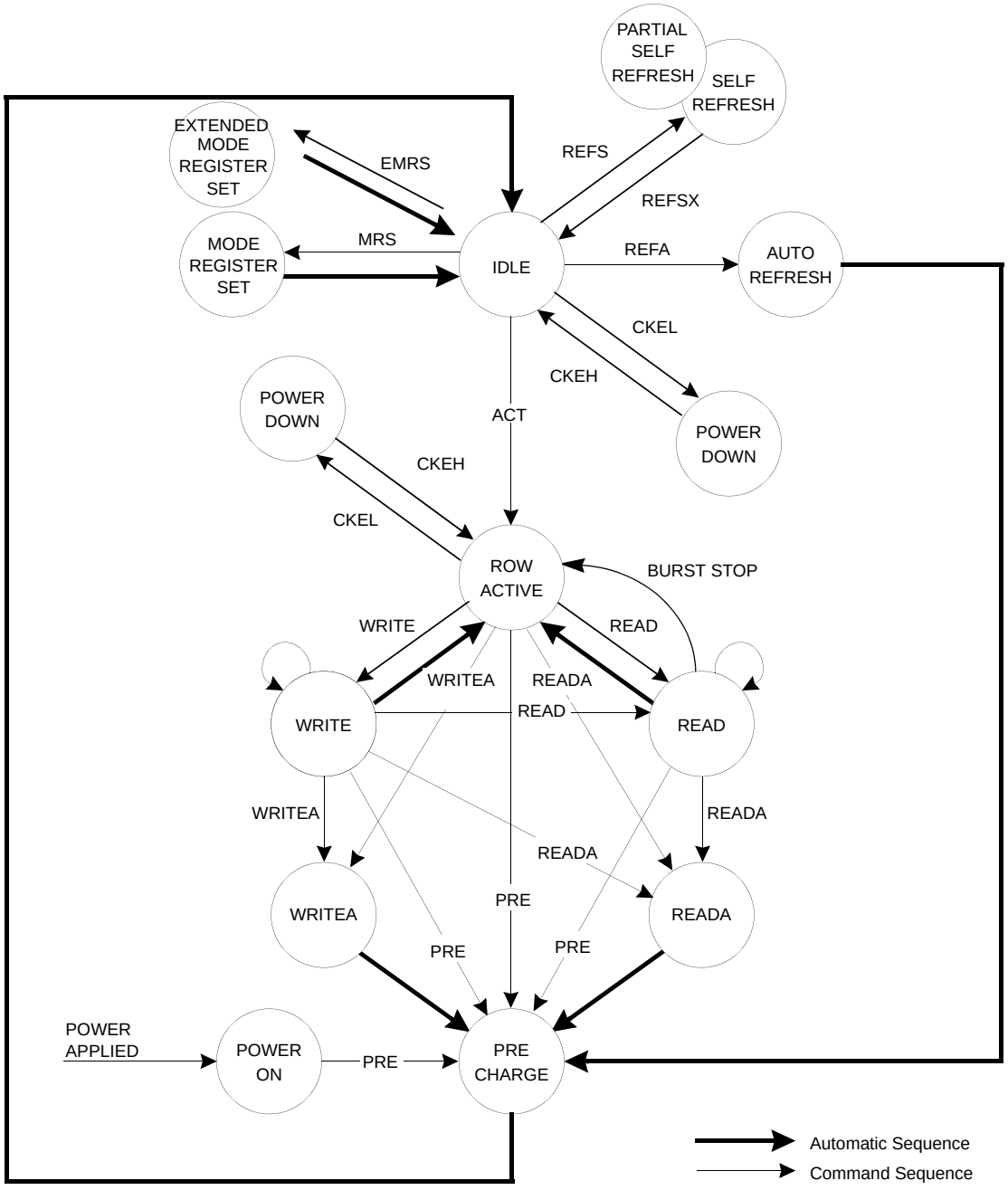
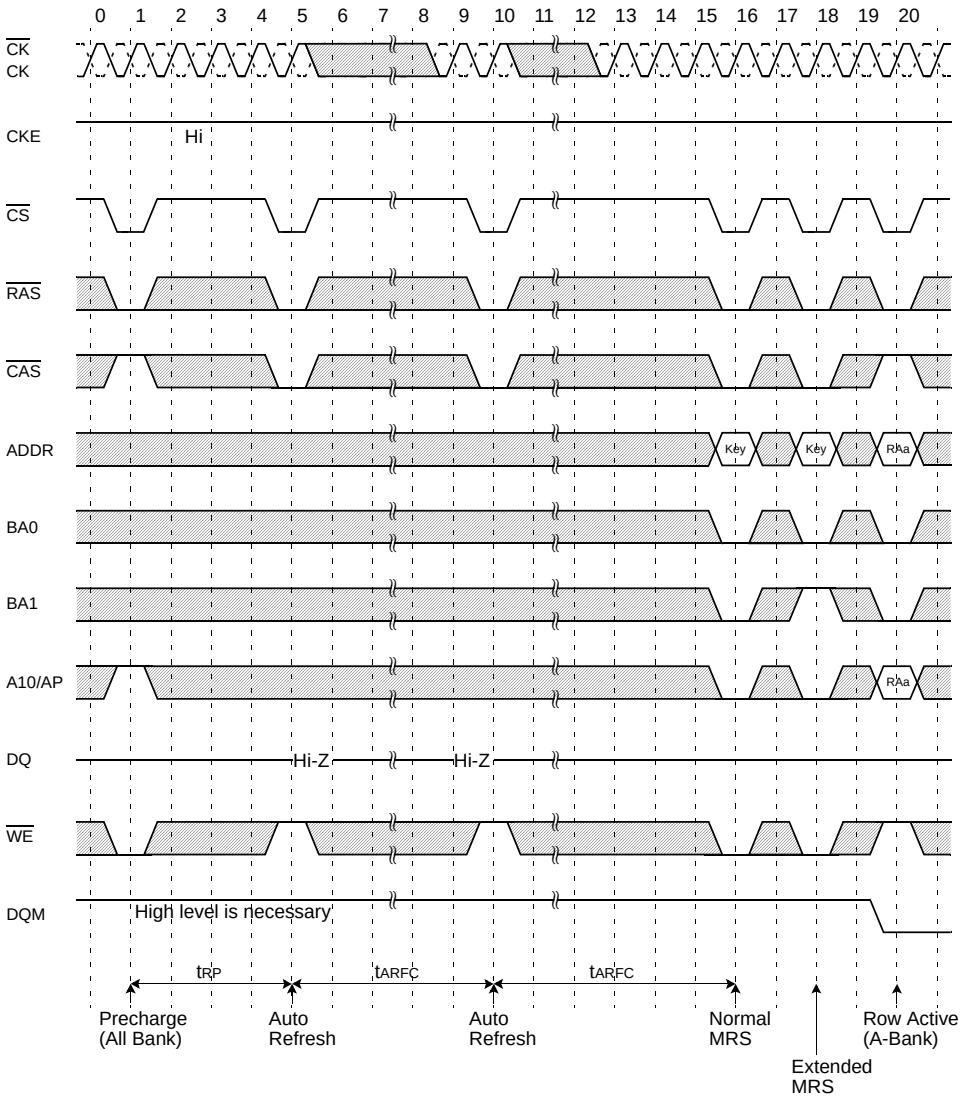


Figure.1 State diagram

Power Up Sequence for Mobile DDR SDRAM



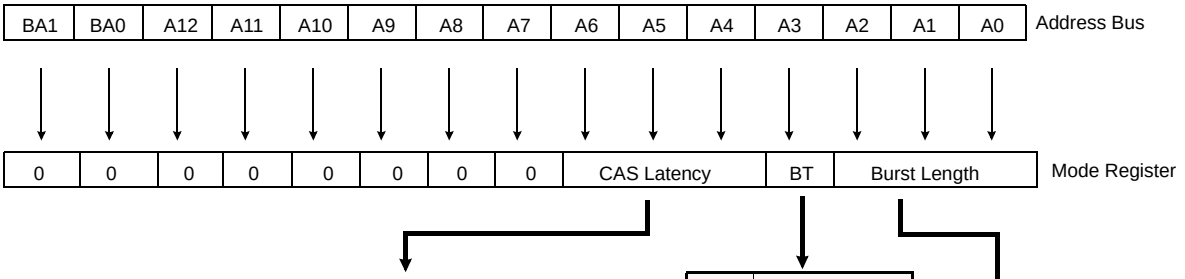
Note:
1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define PASR or DS operating type of the device after normal MRS.

EMRS cycle is not mandatory and the EMRS command needs to be issued only when either PASR or DS is used.
The default state without EMRS command issued is half driver strength, and Full array refreshed .
The device is now ready for the operation selected by EMRS.
For operating with PASR or DS, set PASR or DS mode in EMRS setting stage.
In order to adjust another mode in the state of PASR or DS mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

Mode Register Definition

Mode Register Set(MRS)

The mode register is designed to support the various operating modes of DDR SDRAM. It includes CAS latency, addressing mode, burst length, test mode and vendor specific options to make DDR SDRAM useful for variety of applications. The default value of the mode register is not defined, therefore the mode register must be written in the power up sequence of DDR SDRAM. The mode register is written by asserting low on CS, RAS, CAS and WE(The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 and BA0, BA1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Two clock cycles are required to complete the write operation in the mode register. Even if the power-up sequence is finished and some read or write operations is executed afterward, the mode register contents can be changed with the same command and four clock cycles. This command must be issued only when all banks are in the idle state. If mode register is changed, extended mode register automatically is reset and come into default state. So extended mode register must be set again. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. BA0 and BA1 must be set to low for normal DDR SDRAM operation.



A_6	A_5	A_4	CAS Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	Reserve
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

A_3	Burst Type
0	Sequential
1	Interleave

Burst Length

A_2	A_1	A_0	Burst type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

Figure.2 Mode Register Set

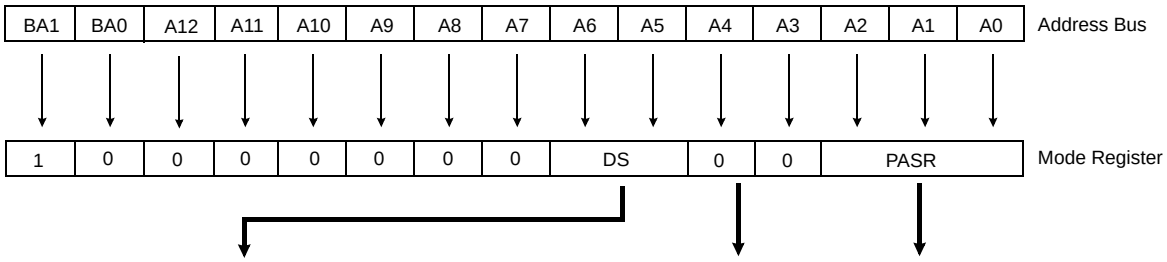
Burst address ordering for burst length

Burst Length	Starting Address(A2, A1, A0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Register Set(EMRS)

The extended mode register is designed to support partial array self refresh or driver strength. EMRS cycle is not mandatory and the EMRS command needs to be issued only when either PASR or DS is used. The default state without EMRS command issued is +85°C, all 4 banks refreshed and the half size of driver strength. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA1 ,low on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. Even if the power-up sequence is finished and some read or write operations is executed afterward, the mode register contents can be changed with the same command and four clock cycles. But this command must be issued only when all banks are in the idle state. A0 - A2 are used for partial array self refresh and A5 - A6 are used for driver strength. "High" on BA1 and"Low" on BA0 are used for EMRS. All the other address pins except A0,A1,A2, BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.

Extended MRS for PASR(Partial Array Self Refresh) & TCSR(Internal Temperature Compensated Self Refresh)



DS		
A_6	A_5	Driver Strength
0	0	Full
0	1	1/2
1	0	1/4
1	1	1/8

Internal TCSR
Self refresh cycle is controlled automatically by internal temperature sensor and control circuit according to the two temperature ; Max 40 °C,Max 85 °C

PASR			
A_2	A_1	A_0	# of Banks
0	0	0	Full Array
0	0	1	1/2 Array
0	1	0	1/4 Array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Internal Temperature Compensated Self Refresh (TCSR)

Note :

1. In order to save power consumption, Mobile DDR SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range ; Max. 40 °C, Max. 85 °C.
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (Icc 6)			Unit
	Full Array	1/2 Array	1/4 Array	
Max. 40 °C	150	125	115	uA
Max. 85 °C	400	300	250	

Partial Array Self Refresh (PASR)

Note :

1. In order to save power consumption, Mobile DDR SDRAM includes PASR option.
2. Mobile DDR SDRAM supports three kinds of PASR in self refresh mode; Full Array, 1/2 Array, 1/4 Array.

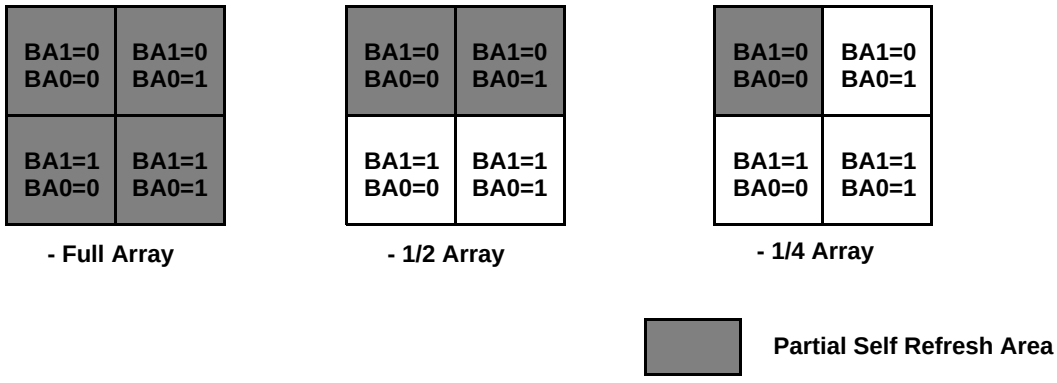


Figure.3 EMRS code and TCSR , PASR

Precharge

The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses(BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied until the precharge command can be issued. After tRP from the precharge, an active command to the same bank can be initiated.

Bank selection for precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

No Operation(NOP) & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode DDR SDRAM should ignore all the control inputs. The DDR SDRAMs are put in NOP mode when $\overline{CS}$ is active and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. Both Device Deselect and NOP command can not affect operation already in progress. So even if the device is deselected or NOP command is issued under operation, operation will be complete.

Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock(CK). The DDR SDRAM has four independent banks, so two Bank Select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time(tRCD min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(tRRD min).

Bank Activation Command Cycle

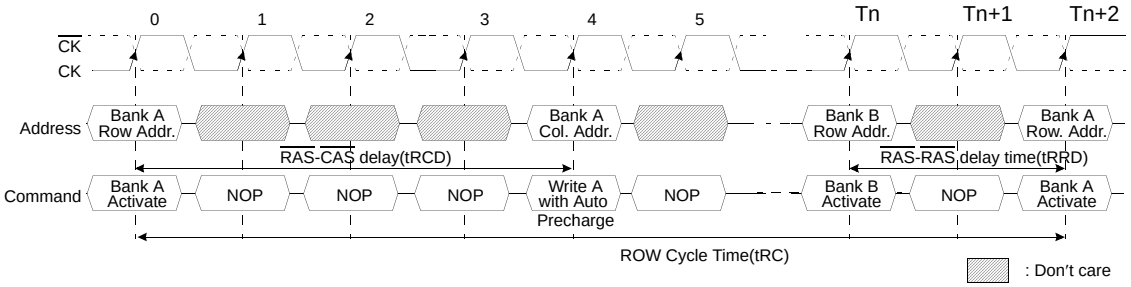


Figure.4 Bank activation command cycle timing

Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS cycle.

Write Bank

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS cycle.

Essential Functionality for DDR SDRAM

The essential functionality that is required for the DDR SDRAM device is described in this chapter

Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock(CK) after tRCD from the bank activation. The address inputs (A0~A9) determine the starting address for the Burst. The Mode Register sets type of burst(Sequential or interleave) and burst length(2, 4, 8). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe(DQS) adopted by DDR SDRAM until the burst length is completed.

< Burst Length=4, $\overline{CAS}$ Latency= 3 >

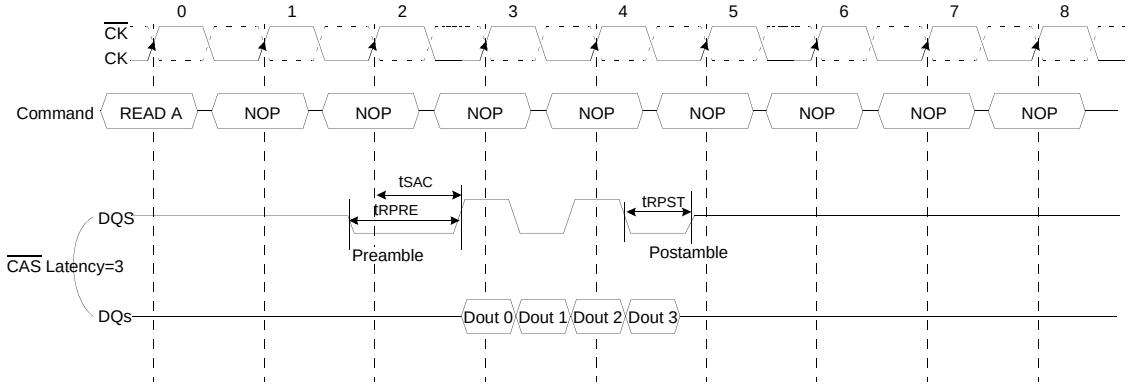


Figure.5 Burst read operation timing

Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock(CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS(Data-in setup time) prior to data strobe edge enabled after tDQSS from the rising edge of the clock(CK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

< Burst Length=4 >

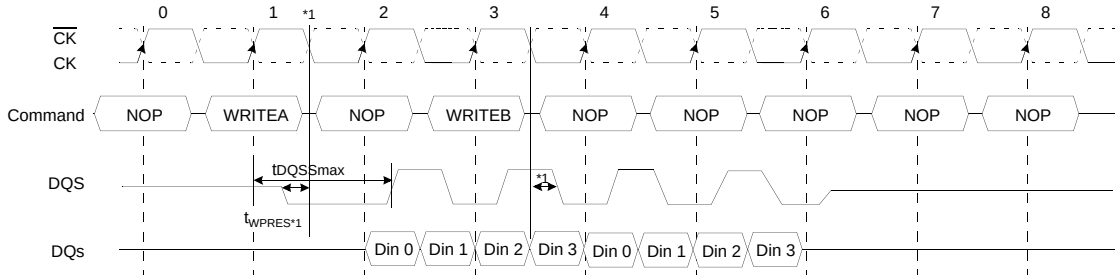


Figure.6 Burst write operation timing

1. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.

< Burst Length=4, CAS Latency=3 >

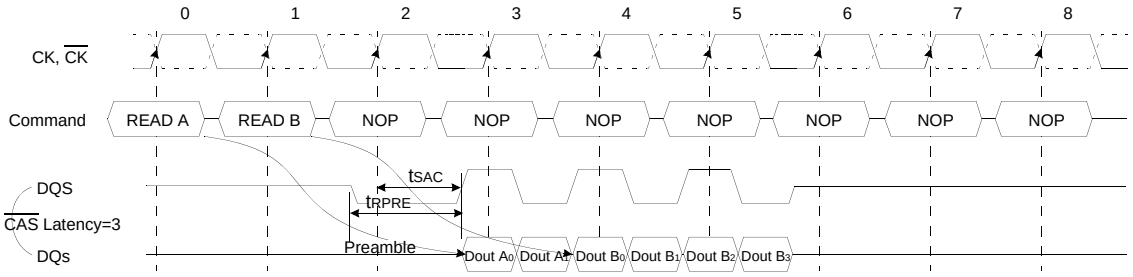


Figure.7 Read interrupted by a read timing

Read Interrupted by a Write & Burst Stop

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQs(Output drivers) in a high impedance state. To insure the DQs are tri-stated one cycle before the beginning of the write operation, Burst stop command must be applied at least 2 clock cycles for CL=2 and at least 3 clock cycles for CL=3 before the Write command.

< Burst Length=4, CAS Latency=3 >

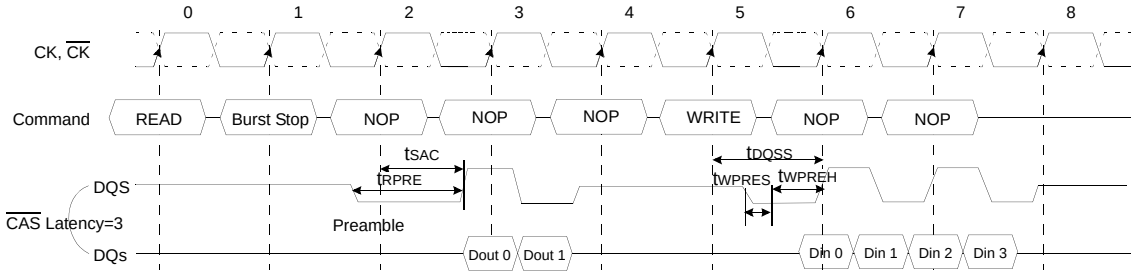


Figure.8 Read interrupted by a write and burst stop timing.

The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU(CL) [CL is the CAS Latency and RU means round up to the nearest integer].
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the CAS latency.

< Burst Length=8, CAS Latency=3 >

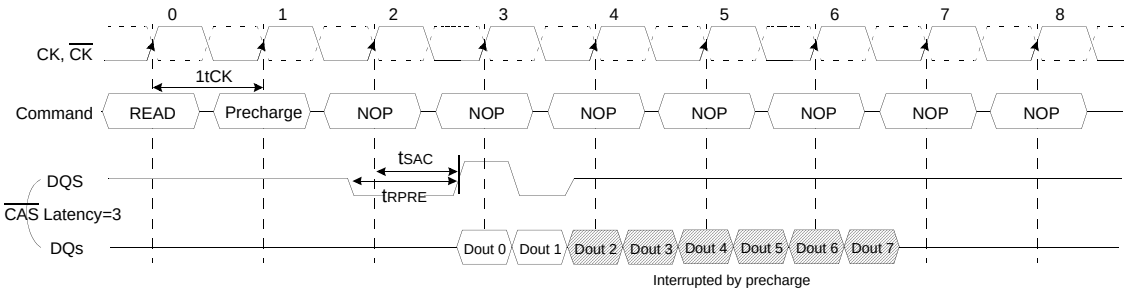


Figure.9 Read interrupted by a precharge timing

When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.
3. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP where tRP begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.
4. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a rising clock edge).In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

< Burst Length=4 >

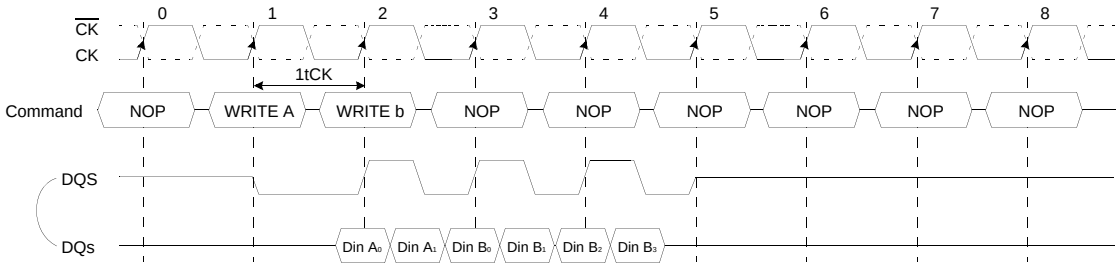


Figure.10 Write interrupted by a write timing

Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time(tWR) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

< Burst Length=8 >

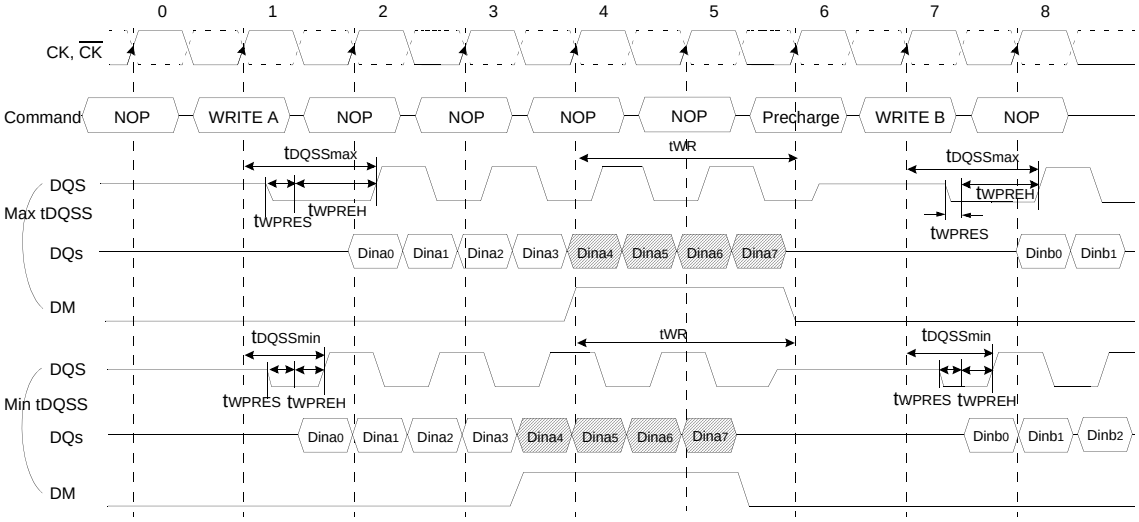


Figure.11 Write interrupted by a precharge and DM timing

Precharge timing for Write operations in DRAMs requires enough time to allow ''write recovery'' which is the time required by a DRAM core to properly store a full ''0'' or ''1'' level before a Precharge operation. For DDR SDRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the SDRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation, i.e., the input clock domain.

tWR starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by tWR.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by tWR.

3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after tWR+tRP where tWR+tRP starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where tRAS(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.
5. Refer to "3.3.2 Burst write operation"

Burst Stop

The burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock(CK). The burst stop command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ latency set in the mode register. The burst stop command, however, is not supported during a write burst operation.

< Burst Length=4, $\overline{CAS}$ Latency= 3 >

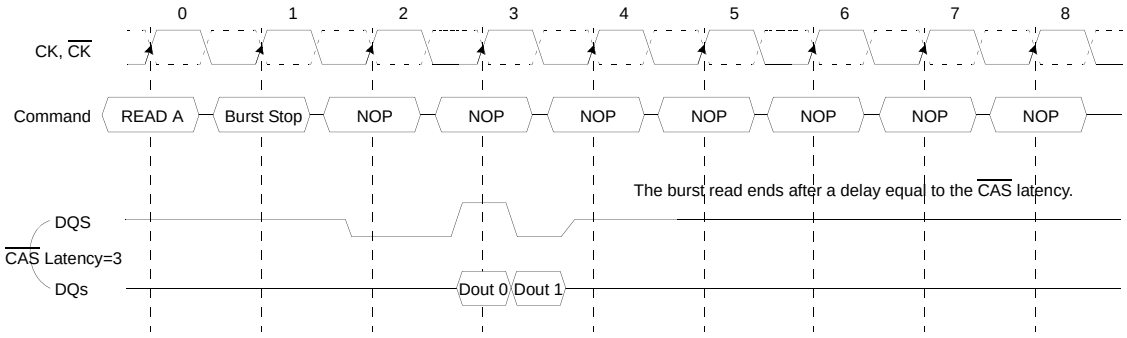


Figure.12 Burst stop timing

The Burst Stop command is a mandatory feature for DDR SDRAMs. The following functionality is required:

1. The BST command may only be issued on the rising edge of the input clock, CK.
2. BST is only a valid command during Read bursts.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).

DM masking

The DDR SDRAM has a data mask function that can be used in conjunction with data write cycle, not read cycle. When the data mask is activated (DM high) during write operation, DDR SDRAM does not accept the corresponding data.(DM to data-mask latency is zero).

DM must be issued at the rising or falling edge of data strobe.

< Burst Length=8 >

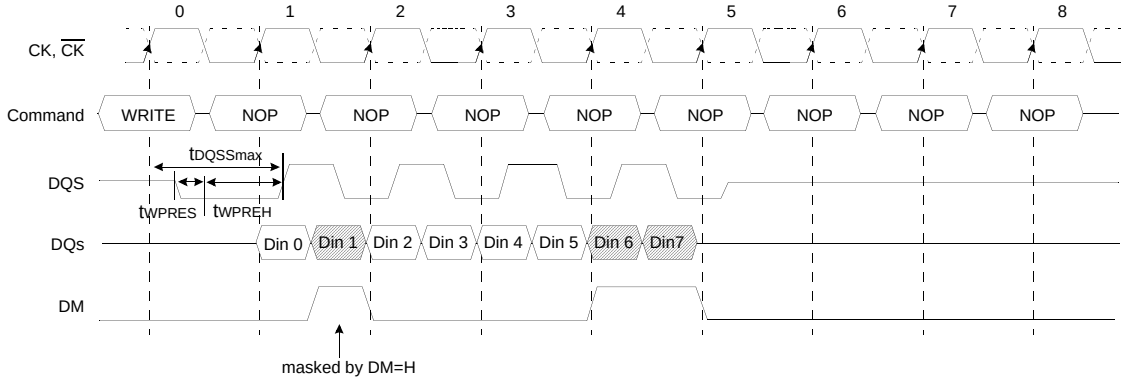


Figure.13 DM masking timing

Read With Auto Precharge

If a read with auto-precharge command is issued, the DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when tRAS(min) is satisfied. If not, the start point of precharge operation will be delayed until tRAS(min) is satisfied. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the precharge time(tRP) has been satisfied.

< Burst Length=4, $\overline{\text{CAS}}$ Latency= 3>

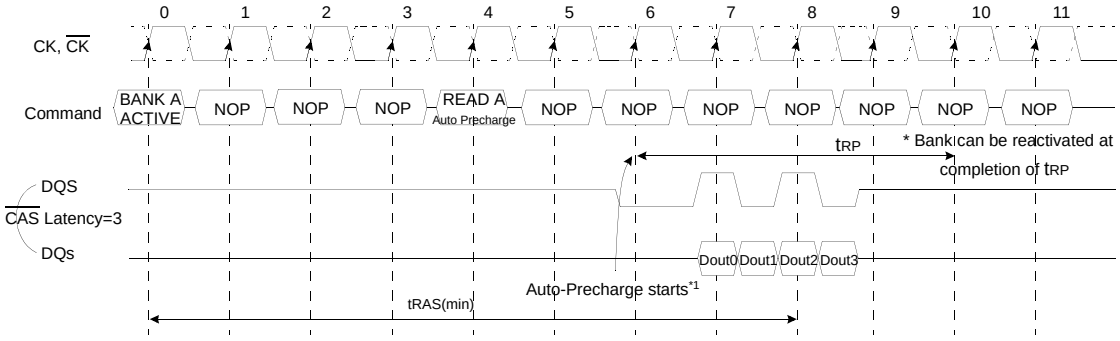


Figure.14 Read with auto precharge timing

***Note :** 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same bank is illegal

Write with Auto Precharge

If A10 is high when write command is issued , the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

< Burst Length=4 >

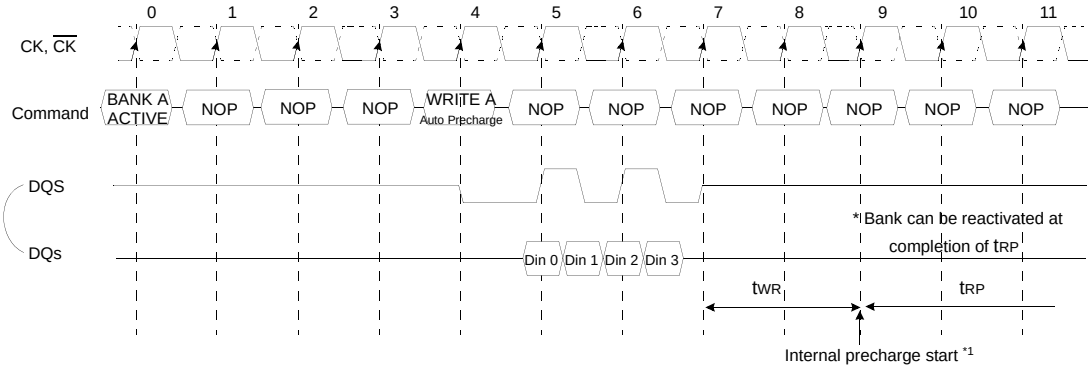


Figure 15. Write with auto precharge timing

***Note :** 1. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same bank is illegal

Auto Refresh & Self Refresh

Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CK). All banks must be precharged and idle for tRP(min) before the auto refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the tARFC(min).

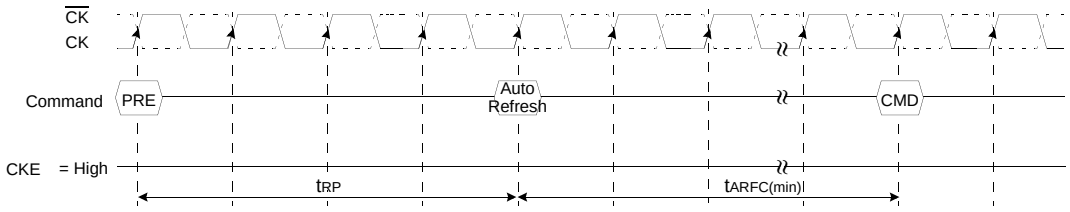


Figure.16 Auto refresh timing

Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CK, $\overline{CK}$) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. To exit the Self Refresh mode, supply stable clock input before returning CKE high, assert deselect or NOP command and then assert CKE high. In case that the system uses burst auto refresh during normal opreation, it is recommended to use burst 8192 auto refresh cycle immediately before entering self refresh mode and after exiting in self refresh mode. On the other hand, if the system uses the distributed auto refresh, the system only has to keep the refresh duty cycle.

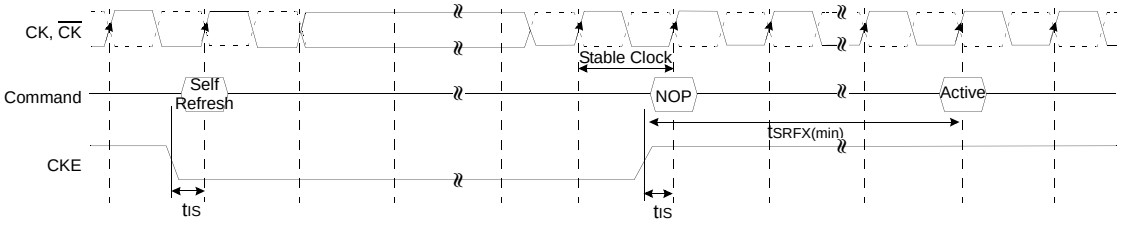


Figure.17 Self refresh timing

Power down

The device enters power down mode when CKE Low,and it exits when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. The both bank should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1 tCK+tIS prior to Row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period(tREF) of the device.

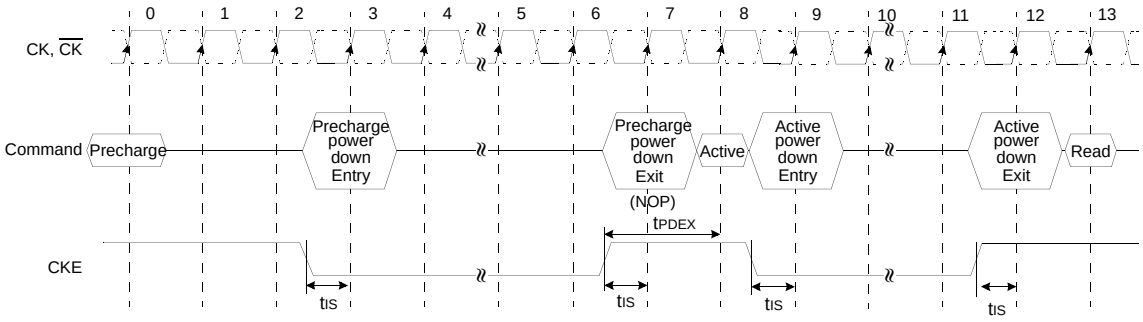


Figure.18 Power down entry and exit timing

Command Truth Table(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

1. OP Code : Operand Code. A0 ~ A11 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

Functional Truth Table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARGE STANDBY	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*4
	L	L	L	H	X	Refresh	AUTO-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ACTIVE STANDBY	L	H	H	L	X	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	L	H	H	L	X	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Functional truth table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Pre-charge*3
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst With DM=High, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE*6 (READA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	*6
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	*6
	L	L	H	L	BA, A10	PRE/PREA	*6
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO RECHARGE*7 (WRITEA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	*7
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	*7
	L	L	H	H	BA, RA	Active	*7
	L	L	H	L	BA, A10	PRE/PREA	*7
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Functional truth table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARGING (DURING tRP)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING (FROM ROW ACTIVE TO tRCD)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING (DURING tWR OR tCDLR)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	H	BA, CA, A10	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Functional truth table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
RE-FRESHING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Functional truth table

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING*8	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOPeration(Maintain Self-Refresh)
POWER DOWN	L	H	X	X	X	X	X	Exit Power Down(Idle after tPDEX)
	L	L	X	X	X	X	X	NOPeration(Maintain Power Down)
ALL BANKS IDLE*9	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State=Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table

ABBREVIATIONS :
H=High Level, L=Low level, X=Don't Care

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around and write recovery requirements.
4. NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Refer to "3.3.10 Read with Auto Precharge" for detailed information.
7. Refer to "3.3.11 Write with Auto Precharge" for detailed information.
8. CKE Low to High transition will re-enable CK, $\overline{CK}$ and other inputs asynchronously. A minimum setup time must be satisfied before issuing any command other than EXIT.
9. Power-Down and Self-Refresh can be entered only from All Bank Idle state.

ILLEGAL = Device operation and/or data integrity are not guaranteed.

Table 10. Absolute maximum ratings

Absolute maximum ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.7	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.7	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions & Specifications

DC Operating Conditions

Recommended operating conditions(Voltage referenced to VSS=0V, TA= -25°C to 85°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 1.8V)	VDD	1.7	1.95		
I/O Supply voltage	VDDQ	1.7	1.95	V	
Input logic high voltage	VIH(DC)	0.7 x VDDQ	VDDQ+0.3	V	1
Input logic low voltage	VIL(DC)	-0.3	0.3 x VDDQ	V	1
Output logic high voltage	VOH(DC)	0.9 x VDDQ	-	V	IOH = -0.1mA
Output logic low voltage	VOL(DC)	-	0.1 x VDDQ	V	IOL = 0.1mA
Input leakage current	II	-2	2	uA	
Output leakage current	IOZ	-5	5	uA	

Notes : 1. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, Temp = -25 to 85°C)

Parameter	Symbol	Test Condition		DDR200	DDR133	Unit
Operating Current (One Bank Active)	I_{CC0}	t RC = t RCmin ; t CK = t CKmin ; CKE is HIGH; CS is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE		30	30	mA
Precharge Standby Current in power-down mode	I_{CC2P}	all banks idle, CKE is LOW; CS is HIGH, t CK = t CKmin ; address and control inputs are SWITCHING; data bus inputs are STABLE		0.3		mA
	I_{CC2PS}	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		0.3		
Precharge Standby Current in non power-down mode	I_{CC2N}	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, t CK = t CKmin ;address and control inputs are SWITCHING; data bus inputs are STABLE		8	8	mA
	I_{CC2NS}	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		4	4	
Active Standby Current in power-down mode	I_{CC3P}	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, t CK = t CKmin ;address and control inputs are SWITCHING; data bus inputs are STABLE		3		mA
	I_{CC3PS}	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH;address and control inputs are SWITCHING; data bus inputs are STABLE		1		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, t CK = t CKmin ;address and control inputs are SWITCHING; data bus inputs are STABLE		10	10	mA
	I_{CC3NS}	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		6	6	mA
Operating Current (Burst Mode)	I_{CC4R}	one bank active; BL = 4; CL = 3; t CK = t CKmin ; continuous read bursts; I OUT = 0 mA address inputs are SWITCHING; 50% data change each burst transfer		65	55	mA
	I_{CC4W}	one bank active; BL = 4; t CK = t CKmin ; continuous write bursts;address inputs are SWITCHING; 50% data change each burst transfer		65	55	mA
Refresh Current	I_{CC5}	t RC = t RFCmin ; t CK = t CKmin ; burst refresh; CKE is HIGH;address and control inputs are SWITCHING; data bus inputs are STABLE		80	80	mA
Self Refresh Current	I_{CC6}	CKE is LOW; t CK = t CKmin ; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	**TCSR Range**	**Max 40**	**Max 85**	°C
			Full Array	150	400	uA
			1/2 Array	125	300	
			1/4 Array	115	250	

Notes:

1. IDD specifications are tested after the device is properly intialized.
2. Input slew rate is 1V/ns.

3. Definitions for IDD:

LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$;

HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$;

STABLE is defined as inputs stable at a HIGH or LOW level;

SWITCHING is defined as:

- address and command: inputs changing between HIGH and LOW once per two clock cycles
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

AC Operating Conditions & Timming Specification

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, all inputs	VIH(AC)	0.8 x VDDQ	VDDQ+0.3	V	1
Input Low (Logic 0) Voltage, all inputs	VIL(AC)	-0.3	0.2 x VDDQ	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(AC)	0.4 x VDDQ	0.6 x VDDQ	V	2

Note : 1. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.

2. The value of V_{IX} is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

AC Timming Parameters & Specifications

Parameter		Symbol	DDR200		DDR133		Unit	Note
			Min	Max	Min	Max		
Clock cycle time	CL=3.0	tCK	10		15		ns	1
Row cycle time		tRC	80		90		ns	
Row active time		tRAS	50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	30		30		ns	
Row precharge time		tRP	30		30		ns	
Row active to Row active delay		tRRD	15		15		ns	
Write recovery time		tWR	15		30		ns	
Last data in to Active delay		tDAL	tWR+tRP		tWR+tRP		-	2
Last data in to Read command		tCDLR	1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		tCK	
Clock high level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	tCK	
Output data access time from CK/$\overline{CK}$	CL=3.0	tSAC	2.0	7.0	2.0	7.0	ns	3
Data strobe edge to ouput data edge		tDQSQ		0.7		0.9	ns	1
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		ns	4
DQS-in hold time		tWPREH	0.25		0.25		tCK	
DQS-in high level width		tDQSH	0.4	0.6	0.4	0.6	tCK	
DQS-in low level width		tDQSL	0.4	0.6	0.4	0.6	tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time		tIS	1.5		2.0		ns	1
Address and Control Input hold time		tIH	1.5		2.0		ns	1
DQ & DM setup time to DQS		tDS	1.1		1.5		ns	5,6
DQ & DM hold time to DQS		tDH	1.1		1.5		ns	5,6
DQ & DM input pulse width		tDIPW	2.2		3.0		ns	
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	tCK	
Refresh interval time	256Mb	tREF	7.8		7.8		us	
Mode register set cycle time		tMRD	2		2		tCK	
Power down exit time		tPDEX	1*tCK +tIS		1*tCK +tIS		ns	
Auto refresh cycle time		tARFC	80		80		ns	
Exit self refresh to active command		tSRFX	120		120		ns	
Data hold from DQS to earliest DQ edge		tQH	tHPmin -1.0ns		tHPmin -1.0ns		ns	
Clock half period		tHP	tCLmin or tCHmin		tCLmin or tCHmin		ns	

1. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+50	+50
0.6	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 1.0V/ns.

2. Minimum 3CLK of tDAL(= tWR + tRP) is required because it need minimum 2CLK for tWR and minimum 1CLK for tRP.

3. tSAC(min) value is measured at the high Vdd(1.95V) and cold temperature(-25°C).
tSAC(max) value is measured at the low Vdd(1.7V) and hot temperature(85°C).
tSAC is measured in the device with half driver strength and under the AC output load condition (Fig.2 in next Page).

4. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

5. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+75	+75
0.6	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 1.0V/ns.

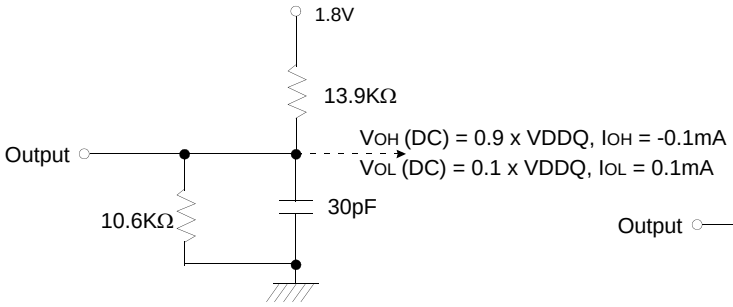
6. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

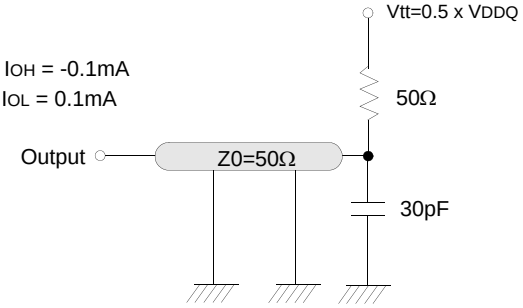
This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

AC Operating Test Conditions(V_{DD} = 1.7V - 1.95V, T_A = -25 to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit

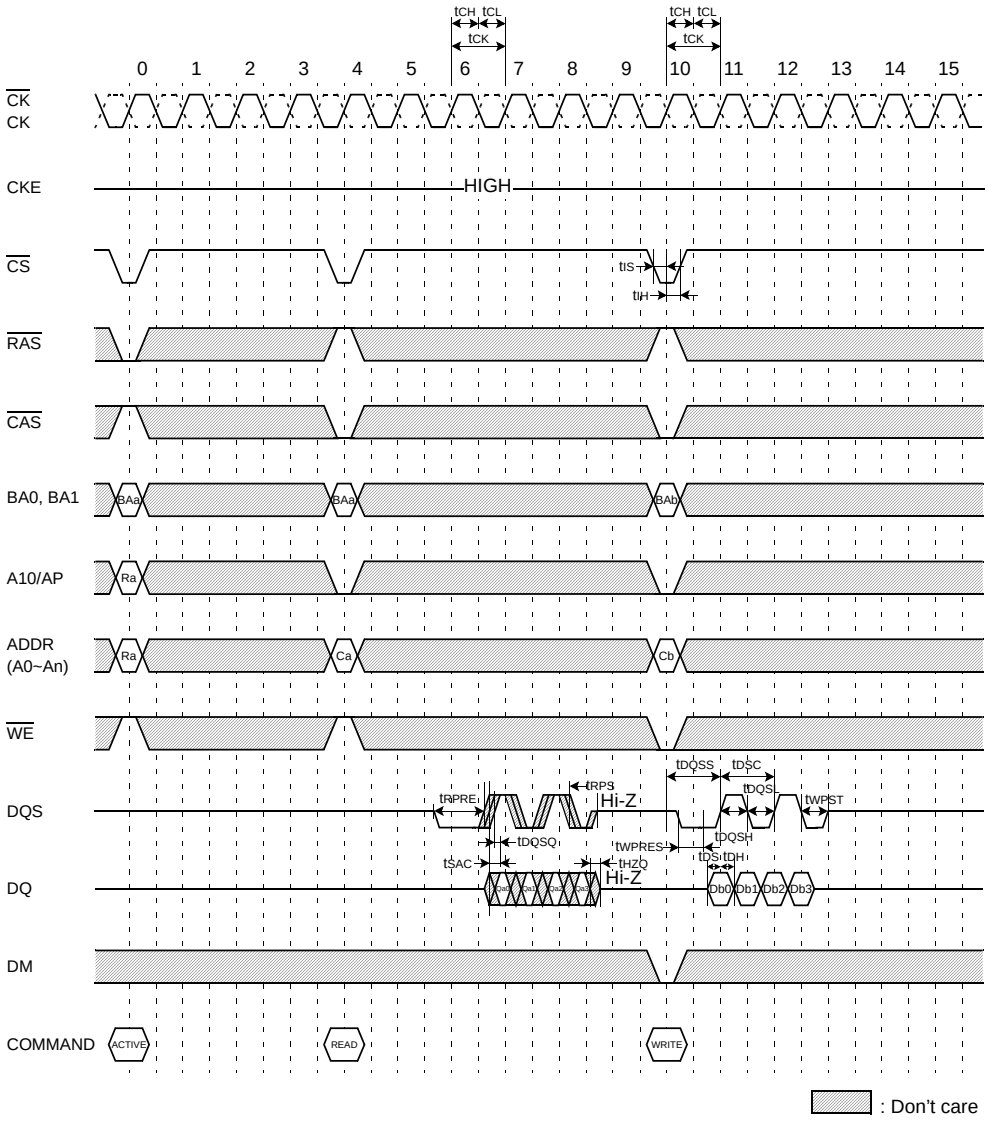


(Fig. 2) AC Output Load Circuit

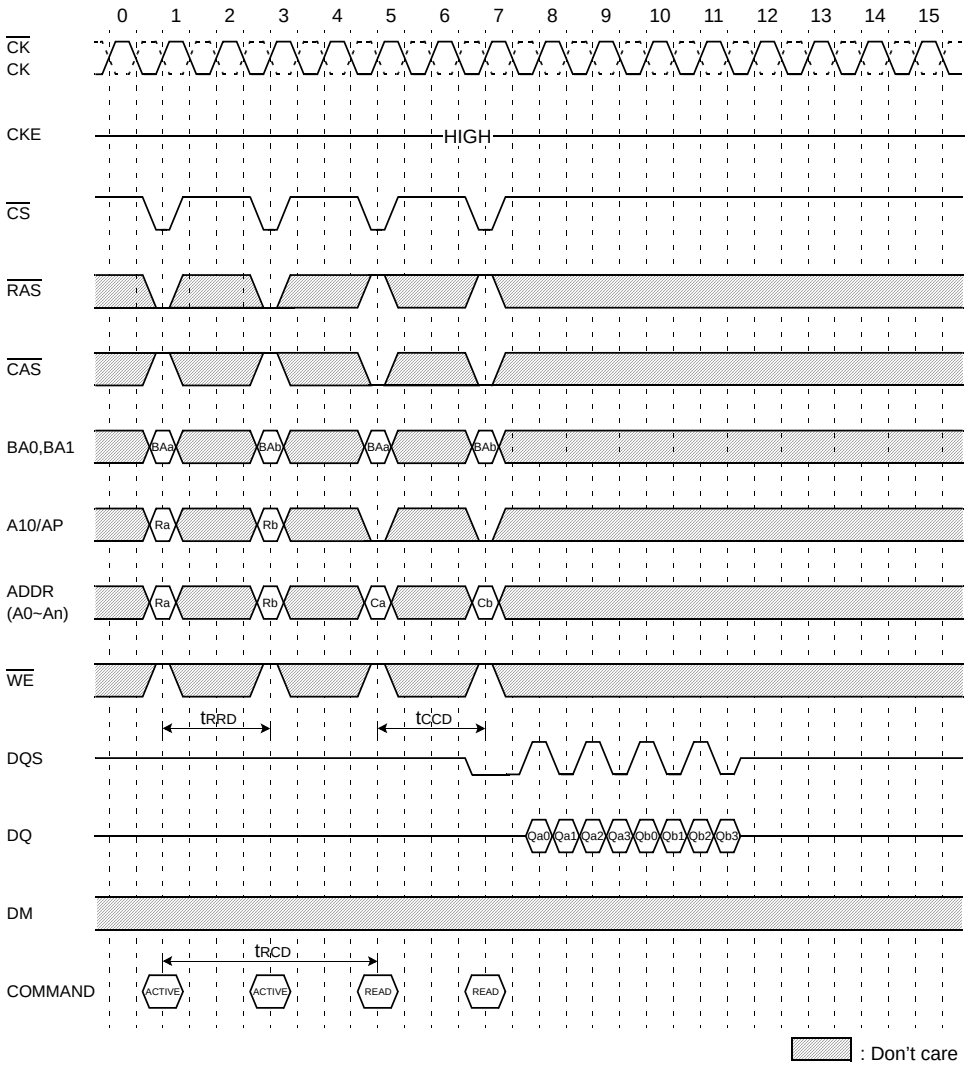
Input/Output Capacitance(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN1	1.5	3.0	pF
Input capacitance(CK, $\overline{CK}$)	CIN2	1.5	3.0	pF
Data & DQS input/output capacitance	COUT	3.0	5.0	pF
Input capacitance(DM)	CIN3	3.0	5.0	pF

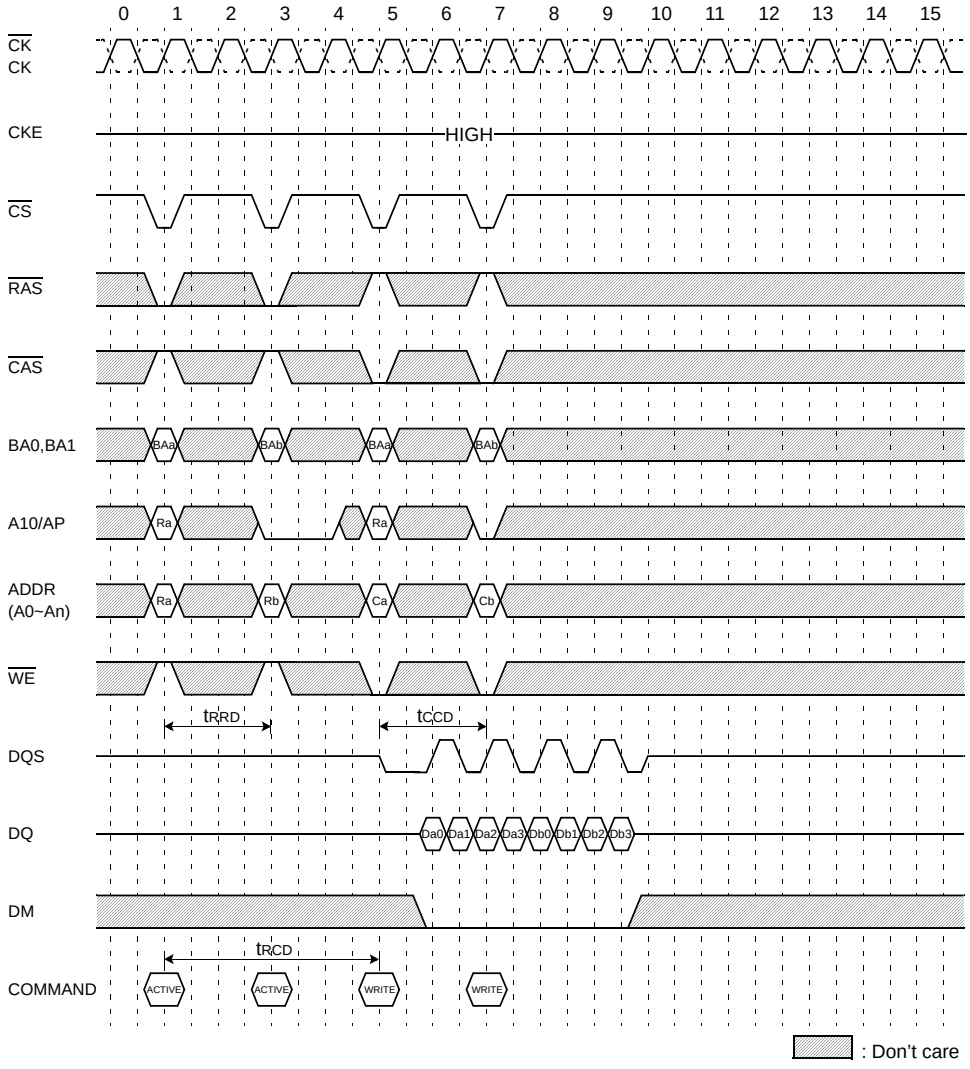
Basic Timing (Setup, Hold and Access Time @BL=4, CL=3)



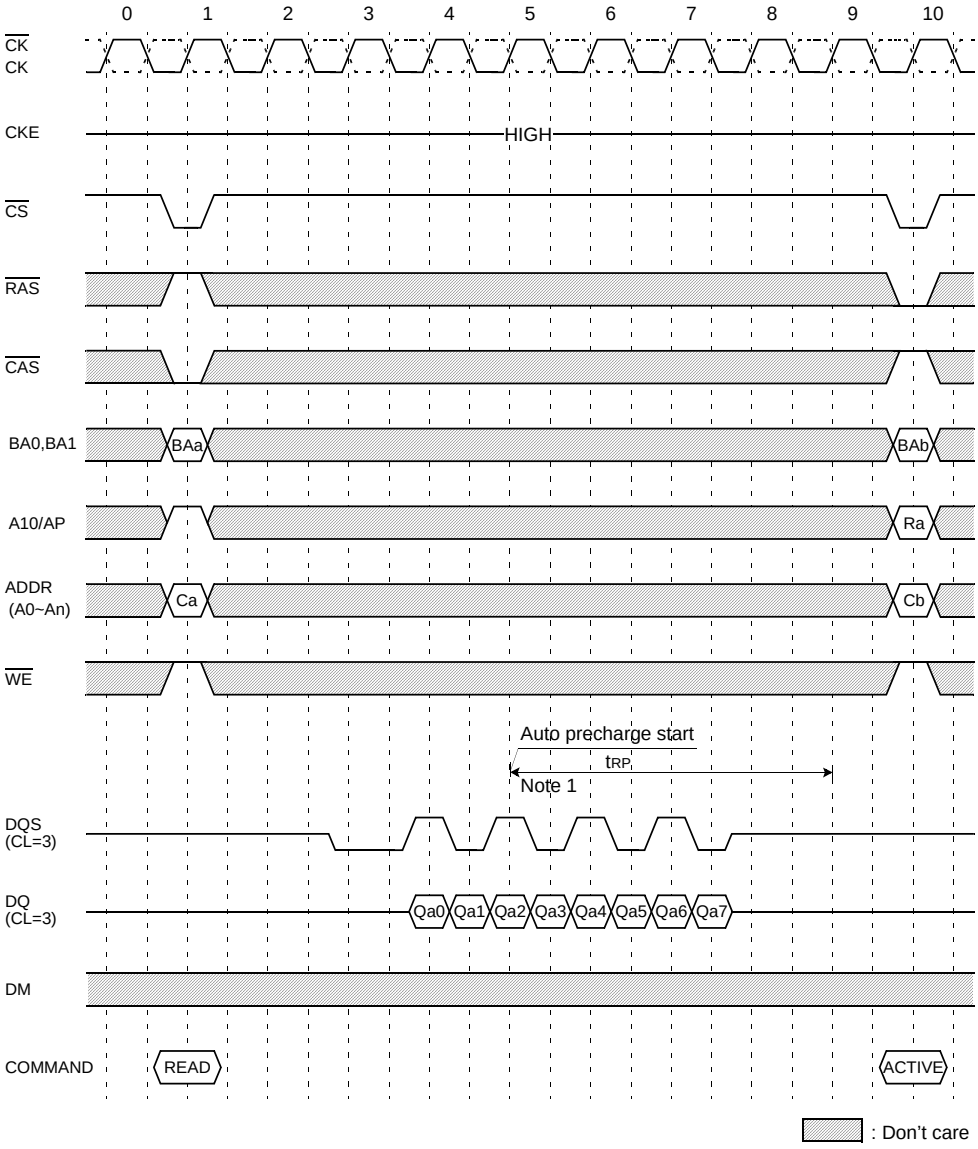
Multi Bank Interleaving READ (@BL=4, CL=3)



Multi Bank Interleaving WRITE (@BL=4)

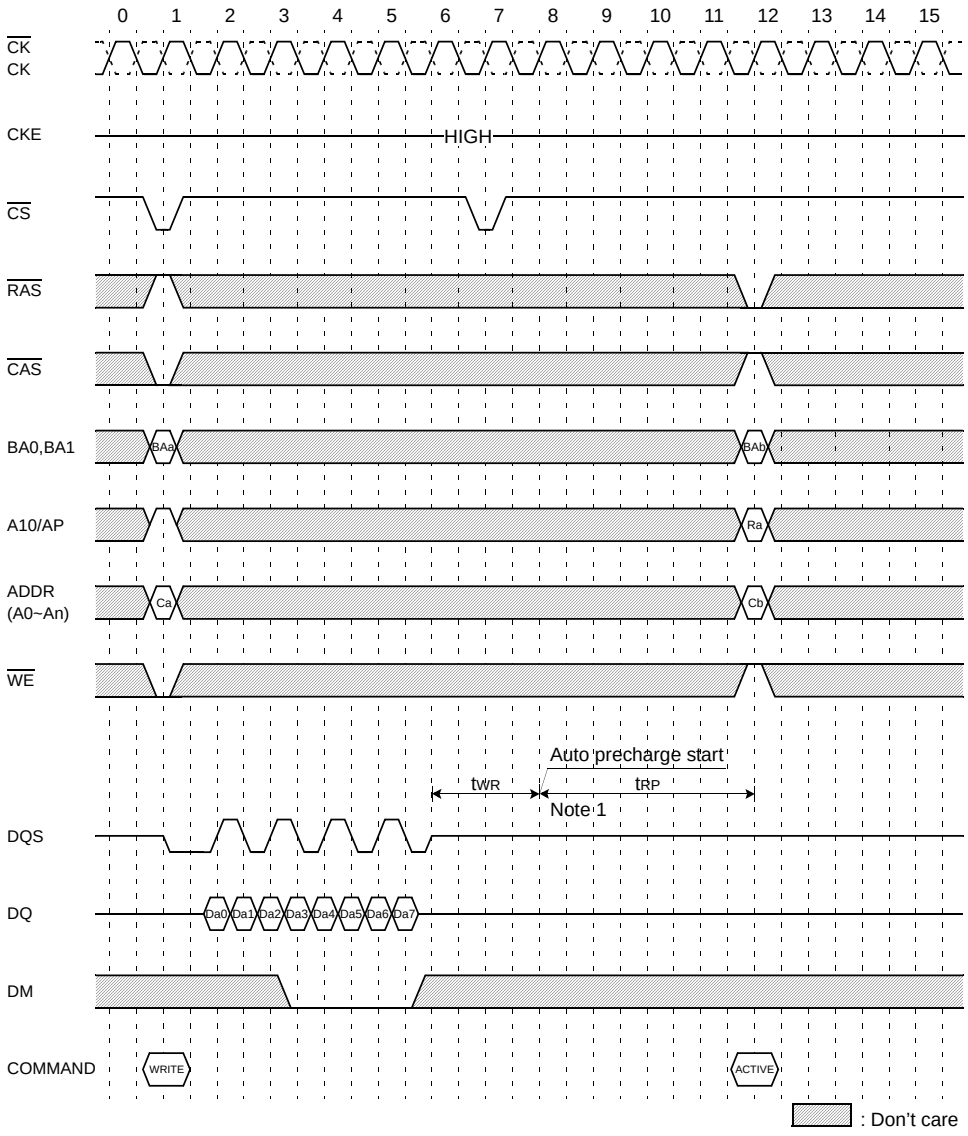


Read with Auto Precharge (@BL=8)



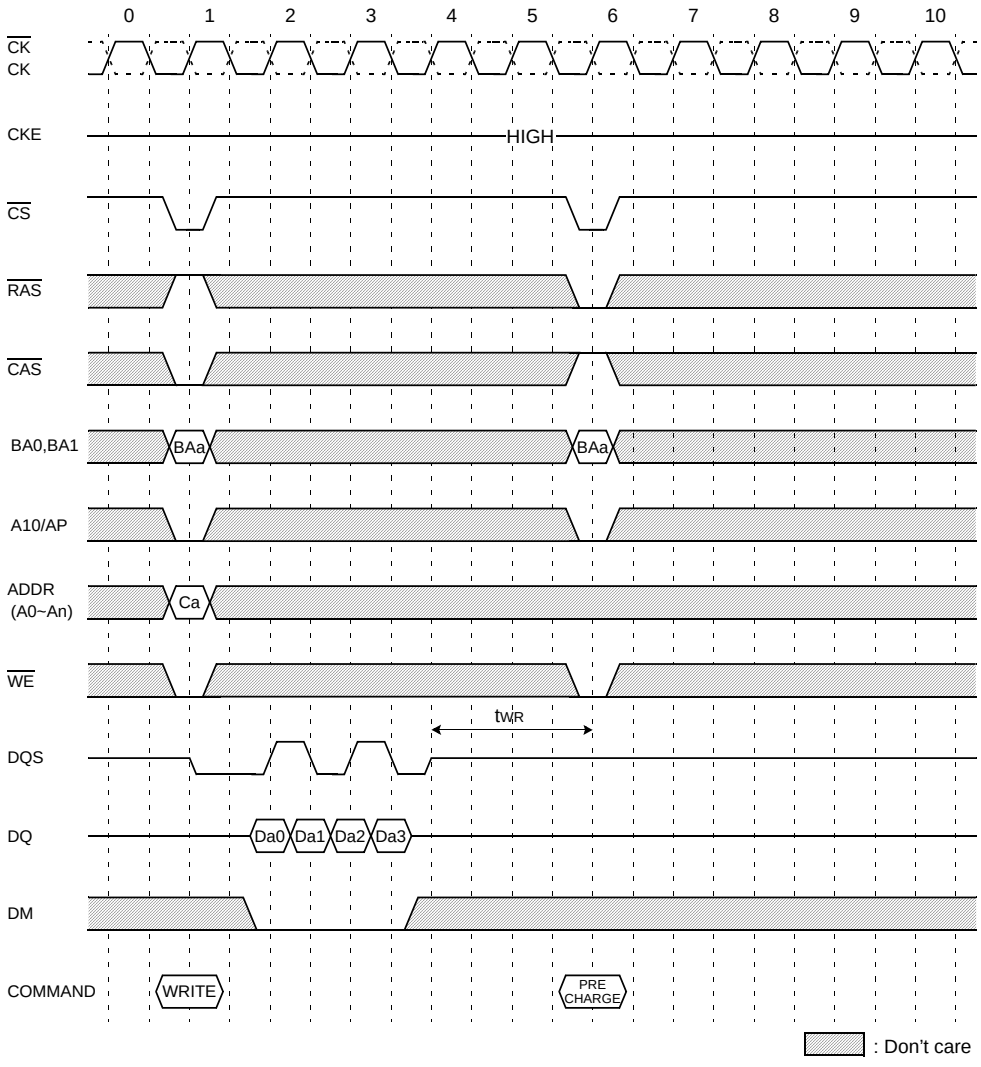
Note: The row active command of the precharge bank can be issued after tRP from this point
The new read/write command of another activated bank can be issued from this point
At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

Write with Auto Precharge (@BL=8)

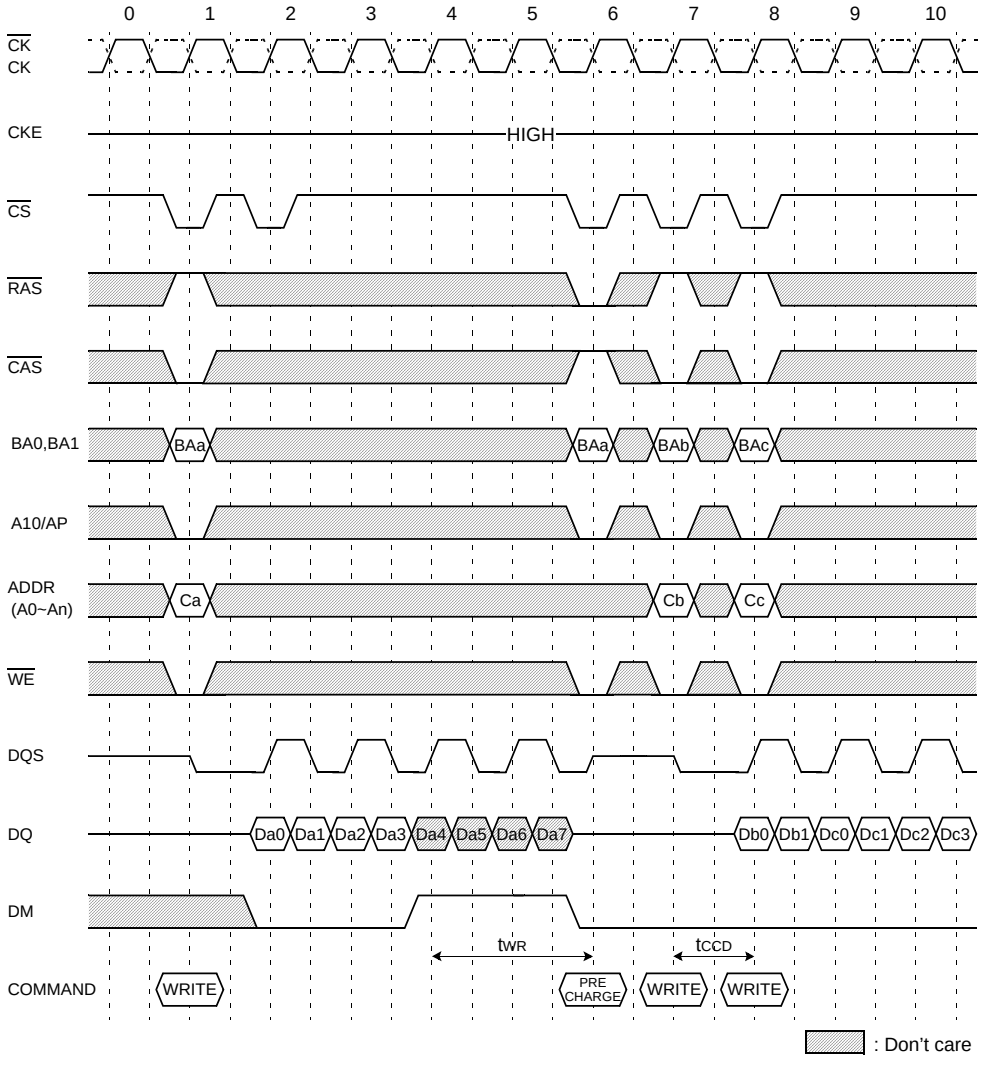


Note: 1. The row active command of the precharge bank can be issued after tRP from this point
The new read/write command of another activated bank can be issued from this point
At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

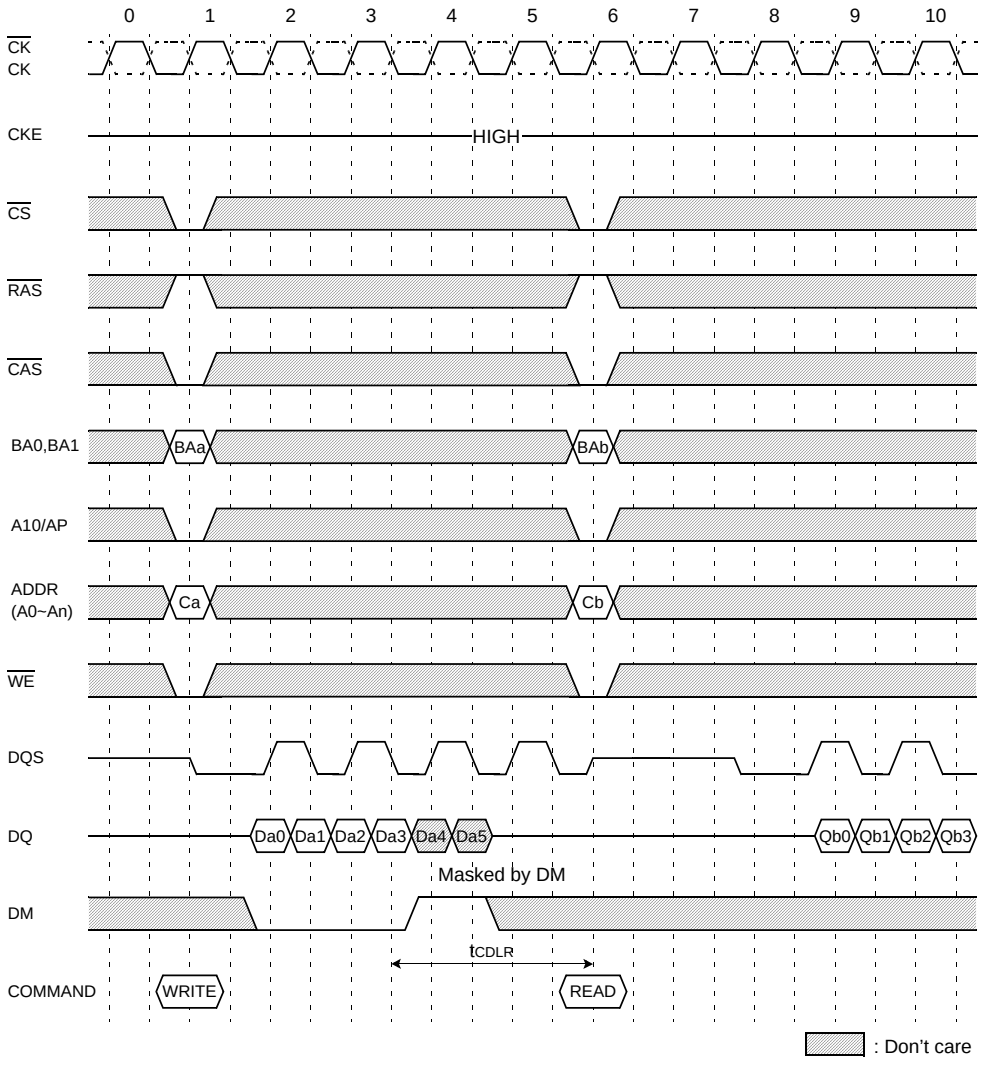
Write followed by Precharge (@BL=4)



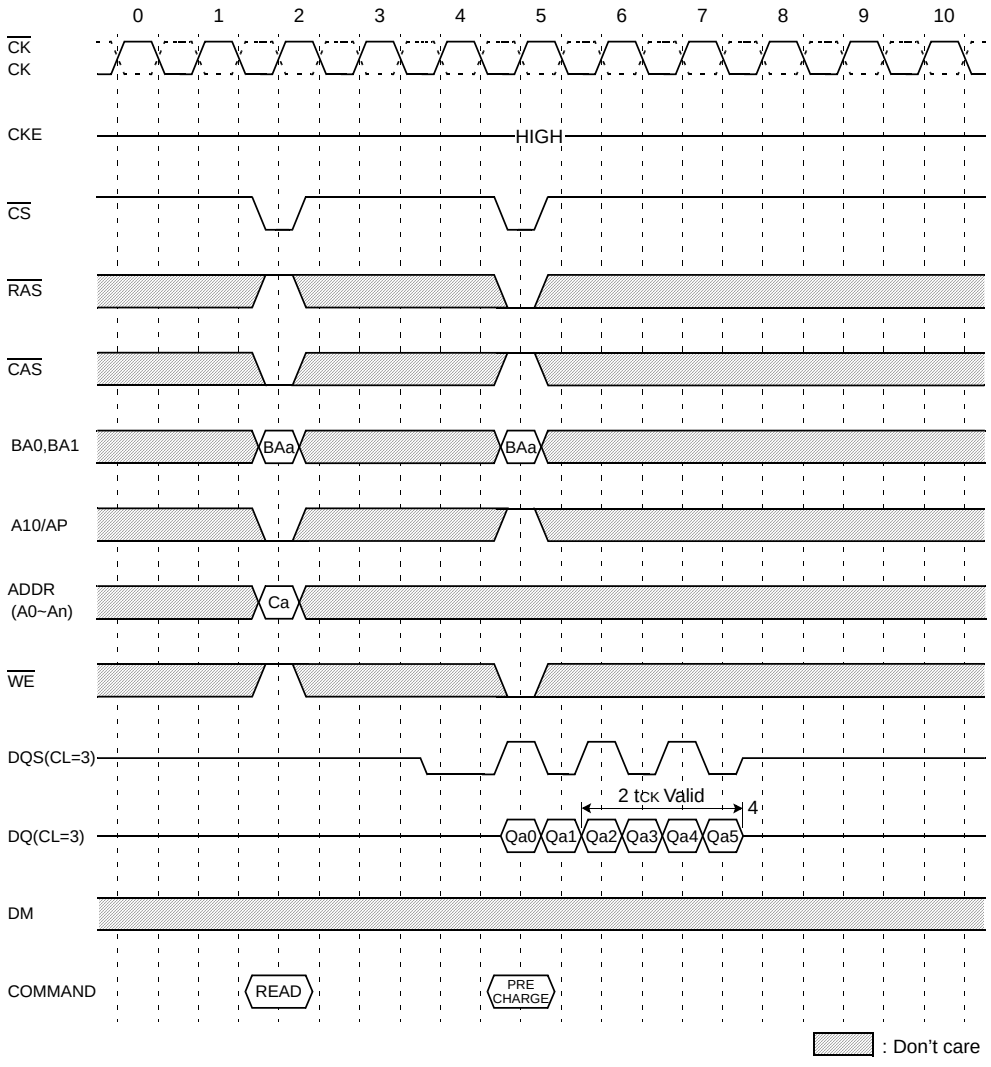
Write Interrupted by Precharge & DM (@BL=8)



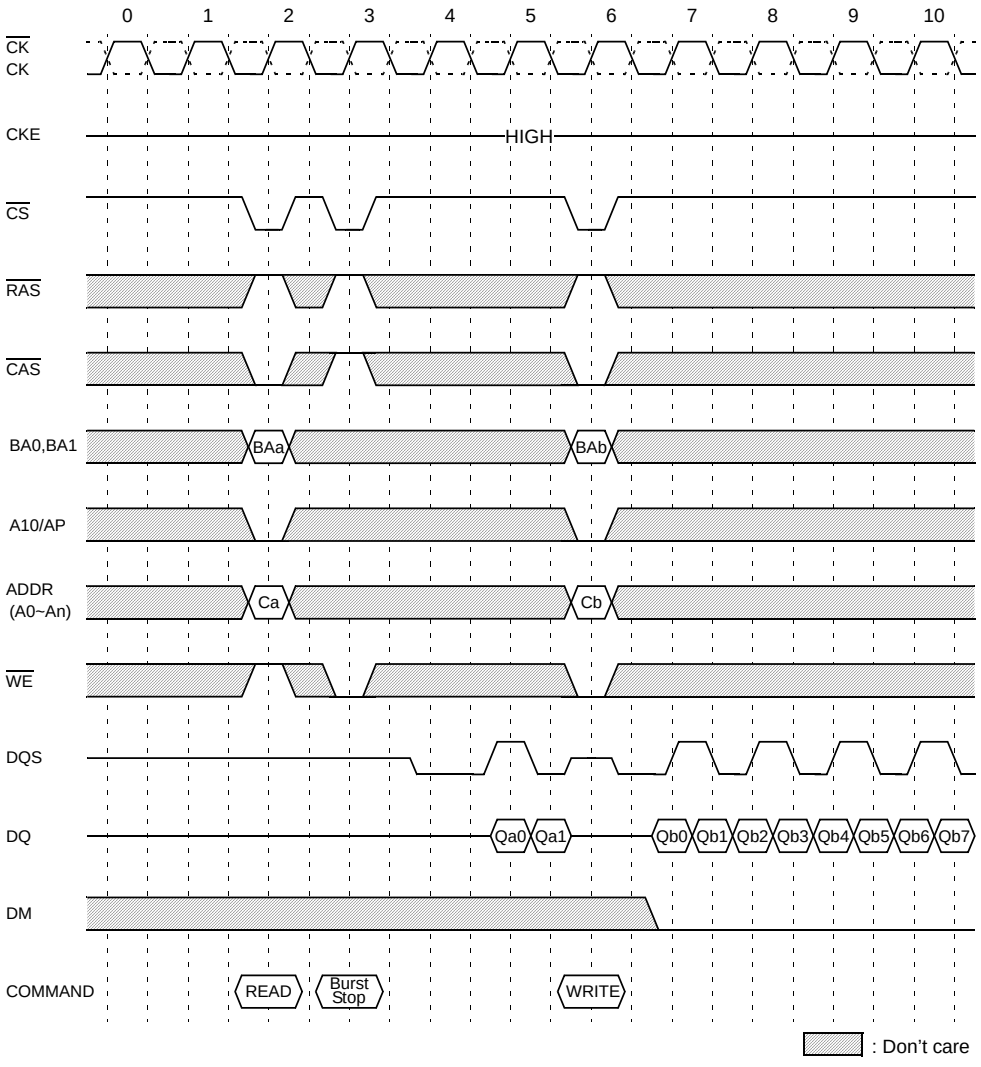
Write Interrupted by a Read (@BL=8, CL=3)



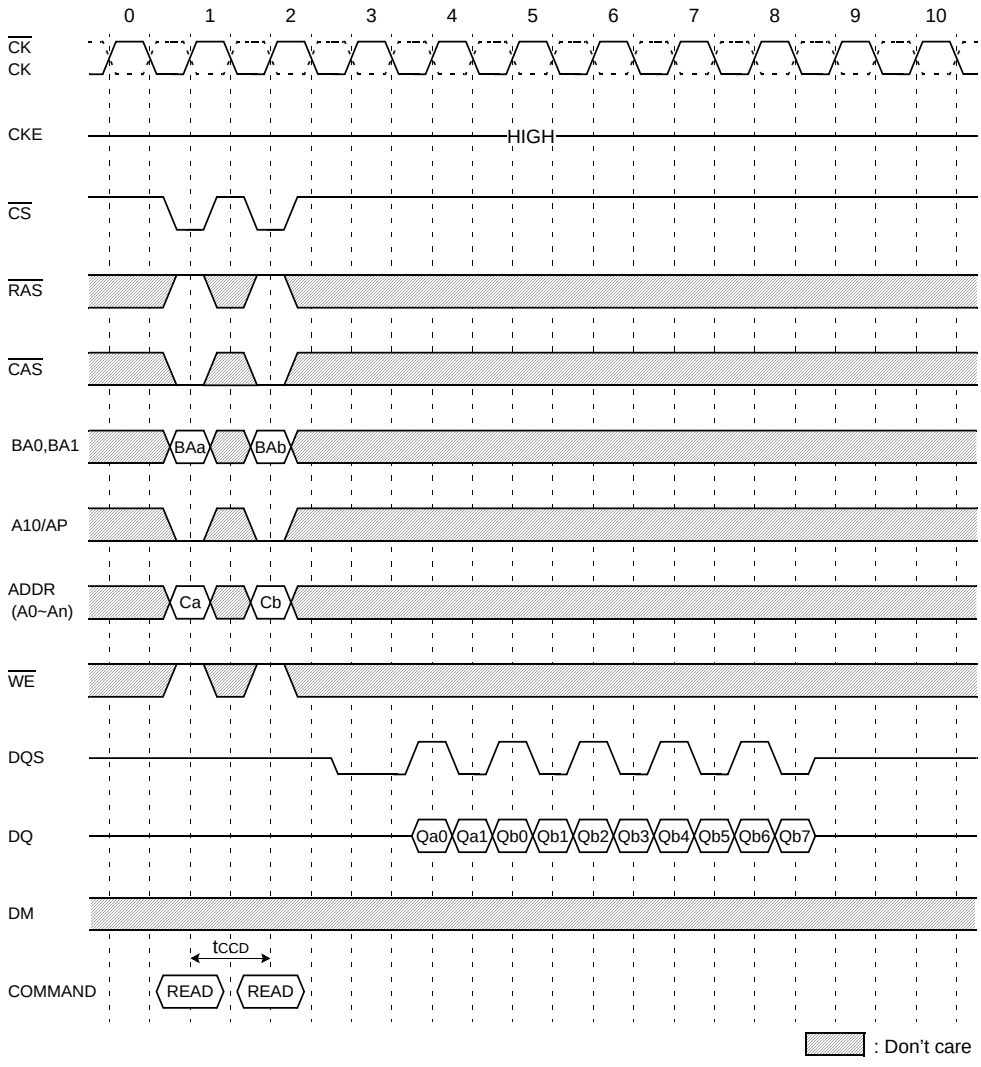
Read Interrupted by Precharge (@BL=8)



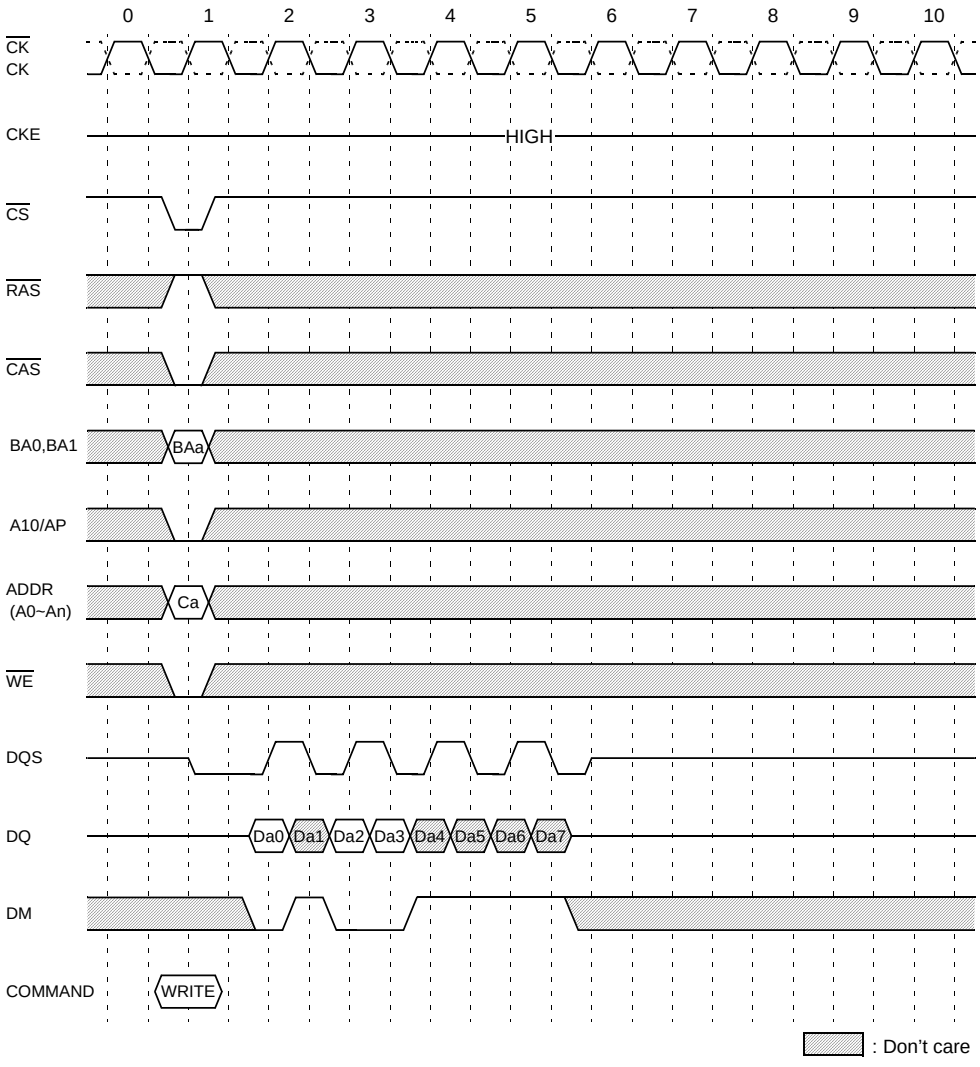
Read Interrupted by a Write & Burst Stop (@BL=8, CL=3)



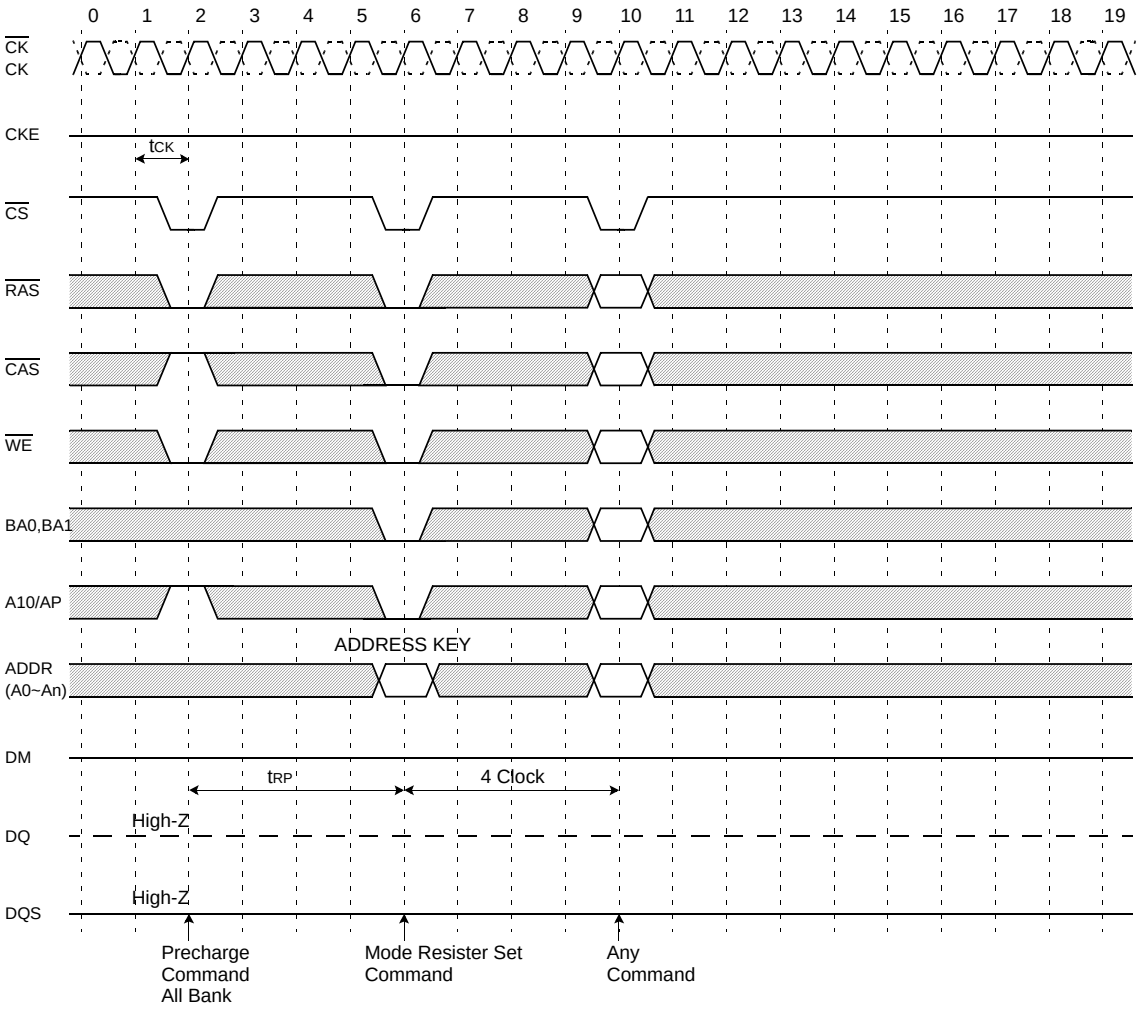
Read Interrupted by a Read (@BL=8, CL=3)



DM Function (@BL=8) only for write



Mode Register Set



Note : Power & Clock must be stable for 200us before precharge all bankes