Document Title

2M x16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
1.0		November 4, 2003	Final

2M x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 2M x16
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs
- Package Type: 55-TBGA-7.50x12.00

GENERAL DESCRIPTION

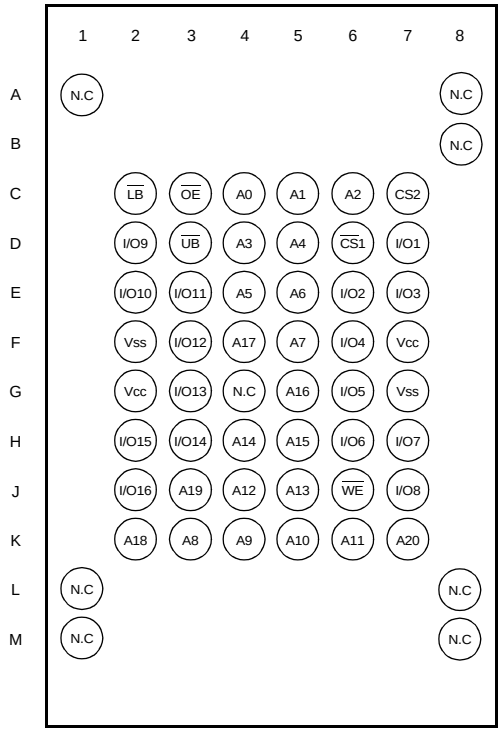
The K6F3216T6M families are fabricated by SAMSUNG′s advanced full CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max.)	Operating (I_{CC1}, Max)	
K6F3216T6M-F	Industrial(-40~85°C)	2.7~3.6V	55[1]/70ns	40μA	7mA	55-TBGA-7.50x12.00

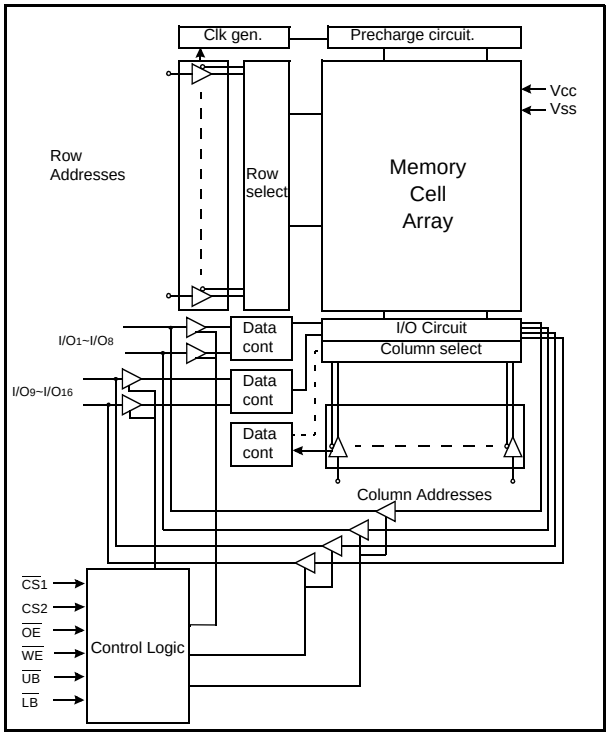
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



55-TBGA: Top View (Ball Down)

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS}_1$, CS_2	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
A_0~A_{20}	Address Inputs	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C	No Connection

PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	**Function**
K6F3216T6M-EF55 K6F3216T6M-EF70	55-TBGA, 55ns, 3.0V/3.3V 55-TBGA, 70ns, 3.0V/3.3V

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$I/O_{1\sim8}$	$I/O_{9\sim16}$	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	X[1]	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to V_{CC}+0.3V(Max. 4.2V)	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.2	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0/3.3	3.6	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

Note:
1. T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

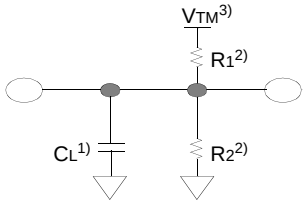
Item	Symbol	Test Conditions		Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH}, V_{IO}=Vss to Vcc		-1	-	1	μA
Average operating current	I_{CC1}	Cycle time=1μs, 100%duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS_2≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	7	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}	70ns	-	-	35	mA
			55ns	-	-	40	
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current (CMOS)	I_{SB1}	Other input =0~Vcc 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or 2) 0V≤CS_2≤0.2V(CS_2 controlled)		-	-	40	μA

1. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage:1.5V
Output load(see right): C_L=100pF+1TTL
C_L=30pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM} =2.8V

AC CHARACTERISTICS (Vcc=2.7~3.3V, Industrial product:T_A=-40 to 85°C)

Parameter List		Symbol	Speed				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	55	-	70	-	ns
	Address access time	t_{AA}	-	55	-	70	ns
	Chip select to output	t_{CO1}, t_{CO2}	-	55	-	70	ns
	Output enable to valid output	t_{OE}	-	25	-	35	ns
	$\overline{UB}$, $\overline{LB}$ valid to data output	t_{BA}	-	55	-	70	ns
	Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	20	0	25	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	0	20	0	25	ns
	Output disable to high-Z output	t_{OHZ}	0	20	0	25	ns
	Output hold from address change	t_{OH}	10	-	10	-	ns
Write	Write cycle time	t_{WC}	55	-	70	-	ns
	Chip select to end of write	t_{CW1}, t_{CW2}	45	-	60	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	45	-	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	45	-	60	-	ns
	Write pulse width	t_{WP}	40	-	50	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	20	ns
	Data to write time overlap	t_{DW}	25	-	30	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

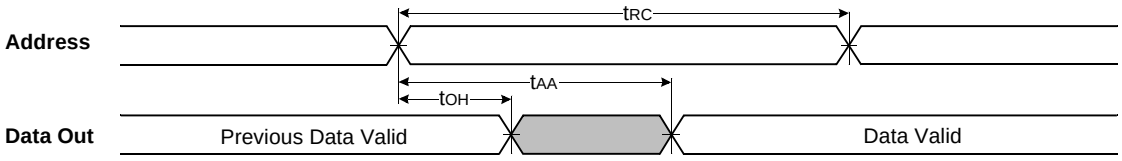
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS_1}$≥Vcc-0.2V[1)], V_{IN}≥0V	1.5	-	3.6	V
Data retention current	IDR	Vcc=1.5V, $\overline{CS_1}$≥Vcc-0.2V[1)], V_{IN}≥0V	-	-	20	µA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

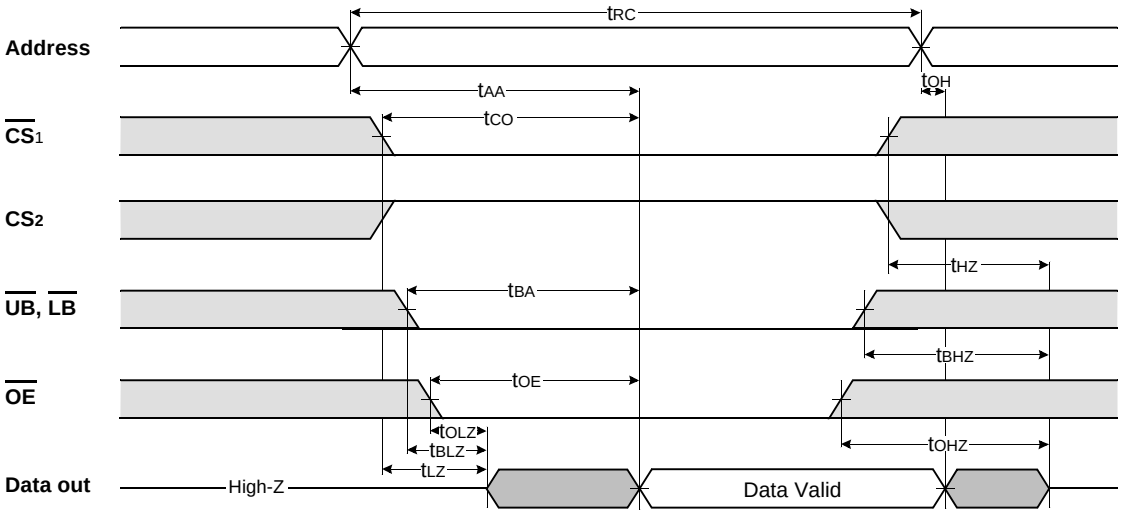
1. 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or
   2) 0≤CS_2≤0.2V(CS_2 controlled)

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}_1$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



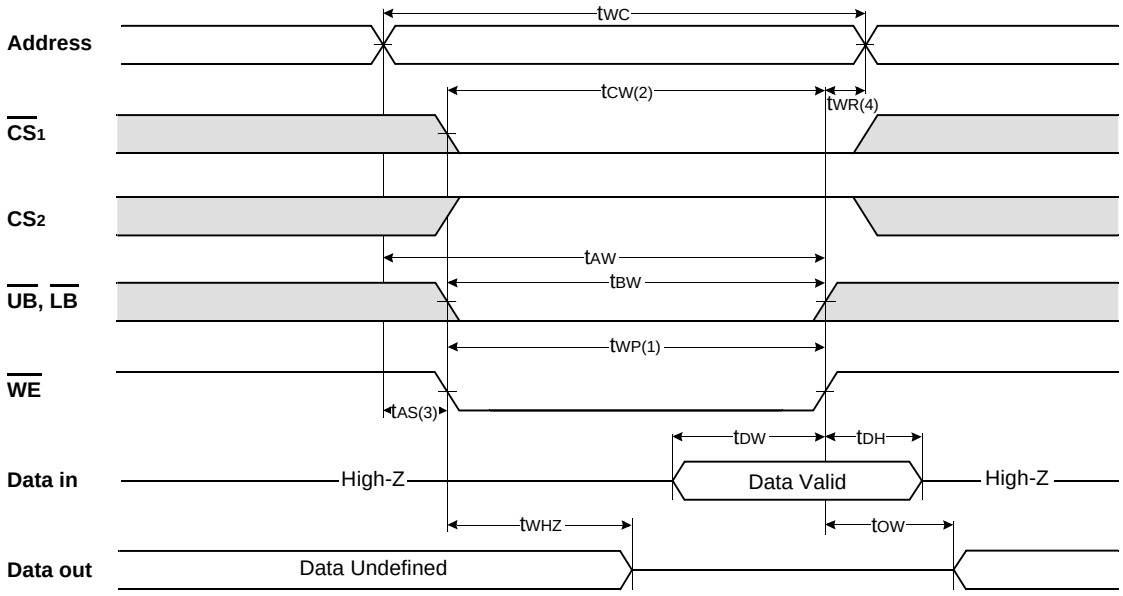
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



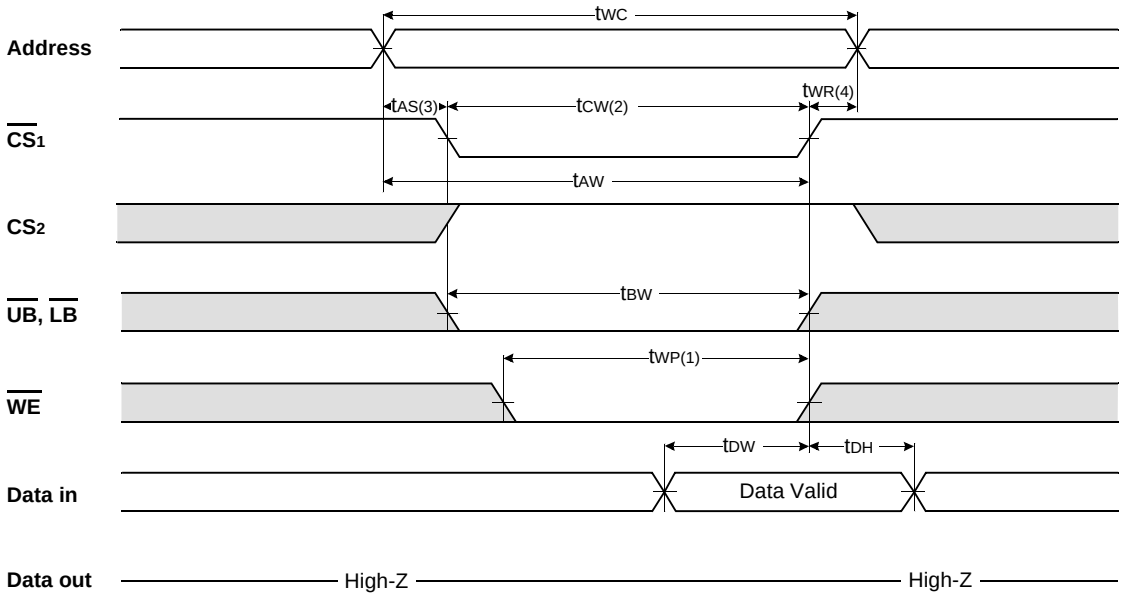
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

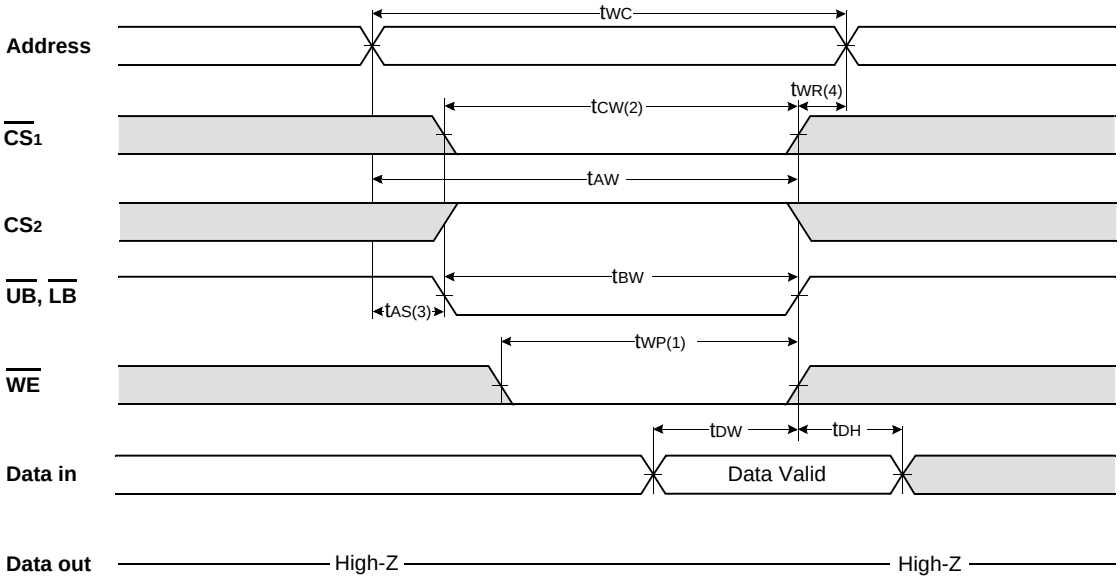
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

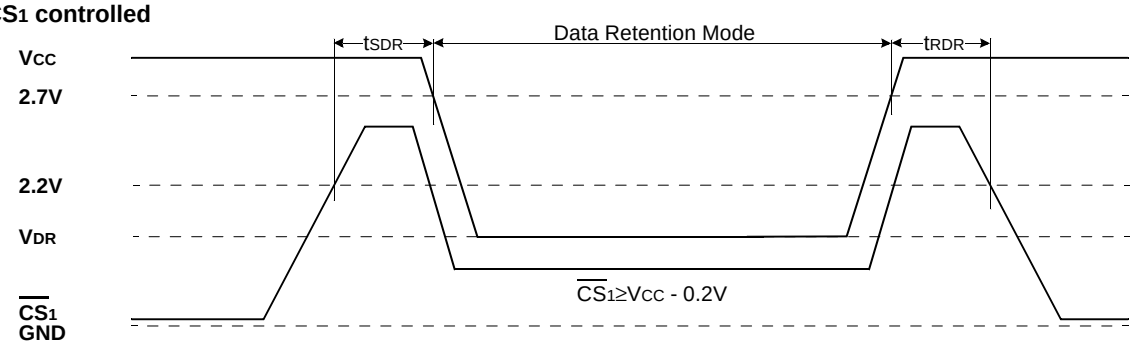


NOTES (WRITE CYCLE)

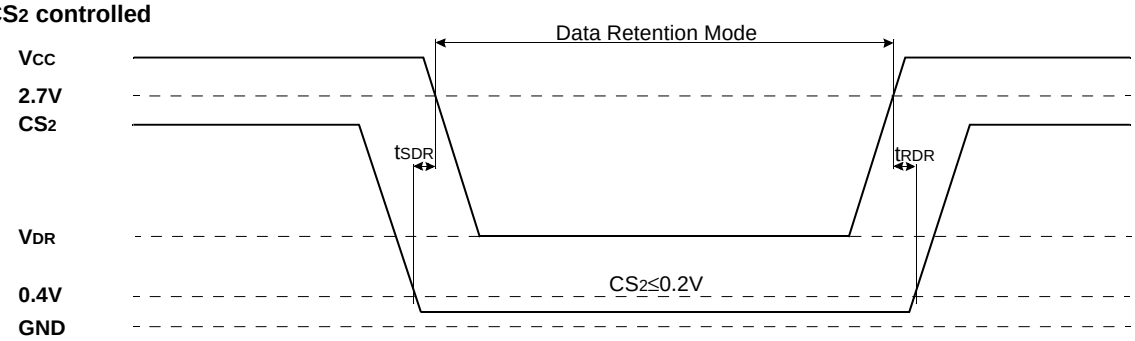
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS_2 controlled

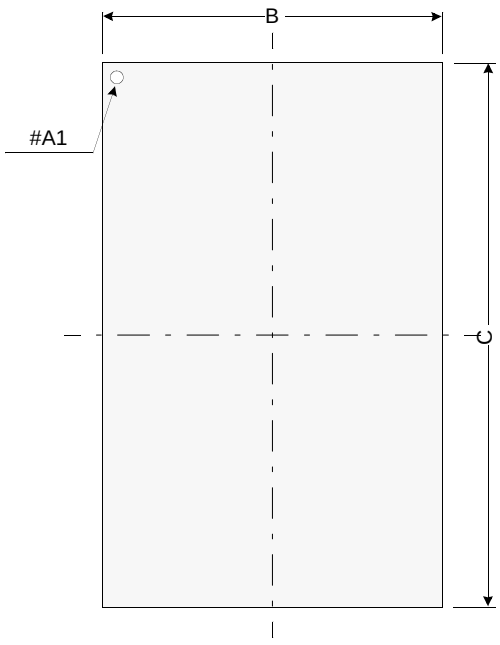


PACKAGE DIMENSION

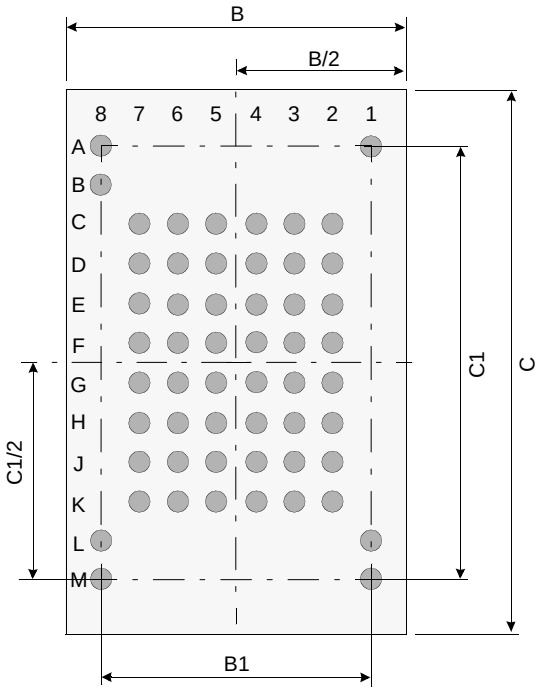
Unit: millimeters

55 BALL TAPE BALL GRID ARRAY(0.75mm ball pitch)

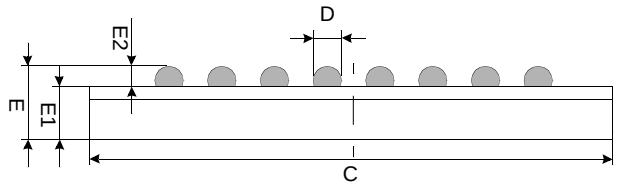
Top View



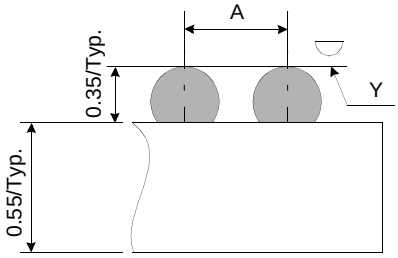
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	7.40	7.50	7.60
B1	-	5.25	-
C	11.90	12.00	12.10
C1	-	8.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 55(12 row x 8 column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)