

K6T4008V1C, K6T4008U1C Family

CMOS SRAM

Document Title

512Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0.0	Initial Draft	January 13, 1998	Advance
0.1	Revised - Speed bin change KM68U4000C : 85/100ns → 70/85/100ns - DC Characteristics change Icc : 5mA at read/write → 4mA at read Icc1 : 3mA → 4mA Icc2 : 35mA → 30mA Isb : 0.5mA → 0.3mA Isb1 : 10μA → 15μA for commercial parts - Add 32-TSOP1-0820	June 12, 1998	Preliminary
0.11	Errata correct - 32-TSOP1-0813 products: T → TG	November 7, 1998	
1.0	Finalize	January 15, 1999	Final

K6T4008V1C, K6T4008U1C Family

CMOS SRAM

512K×8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 512K×8
- Power Supply Voltage
K6T4008V1C Family: 3.0~3.6V
K6T4008U1C Family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-SOP-525, 32-TSOP2-400F/R
32-TSOP1-0820F, 32-TSOP1-0813.4F

GENERAL DESCRIPTION

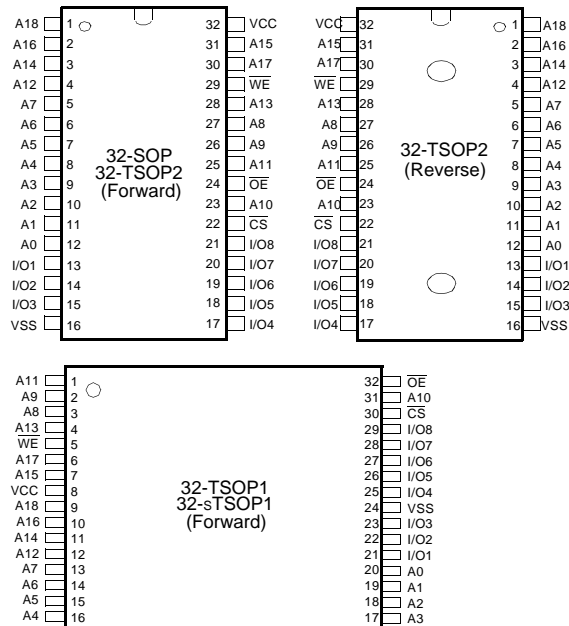
The K6T4008V1C and K6T4008U1C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature range and have various package type for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6T4008V1C-B	Commercial(0~70°C)	3.0~3.6V	70 ¹⁾ /85ns	15μA	30mA	32-SOP 32-TSOP2-F/R 32-TSOP1-F 32-sTSOP1-F
K6T4008U1C-B		2.7~3.3V	70 ¹⁾ /85/100ns			
K6T4008V1C-F	Industrial(-40~85°C)	3.0~3.6V	70 ¹⁾ /85ns	20μA		
K6T4008U1C-F		2.7~3.3V	70 ¹⁾ /85/100ns			

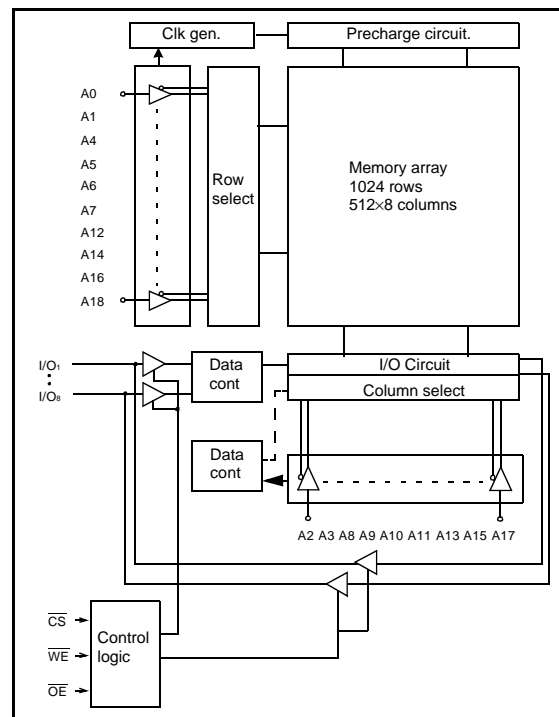
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
\overline{WE}	Write Enable Input	Vss	Ground
\overline{CS}	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
\overline{OE}	Output Enable Input		

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

K6T4008V1C, K6T4008U1C Family

CMOS SRAM

PRODUCT LIST

Commercial Temp Products(0~70°C)		Industrial Temp Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T4008V1C-GB70	32-SOP, 70ns, 3.3V, LL	K6T4008V1C-GF70	32-SOP, 70ns, 3.3V, LL
K6T4008V1C-GB85	32-SOP, 85ns, 3.3V, LL	K6T4008V1C-GF85	32-SOP, 85ns, 3.3V, LL
K6T4008V1C-VB70	32-TSOP2-F, 70ns, 3.3V, LL	K6T4008V1C-VF70	32-TSOP2-F, 70ns, 3.3V, LL
K6T4008V1C-VB85	32-TSOP2-F, 85ns, 3.3V, LL	K6T4008V1C-VF85	32-TSOP2-F, 85ns, 3.3V, LL
K6T4008V1C-MB70	32-TSOP2-R, 70ns, 3.3V, LL	K6T4008V1C-MF70	32-TSOP2-R, 70ns, 3.3V, LL
K6T4008V1C-MB85	32-TSOP2-R, 85ns, 3.3V, LL	K6T4008V1C-MF85	32-TSOP2-R, 85ns, 3.3V, LL
K6T4008V1C-TB70	32-TSOP1-F, 70ns, 3.3V, LL	K6T4008V1C-TF70	32-TSOP1-F, 70ns, 3.3V, LL
K6T4008V1C-TB85	32-TSOP1-F, 85ns, 3.3V, LL	K6T4008V1C-TF85	32-TSOP1-F, 85ns, 3.3V, LL
K6T4008V1C-YB70	32-sTSOP1-F, 70ns, 3.3V, LL	K6T4008V1C-YF70	32-sTSOP1-F, 70ns, 3.3V, LL
K6T4008V1C-YB85	32-sTSOP1-F, 85ns, 3.3V, LL	K6T4008V1C-YF85	32-sTSOP1-F, 85ns, 3.3V, LL
K6T4008U1C-GB70	32-SOP, 70ns, 3.0V, LL	K6T4008U1C-GF70	32-SOP, 70ns, 3.0V, LL
K6T4008U1C-GB85	32-SOP, 85ns, 3.0V, LL	K6T4008U1C-GF85	32-SOP, 85ns, 3.0V, LL
K6T4008U1C-GB10	32-SOP, 100ns, 3.0V, LL	K6T4008U1C-GF10	32-SOP, 100ns, 3.0V, LL
K6T4008U1C-VB70	32-TSOP2-F, 70ns, 3.0V, LL	K6T4008U1C-VF70	32-TSOP2-F, 70ns, 3.0V, LL
K6T4008U1C-VB85	32-TSOP2-F, 85ns, 3.0V, LL	K6T4008U1C-VF85	32-TSOP2-F, 85ns, 3.0V, LL
K6T4008U1C-VB10	32-TSOP2-F, 100ns, 3.0V, LL	K6T4008U1C-VF10	32-TSOP2-F, 100ns, 3.0V, LL
K6T4008U1C-MB70	32-TSOP2-R, 70ns, 3.0V, LL	K6T4008U1C-MF70	32-TSOP2-R, 70ns, 3.0V, LL
K6T4008U1C-MB85	32-TSOP2-R, 85ns, 3.0V, LL	K6T4008U1C-MF85	32-TSOP2-R, 85ns, 3.0V, LL
K6T4008U1C-MB10	32-TSOP2-R, 100ns, 3.0V, LL	K6T4008U1C-MF10	32-TSOP2-R, 100ns, 3.0V, LL
K6T4008U1C-TB70	32-TSOP1-F, 70ns, 3.0V, LL	K6T4008U1C-TF70	32-TSOP1-F, 70ns, 3.0V, LL
K6T4008U1C-TB85	32-TSOP1-F, 85ns, 3.0V, LL	K6T4008U1C-TF85	32-TSOP1-F, 85ns, 3.0V, LL
K6T4008U1C-TB10	32-TSOP1-F, 100ns, 3.0V, LL	K6T4008U1C-TF10	32-TSOP1-F, 100ns, 3.0V, LL
K6T4008U1C-YB70	32-sTSOP1-F, 70ns, 3.0V, LL	K6T4008U1C-YF70	32-sTSOP1-F, 70ns, 3.0V, LL
K6T4008U1C-YB85	32-sTSOP1-F, 85ns, 3.0V, LL	K6T4008U1C-YF85	32-sTSOP1-F, 85ns, 3.0V, LL
K6T4008U1C-YB10	32-sTSOP1-F, 100ns, 3.0V, LL	K6T4008U1C-YF10	32-sTSOP1-F, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

CS	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T4008V1C-L, K6T4008U1C-L
		-40 to 85	°C	K6T4008V1C-P, K6T4008U1C-P

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

K6T4008V1C, K6T4008U1C Family

CMOS SRAM

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T4008V1C Family K6T4008U1C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6T4008V1C, K6T4008U1C Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	K6T4008V1C, K6T4008U1C Family	-0.3 ³⁾	-	0.6	V

Note:

1. Commercial Product : T_A=0 to 70°C, otherwise specified

Industrial Product : T_A=-40 to 85°C, otherwise specified

2. Overshoot : V_{CC}+2.0V in case of pulse width ≤ 30ns

3. Undershoot : -2.0V in case of pulse width ≤ 30ns

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH} , Read	-	-	4	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	-	30	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs = V _{IL} or V _{IH}	-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	-	-	15 ¹⁾	μA

1. Industrial product = 20μA

K6T4008V1C, K6T4008U1C Family

CMOS SRAM

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

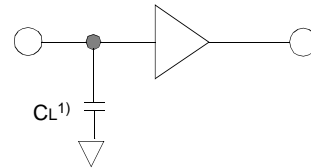
Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right): $C_L = 100\text{pF} + 1\text{TTL}$

$C_L^{(1)} = 30\text{pF} + 1\text{TTL}$

1. 70ns product



1. Including scope and jig capacitance

AC CHARACTERISTICS (K6T4008V1C Family: $V_{CC} = 3.0 \sim 3.6\text{V}$, K6T4008U1C Family: $V_{CC} = 2.7 \sim 3.3\text{V}$ Commercial product: $T_A = 0$ to 70°C , Industrial product: $T_A = -40$ to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tdw	30	-	35	-	40	-	ns
	Data hold from write time	tdH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns

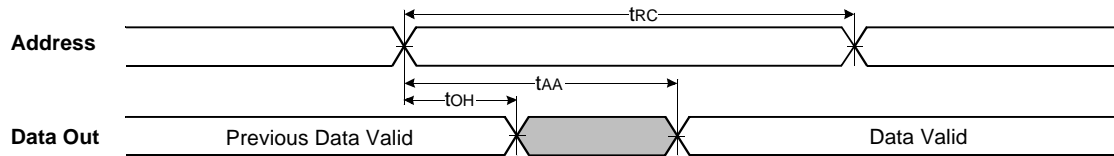
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC} = 3.0\text{V}$, $\overline{CS} \geq V_{CC} - 0.2\text{V}$	-	0.5	15 ¹⁾	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

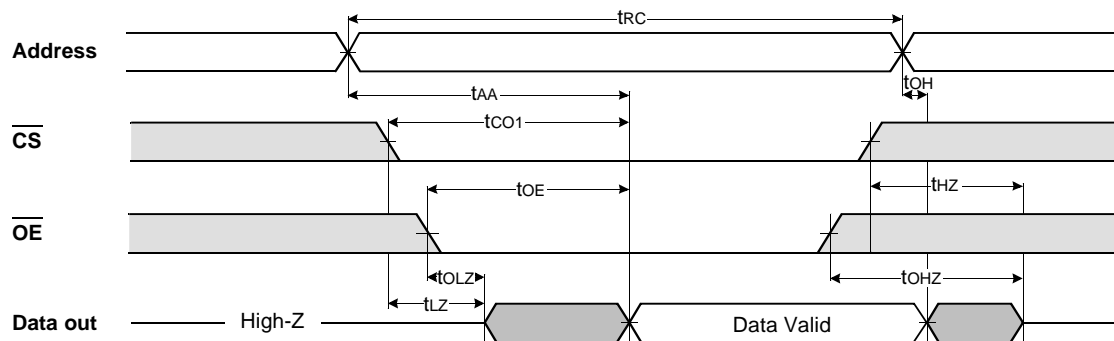
1. Industrial product = 20μA

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



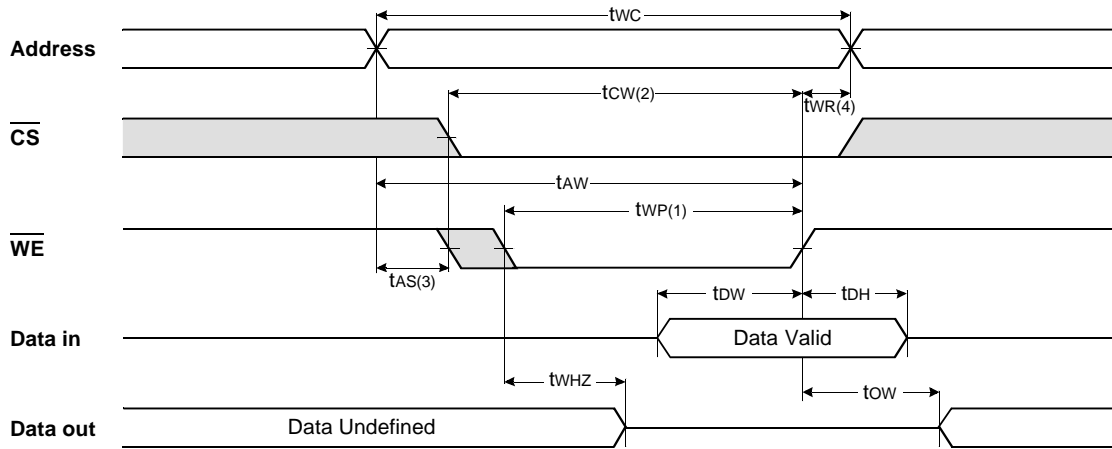
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



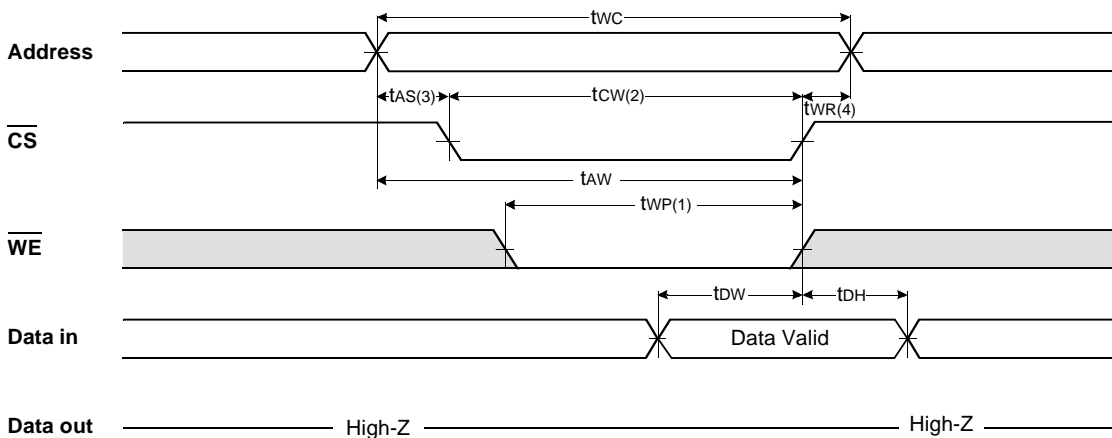
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)

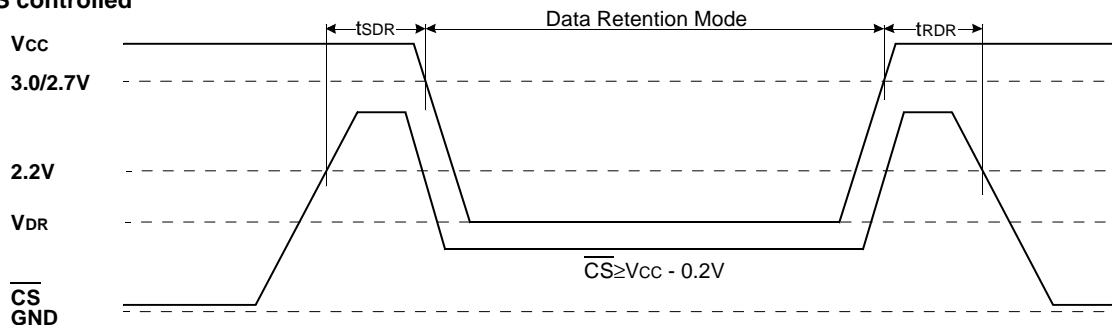


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going Low and \overline{WE} going low : A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

\overline{CS} controlled



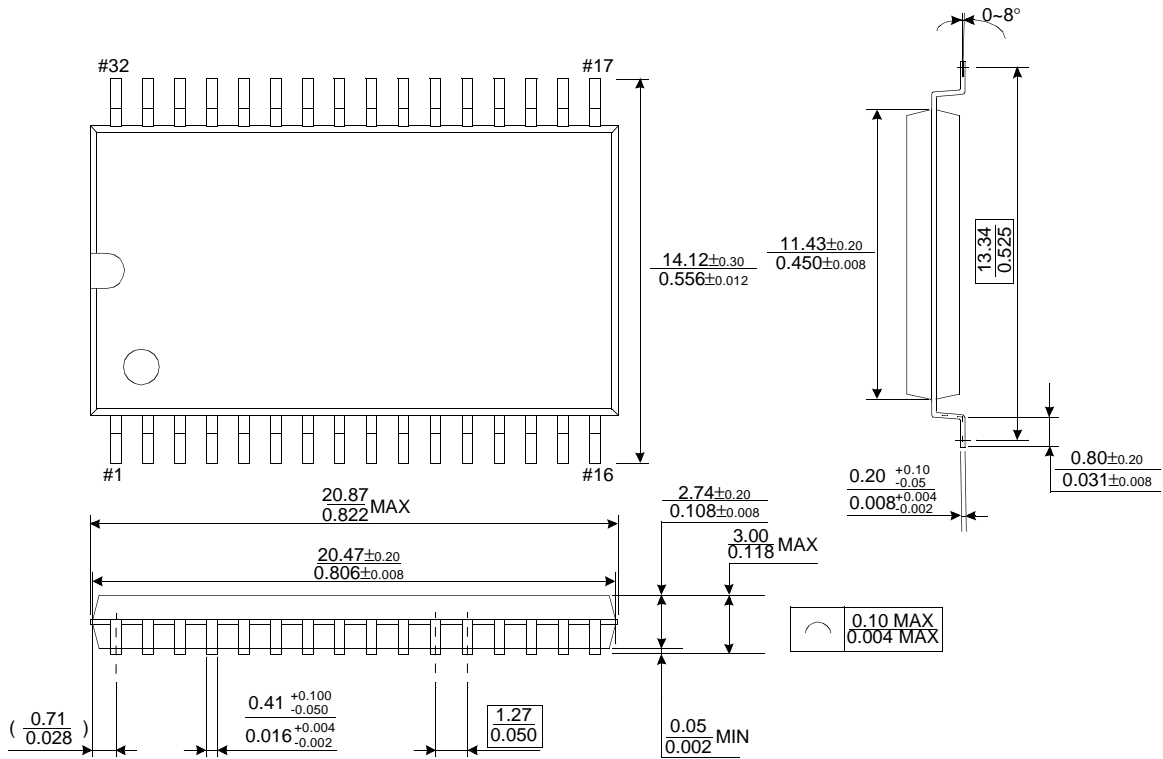
K6T4008V1C, K6T4008U1C Family

CMOS SRAM

PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



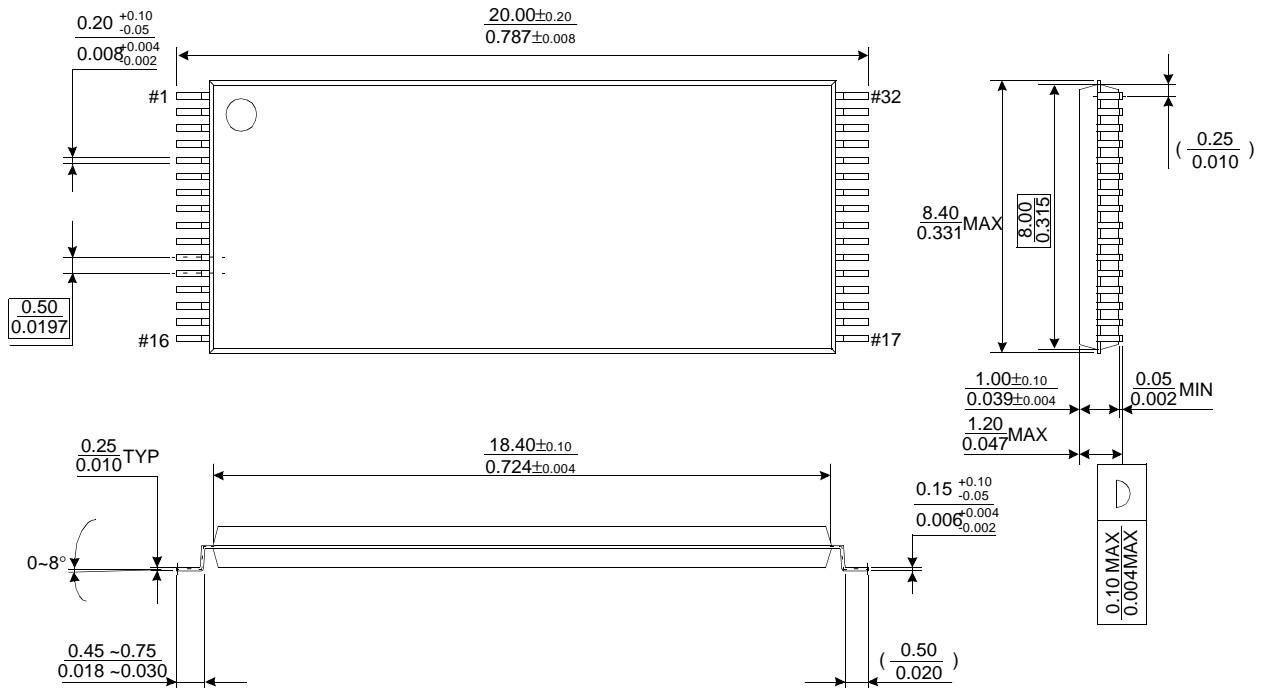
K6T4008V1C, K6T4008U1C Family

CMOS SRAM

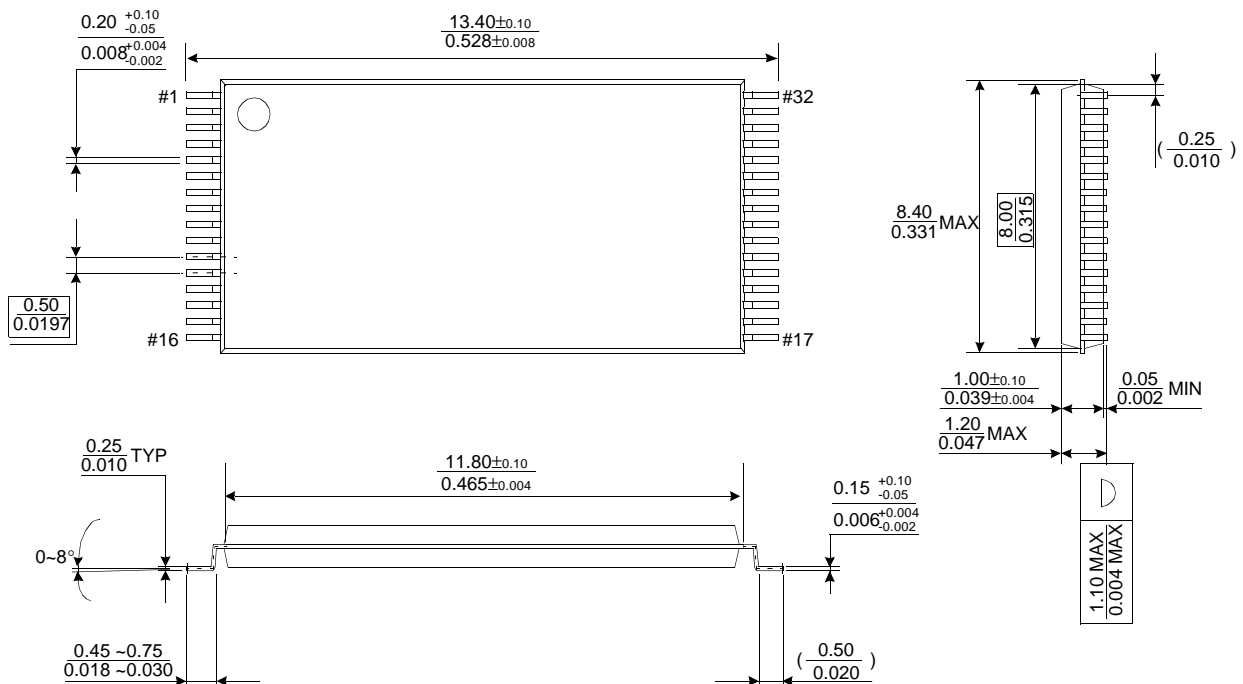
PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



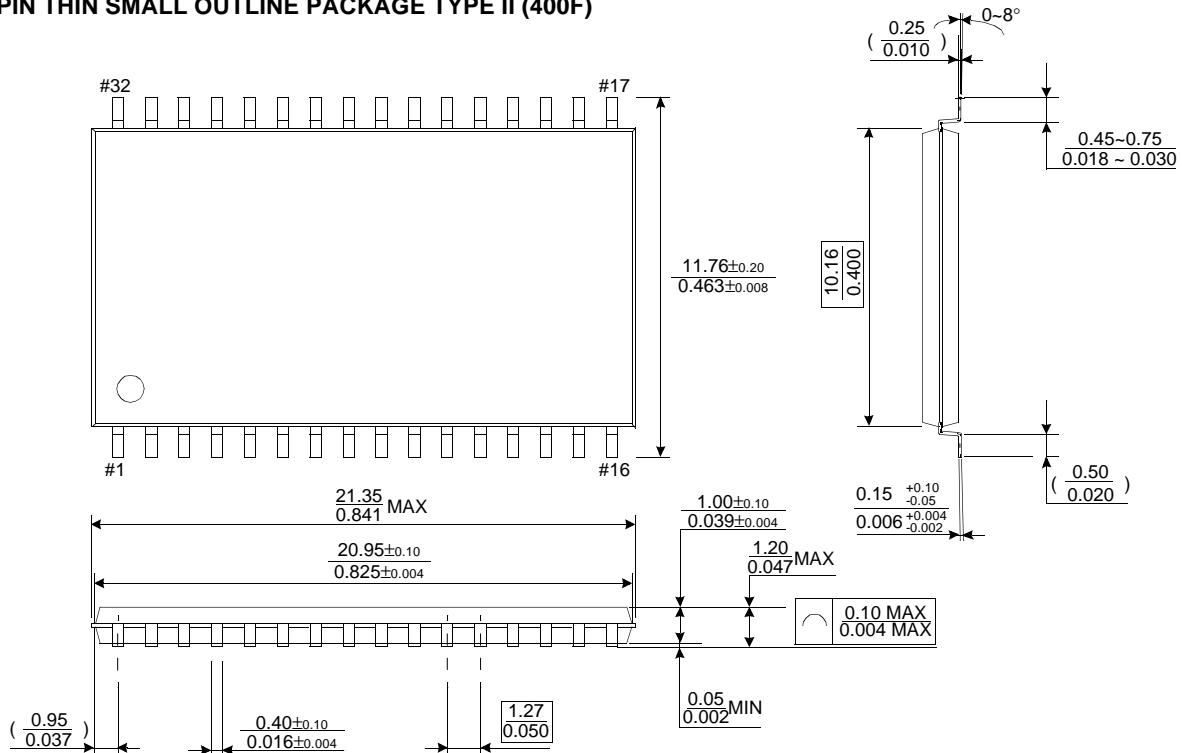
K6T4008V1C, K6T4008U1C Family

CMOS SRAM

PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

