Document Title

256Kx36 & 512Kx18-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial draft	April. 10 . 1998	Preliminary
0.1	Change DC Characteristics. I_{SB} value from 60mA to 90mA at -8 I_{SB} value from 50mA to 80mA at -9 I_{SB} value from 40mA to 70mA at -10 I_{SB1} value from 10mA to 30mA I_{SB2} value from 10mA to 30mA	Aug. 31. 1998	Preliminary
0.2	1. Changed t_{CD} from 8.0ns to 8.5ns at -8 2. Changed t_{CYC} from 13.0ns to 12.0ns at -10 3. Changed DC condition at Icc and parameters I_{CC} ; from 300mA to 350mA at -8, from 260mA to 300mA at -9, from 220mA to 260mA at -10, I_{SB} ; from 90mA to 130mA at -8, from 80mA to 120mA at -9, from 70mA to 110mA at -10,	Sep. 09. 1998	Preliminary
0.3	1. ADD 119BGA(7x17 Ball Grid Array Package) . 2. ADD x32 organization.	Oct. 15. 1998	Preliminary
0.4	Add V_{DDQ} Supply voltage(2.5V)	Dec. 10. 1998	Preliminary
0.5	Changed V_{OL} Max value from 0.2V to 0.4V at 2.5V I/O.	Dec. 23. 1998	Preliminary
1.0	1. Final Spec Release. 2. Remove x32 organization.	Jan. 29. 1999	Final
2.0	1. Remove V_{DDQ} supply voltage(2.5V)	Feb. 25. 1999	Final
3.0	1. Changed I_{CC} from 350mA to 330mA at -8. 2. Add bin -7. (tCD 7.5ns).	Mar. 30. 1999	Final
4.0	1. Add V_{DDQ} supply voltage(2.5V)	May. 13. 1999	Final
5.0	1. Changed tCYC from 12ns to 10ns at -9.	Nov. 19. 1999	Final

256Kx36 & 512Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package)

FAST ACCESS TIMES

PARAMETER	Symbol	-75	-85	-90	-10	Unit
Cycle Time	t_{CYC}	8.5	10	10	12	ns
Clock Access Time	t_{CD}	7.5	8.5	9.0	10.0	ns
Output Enable Access Time	t_{OE}	3.5	3.5	3.5	3.5	ns

GENERAL DESCRIPTION

The K7B803625M and K7B801825M are 9,437,184-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 256K(512K) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with CS1 high, ADSP is blocked to control signals.

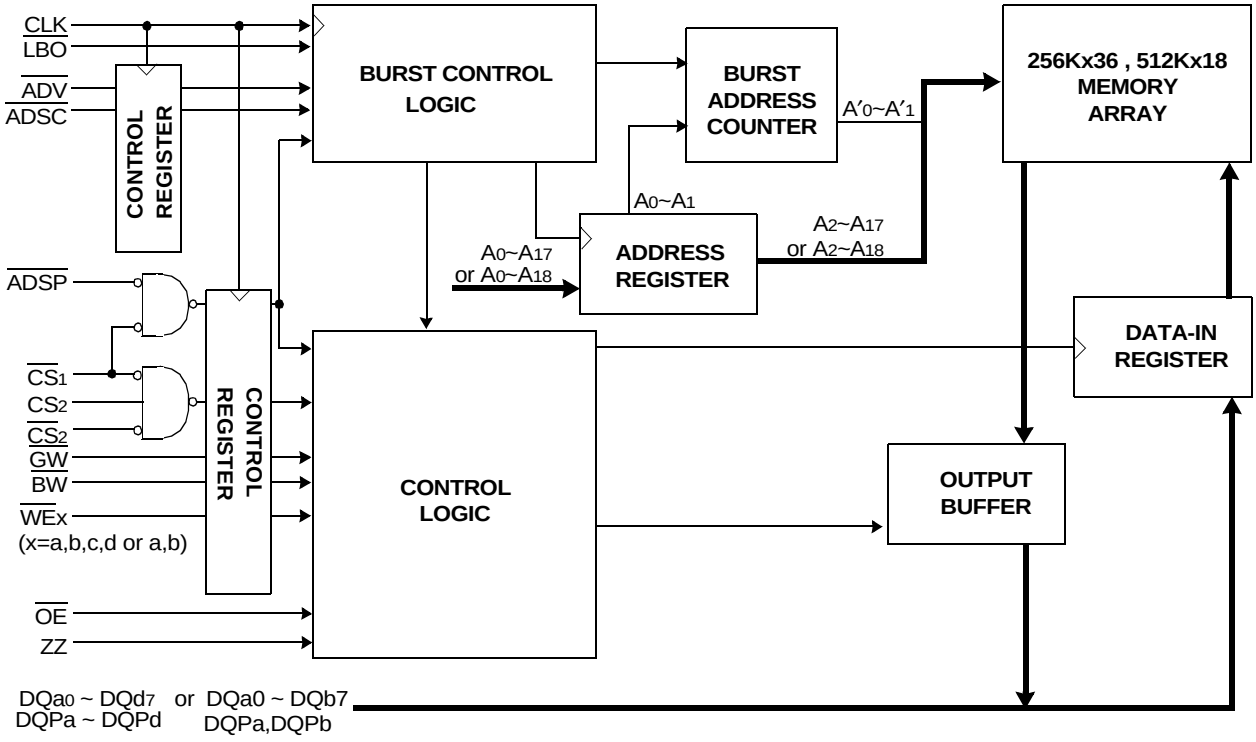
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

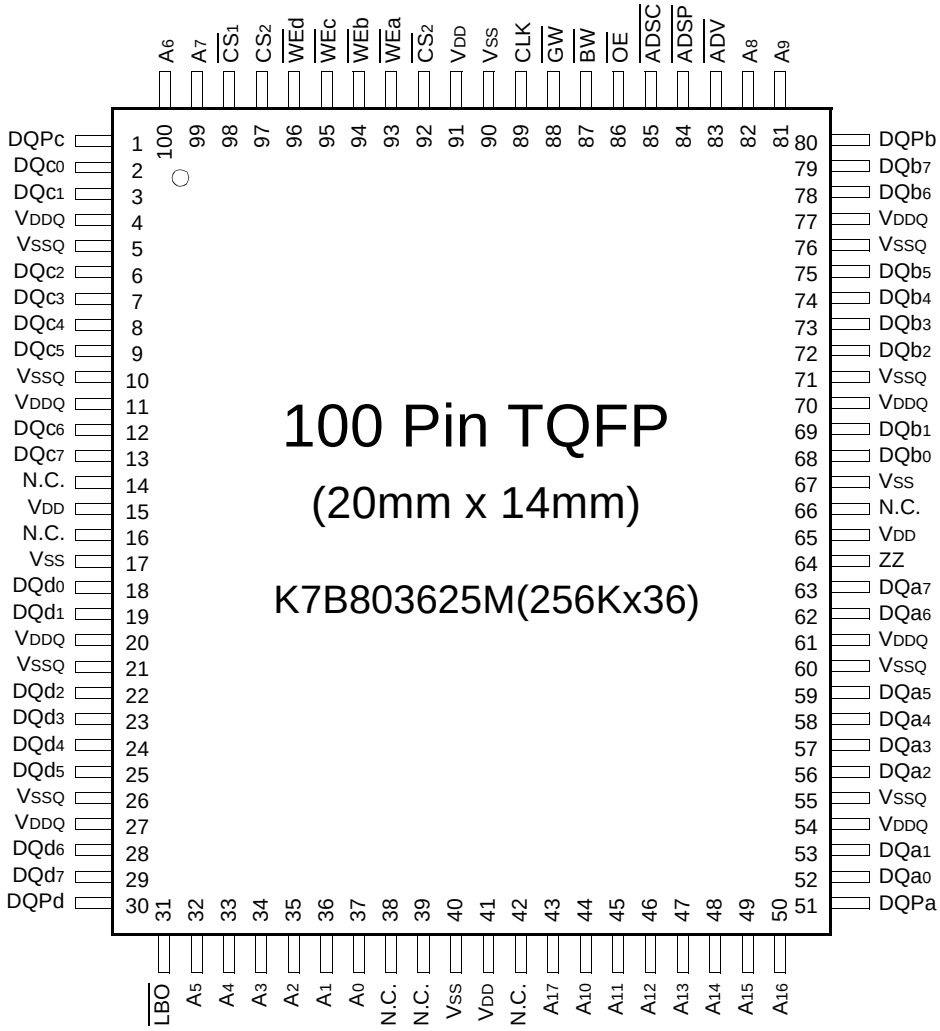
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B803625M and K7B801825M are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

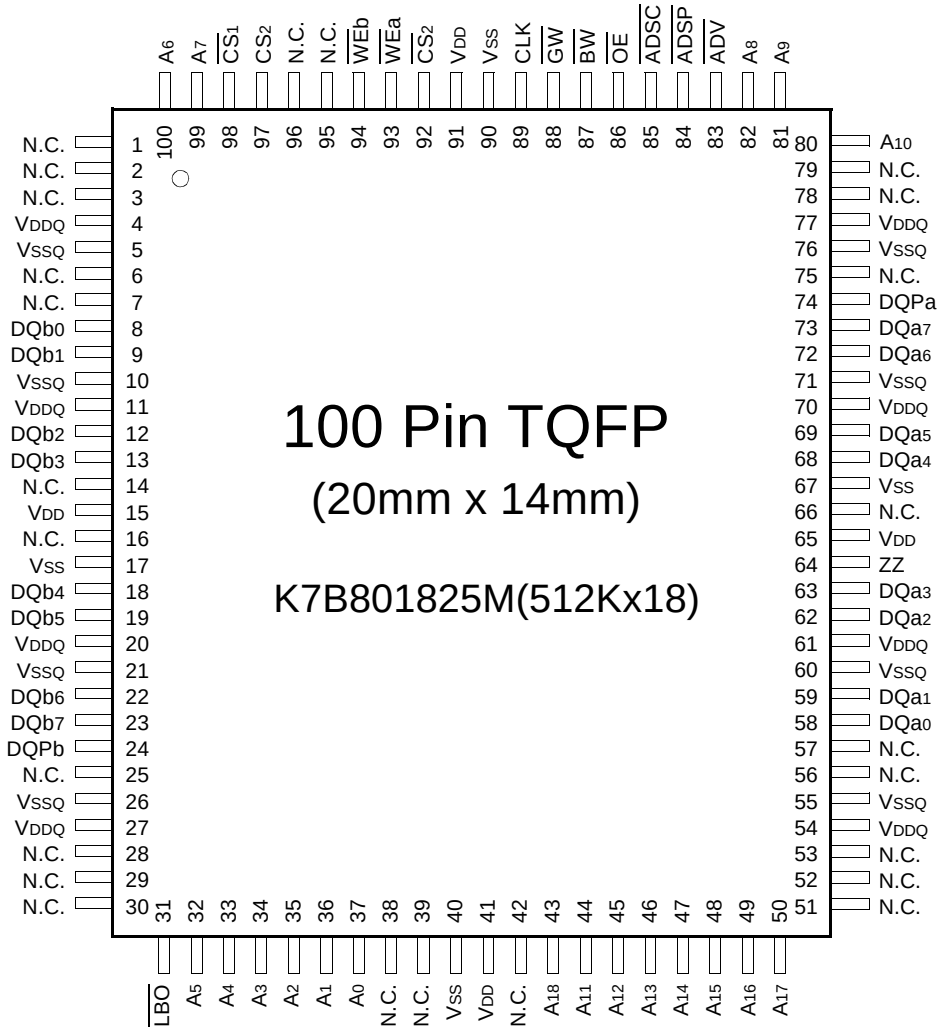


PIN

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{17}	Address Inputs	32,33,34,35,36,37,43	V_{DD}	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,49,50	V_{SS}	Ground	17,40,67,90
		81,82,99,100	N.C.	No Connect	14,16,38,39,42,66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa_0~a_7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb_0~b_7		68,69,72,73,74,75,78,79
$\overline{CLK}$	Clock	89	DQc_0~c_7		2,3,6,7,8,9,12,13
$\overline{CS_1}$	Chip Select	98	DQd_0~d_7		18,19,22,23,24,25,28,29
CS_2	Chip Select	97	DQPa~Pd		51,80,1,30
$\overline{CS_2}$	Chip Select	92	V_{DDQ}	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{WE}$x(x=a,b,c,d)	Byte Write Inputs	93,94,95,96		(2.5V or 3.3V)	
$\overline{OE}$	Output Enable	86	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
2. The pin 42 is reserved for address bit for the 16Mb .

PIN CONFIGURATION(TOP VIEW)



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		44,45,46,47,48,49,50	V_{SS}	Ground	17,40,67,90
		80,81,82,99,100	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29,
$\overline{ADV}$	Burst Address Advance	83			30,38,39,42,51,52,53,56,
$\overline{ADSP}$	Address Status Processor	84			57,66,75,78,79,95,96
$\overline{ADSC}$	Address Status Controller	85			
$\overline{CLK}$	Clock	89	DQa_0 ~ a_7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_1}$	Chip Select	98	DQb_0 ~ b_7		8,9,12,13,18,19,22,23
$\overline{CS_2}$	Chip Select	97	DQPa, Pb		74,24
$\overline{CS_2}$	Chip Select	92	V_{DDQ}	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{WE}$x	Byte Write Inputs	93,94		(2.5V or 3.3V)	
$\overline{OE}$	Output Enable	86	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
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$\overline{LBO}$	Burst Mode Control	31			

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
2. The pin 42 is reserved for address bit for the 16Mb .

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B803625M(256Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CS2	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CS_1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{WEc}$	$\overline{ADV}$	$\overline{WEb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{GW}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{WEd}$	NC	$\overline{WEa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A_1*	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A_0*	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply(+3.3V)
A_0, A_1	Burst Count Address	V_{SS}	Ground
$\overline{ADV}$	Burst Address Advance	N.C.	No Connect
$\overline{ADSP}$	Address Status Processor		
$\overline{ADSC}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQc	Data Inputs/Outputs
CS_2	Chip Select	DQd	Data Inputs/Outputs
$\overline{WEx}$ (x=a,b,c,d)	Byte Write Inputs	DQPa~Pd	Data Inputs/Outpus
		V_{DDQ}	Output Power Supply (2.5V or 3.3V)
$\overline{OE}$	Output Enable		
$\overline{GW}$	Global Write Enable		
$\overline{BW}$	Byte Write Enable		
$\overline{ZZ}$	Power Down Input		
$\overline{LBO}$	Burst Mode Control		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B801825M(512Kx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CS2	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CS_1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{WE}$b	$\overline{ADV}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{WE}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A_1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A_0*	V_{SS}	NC	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply(+3.3V)
A_0,A_1	Burst Count Address	V_{SS}	Ground
$\overline{ADV}$	Burst Address Advance	N.C.	No Connect
$\overline{ADSP}$	Address Status Processor		
$\overline{ADSC}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQPa~Pb	Data Inputs/Outpus
CS_2	Chip Select		
$\overline{WE}$x (x=a,b)	Byte Write Inputs	V_{DDQ}	Output Power Supply (2.5V or 3.3V)
$\overline{OE}$	Output Enable		
$\overline{GW}$	Global Write Enable		
$\overline{BW}$	Byte Write Enable		
$\overline{ZZ}$	Power Down Input		
$\overline{LBO}$	Burst Mode Control		

FUNCTION DESCRIPTION

The K7B803625M and K7B801825M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B803625M, a 256Kx36 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb, $\overline{WE}$c controls DQc0 ~ DQc7 and DQPc and $\overline{WE}$d controls DQd0 ~ DQd7 and DQPd.

$\overline{CS_1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to 4.6	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ}+0.5	V
Power Dissipation	P_D	1.4	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Notes :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

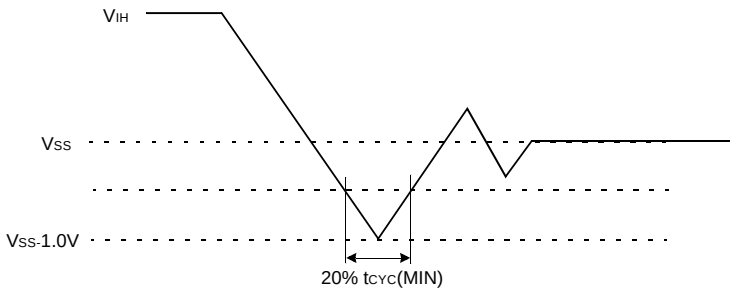
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***Note :** Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled, V_{out}=V_{SS} to V_{DDQ}		-2	+2	µA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL} , Cycle Time ≥ t_{CYC} Min	-75	-	350	mA	1,2
			-85	-	330		
			-90	-	300		
			-10	-	260		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-75	-	140	mA	
			-85	-	130		
			-90	-	120		
			-10	-	120		
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	30	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	30	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.5**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.5**	V	3

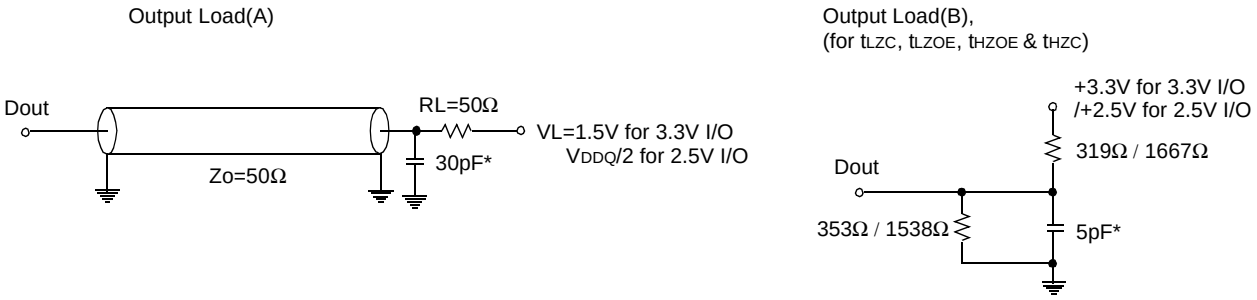
Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V



TEST CONDITIONS

(V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=3.3V+0.165/-0.165V or V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0to70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1



* Including Scope and Jig Capacitance

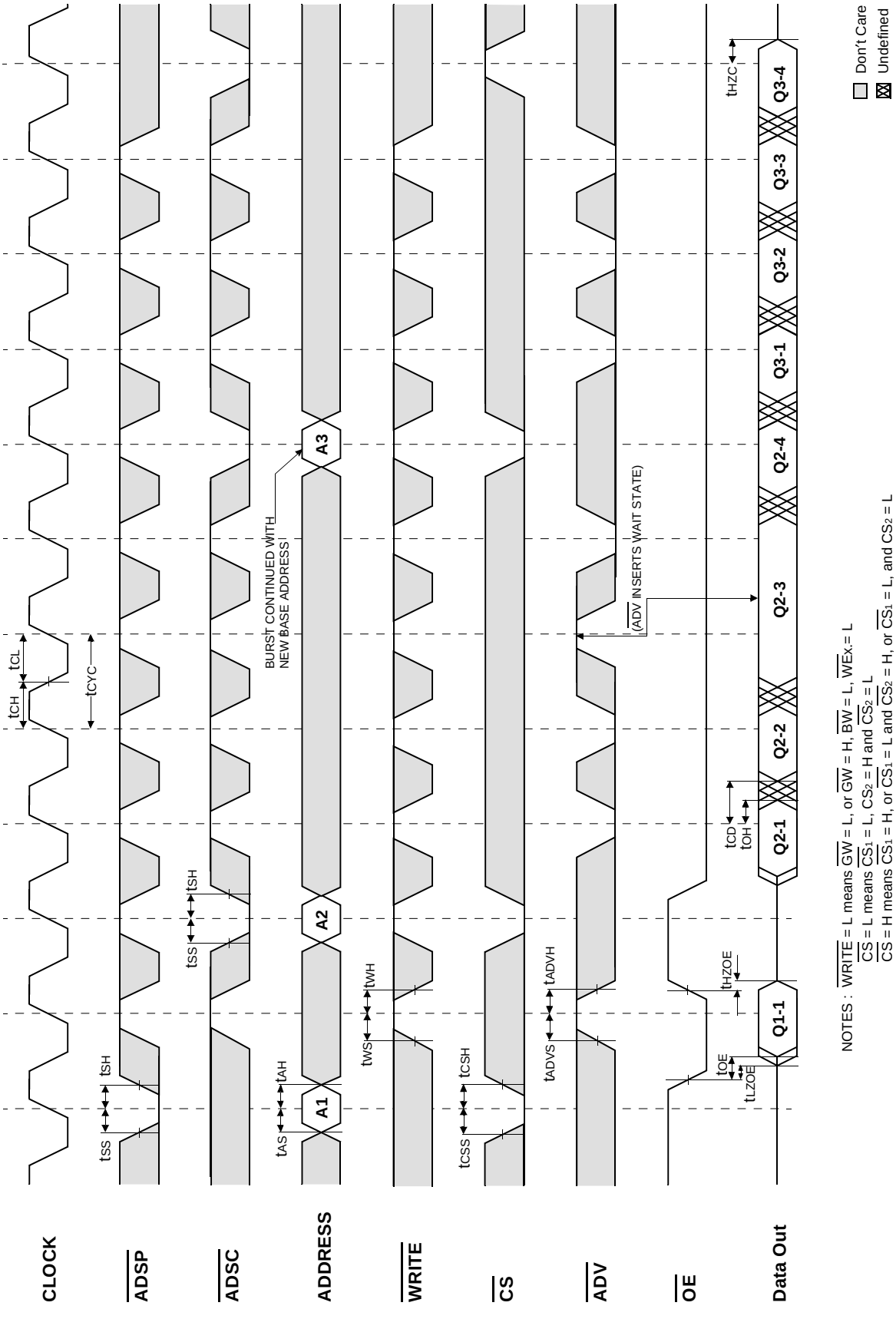
Fig. 1

AC TIMING CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

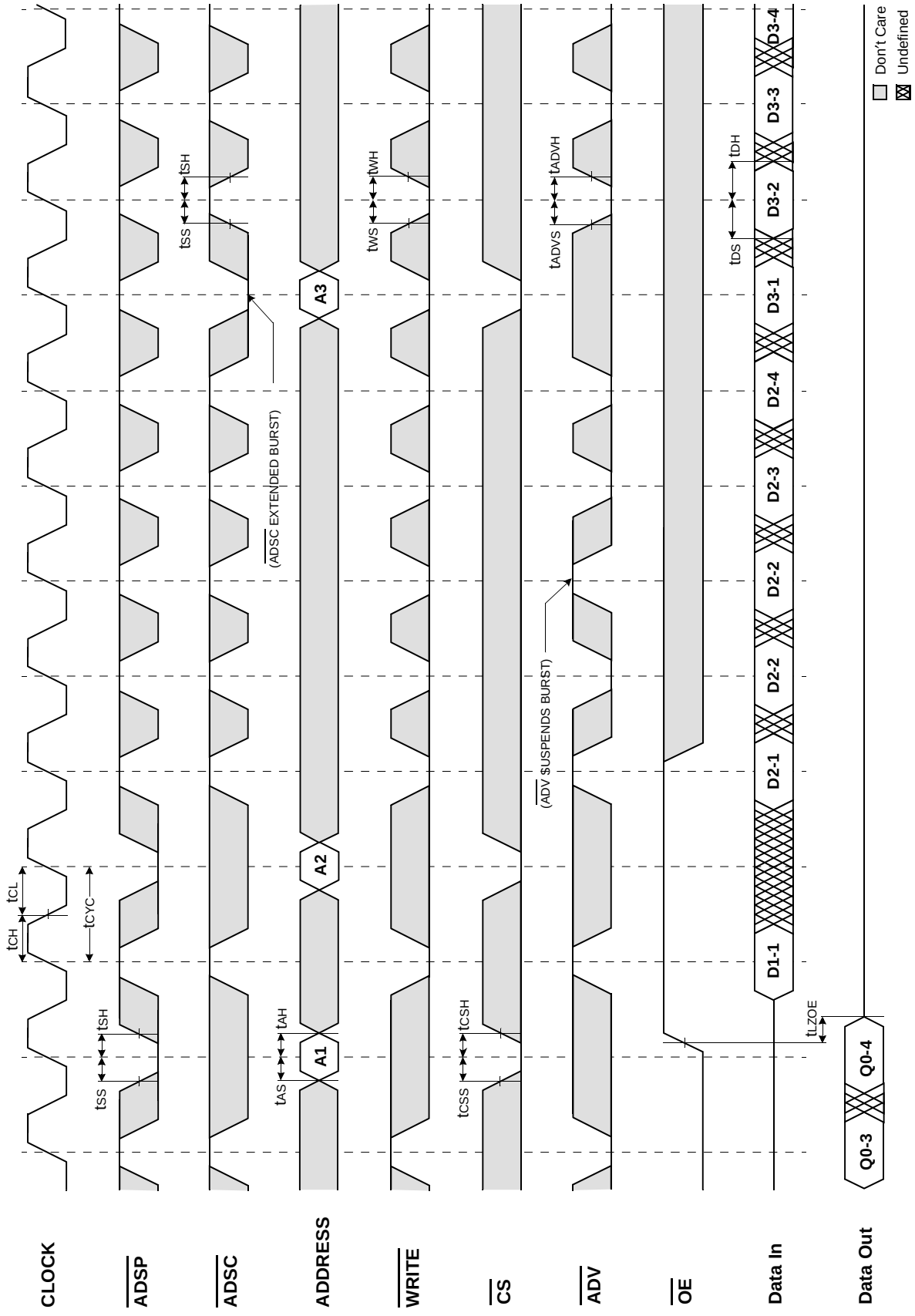
PARAMETER	SYMBOL	-75		-85		-90		-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CYC}	8.5	-	10	-	10	-	12	-	ns
Clock Access Time	t_{CD}	-	7.5	-	8.5	-	9.0	-	10	ns
Output Enable to Data Valid	t_{OE}	-	3.5	-	3.5	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t_{LZC}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Output Hold from Clock High	t_{OH}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	-	3.5	-	3.5	-	4.0	ns
Clock High to Output High-Z	t_{HZC}	-	4.0	-	5.0	-	5.0	-	6.0	ns
Clock High Pulse Width	t_{CH}	2.5	-	3.0	-	3.0	-	3.0	-	ns
Clock Low Pulse Width	t_{CL}	2.5	-	3.0	-	3.0	-	3.0	-	ns
Address Setup to Clock High	t_{AS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t_{SS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t_{DS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t_{WS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t_{ADVS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t_{CSS}	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t_{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

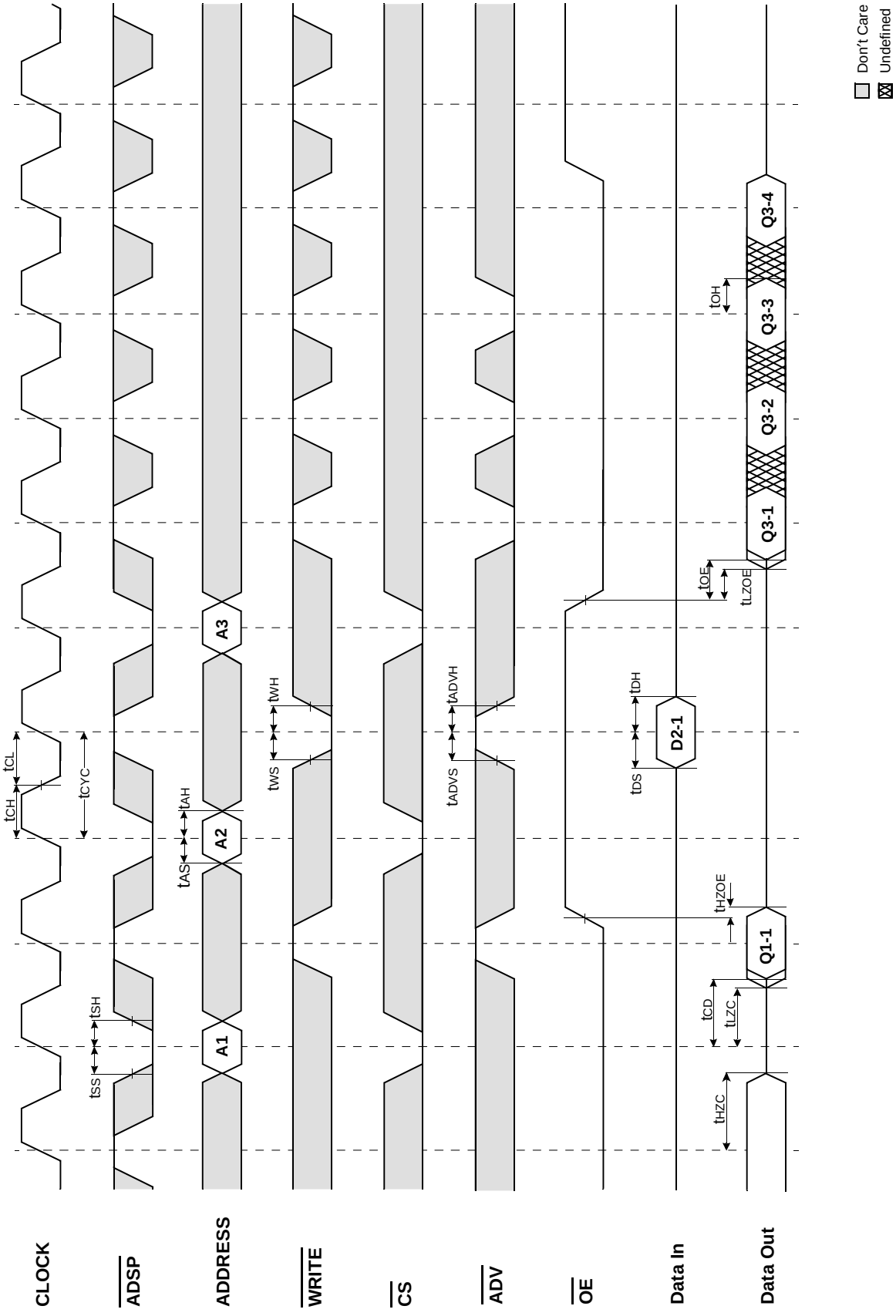
TIMING WAVEFORM OF READ CYCLE



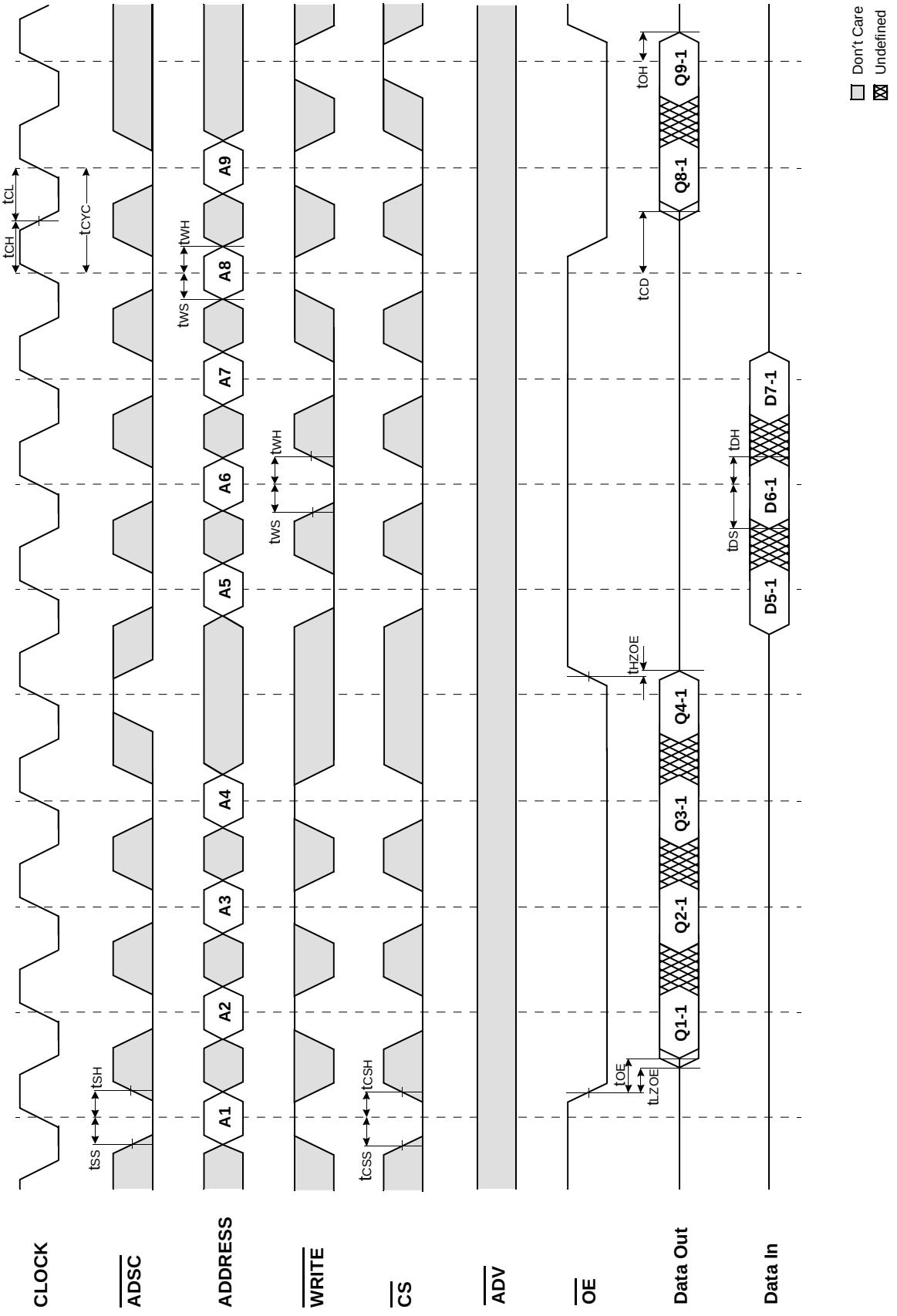
TIMING WAVEFORM OF WRTE CYCLE



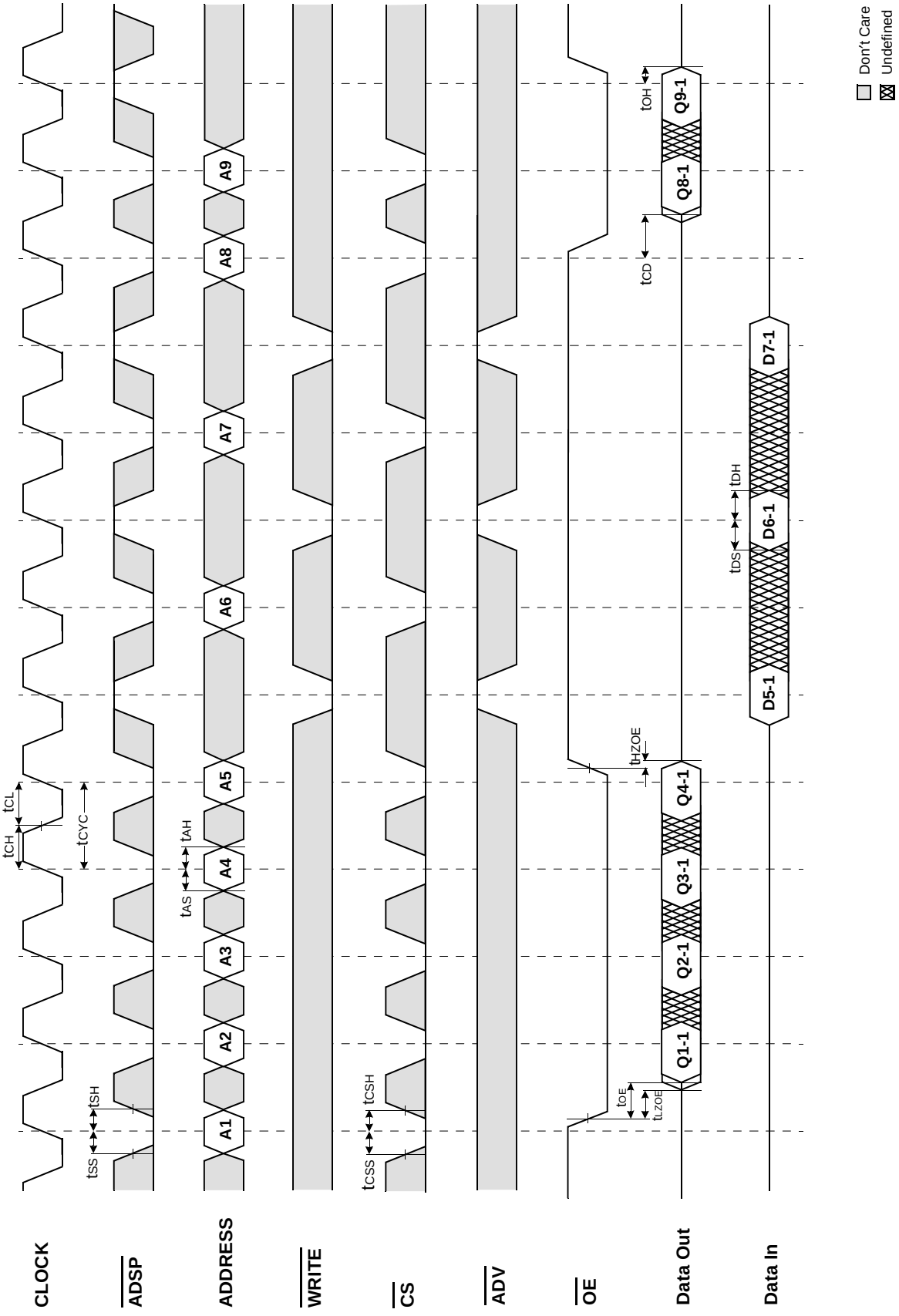
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



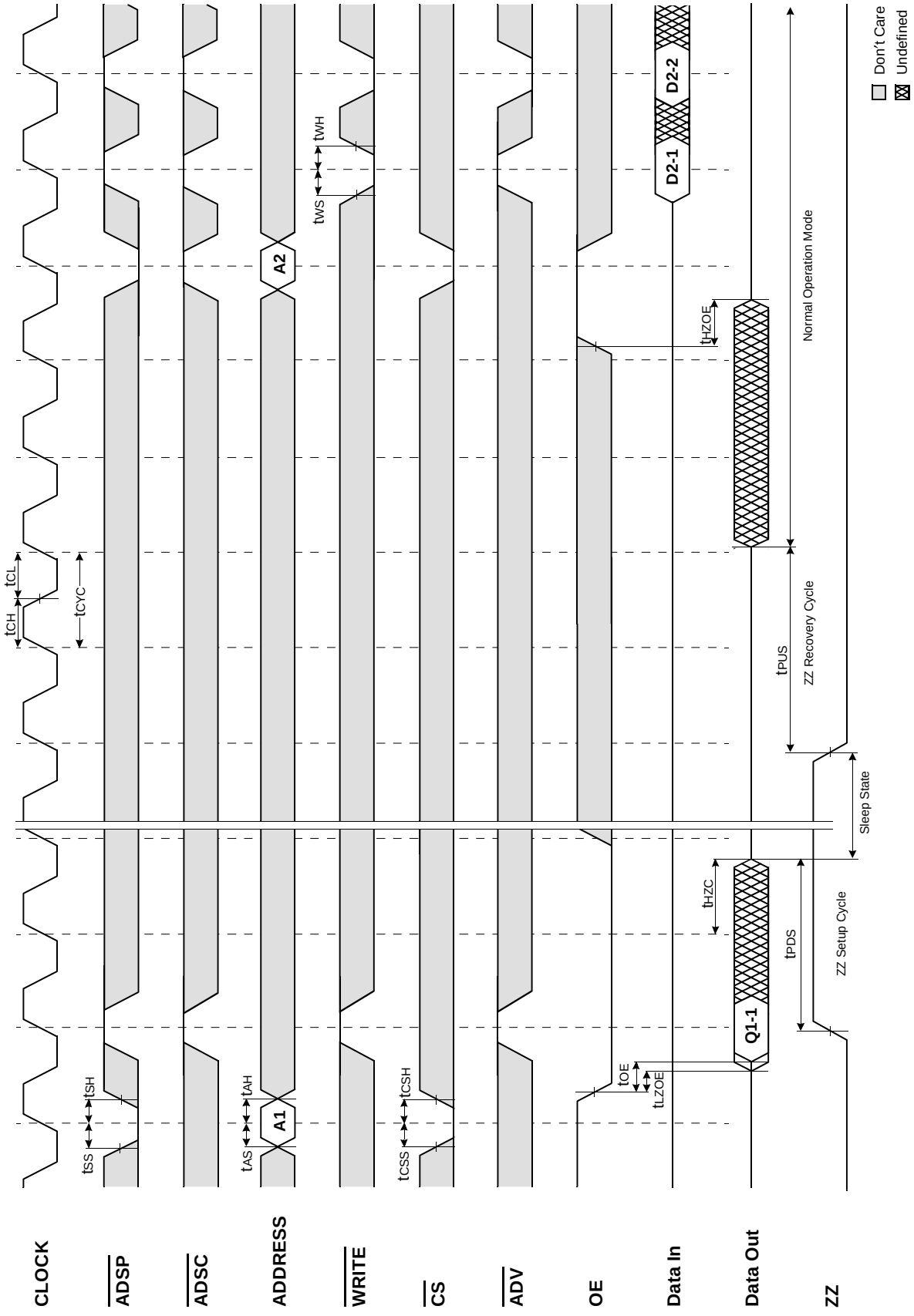
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



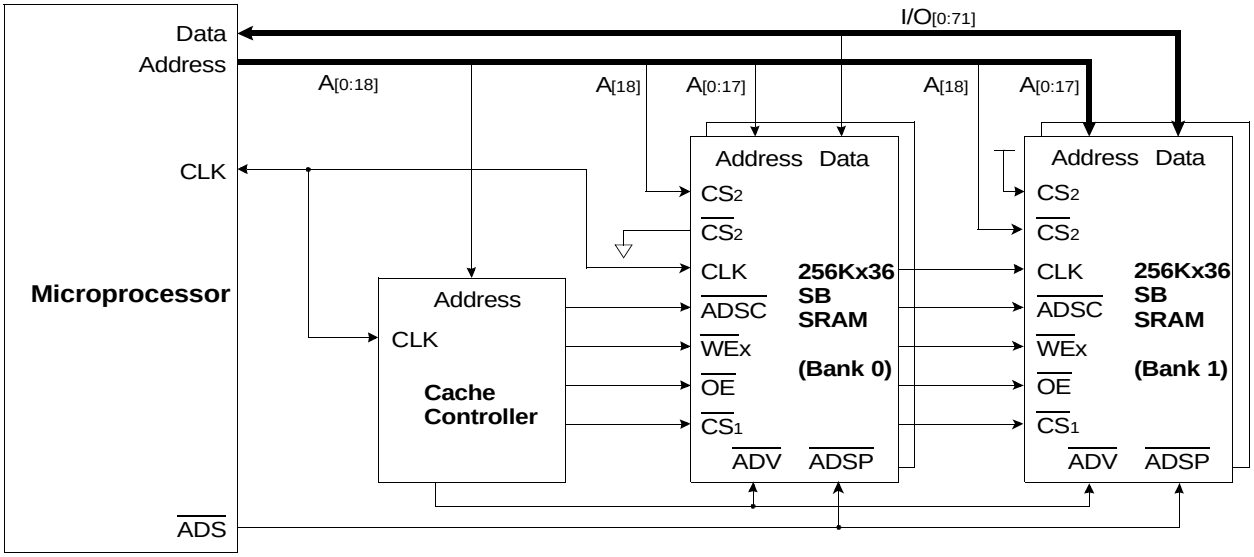
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

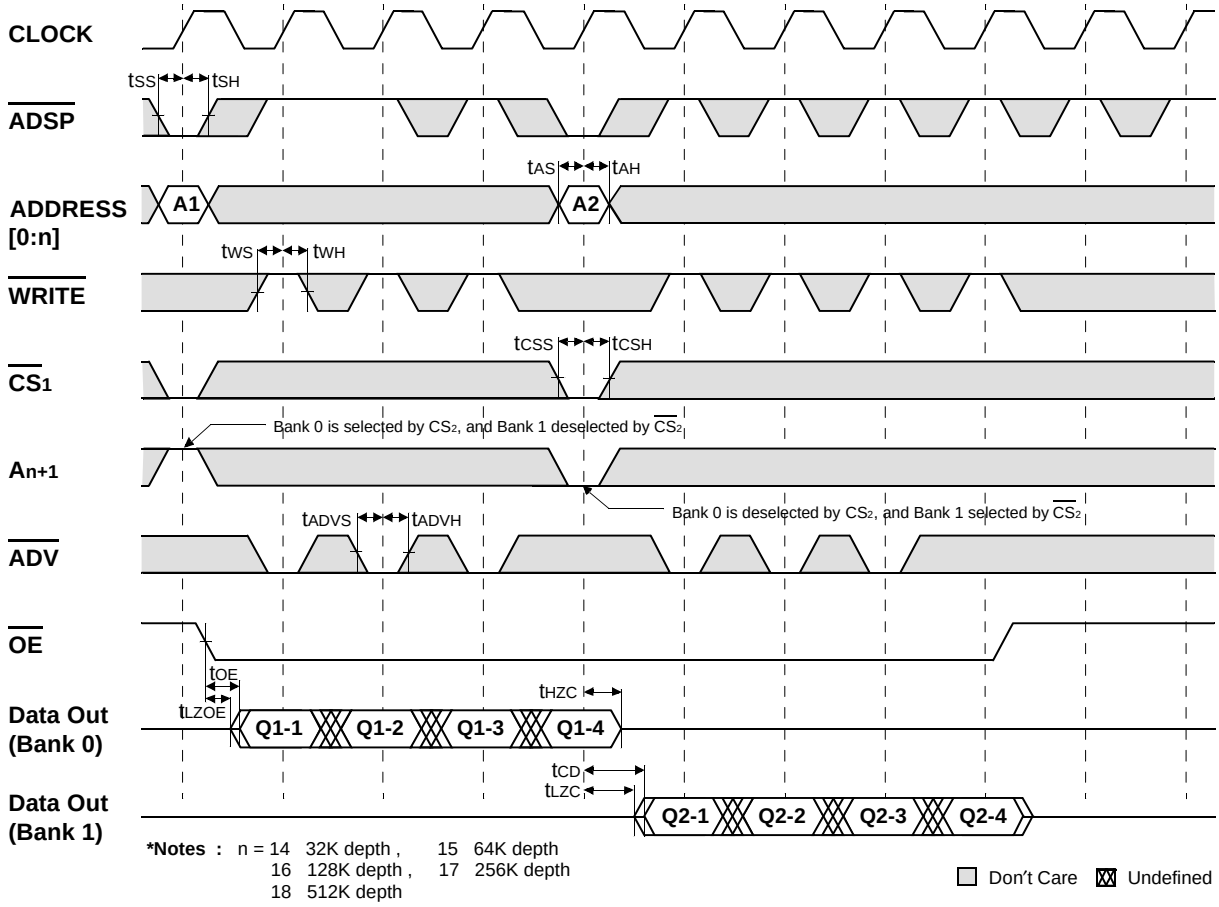
DEPTH EXPANSION

The Samsung 256Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)



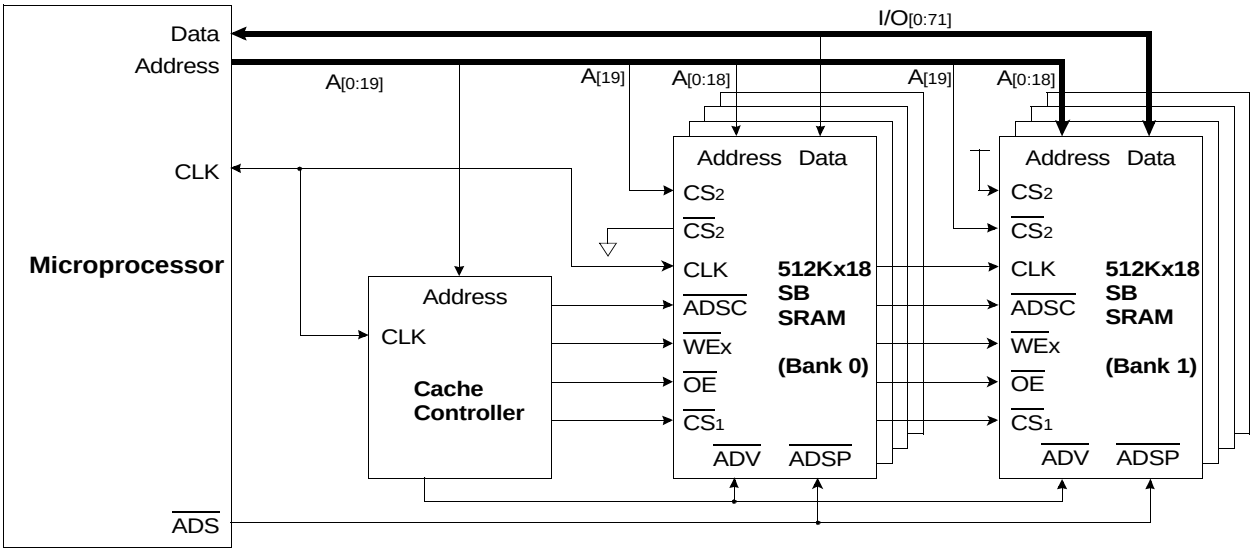
***Notes :** n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth

Don't Care Undefined

APPLICATION INFORMATION

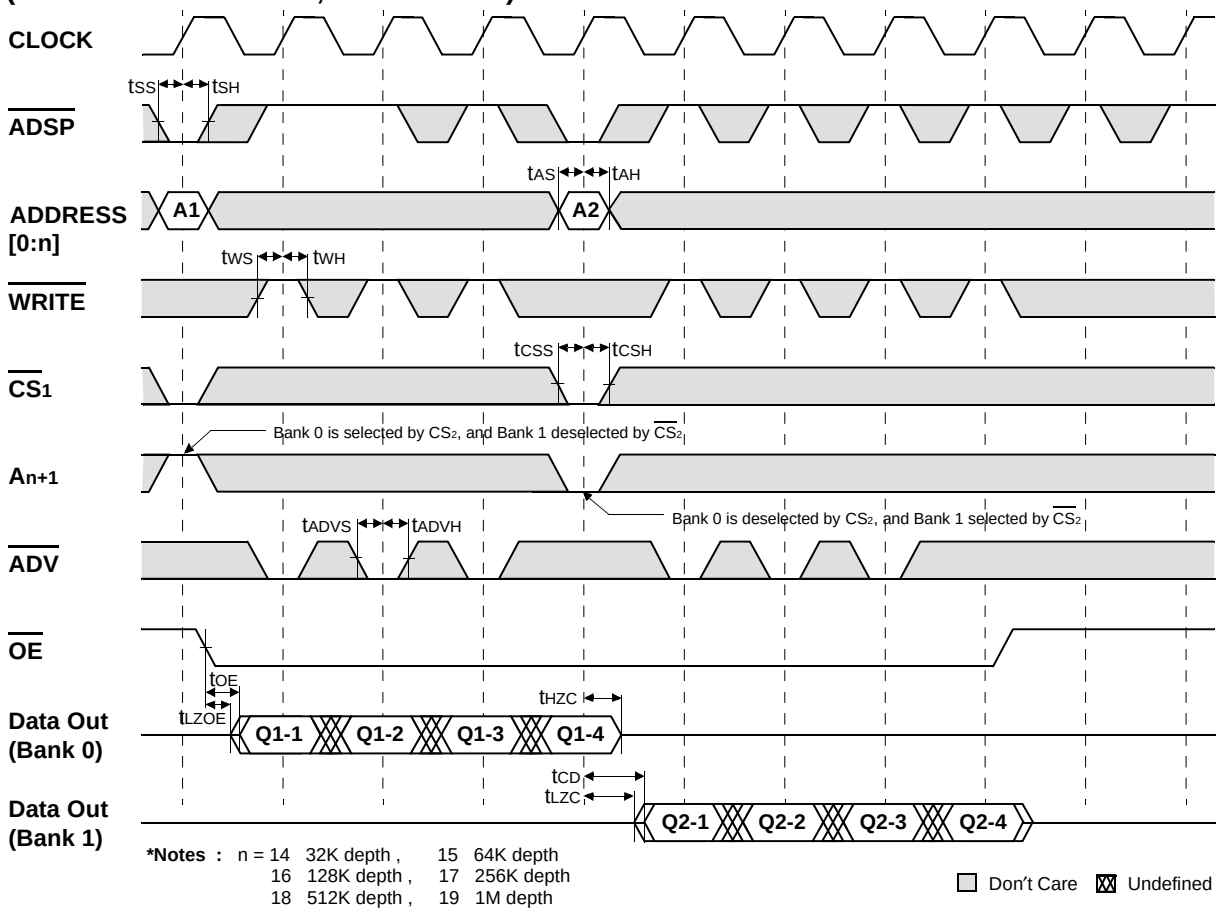
DEPTH EXPANSION

The Samsung 512Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

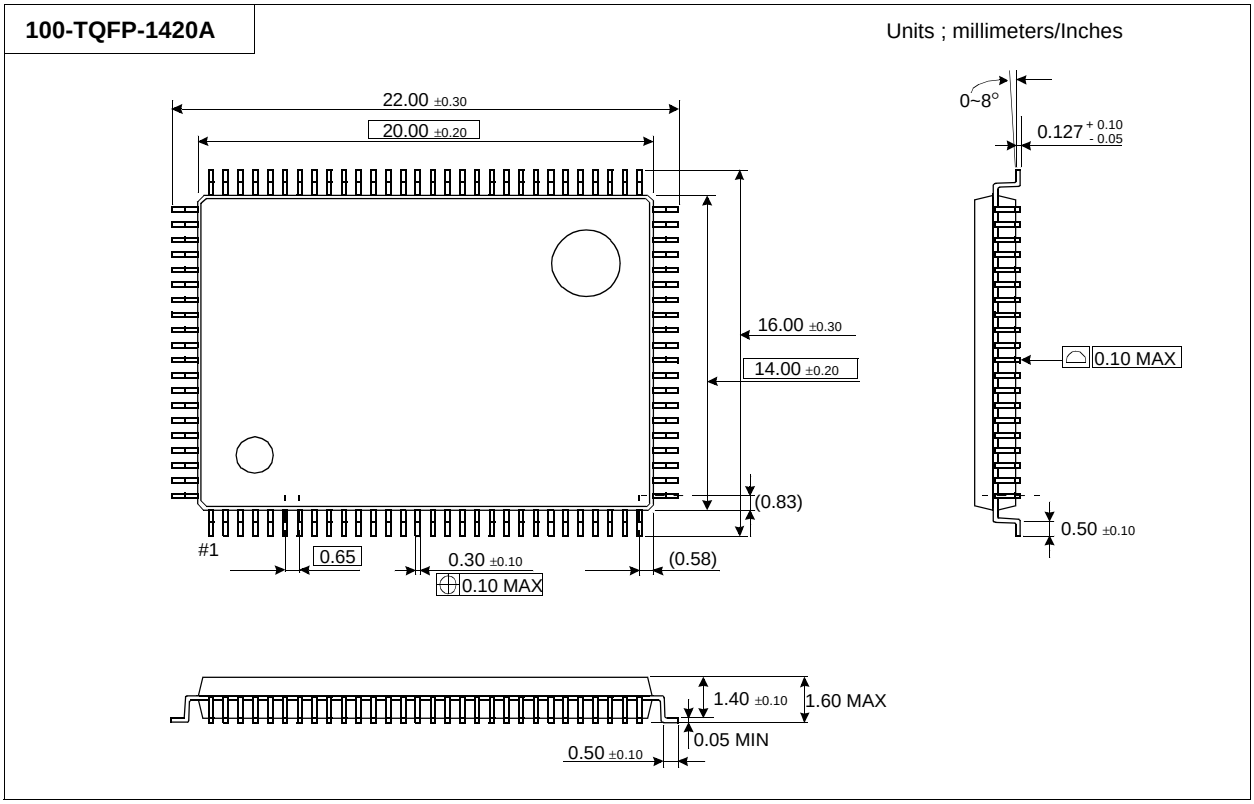
($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)



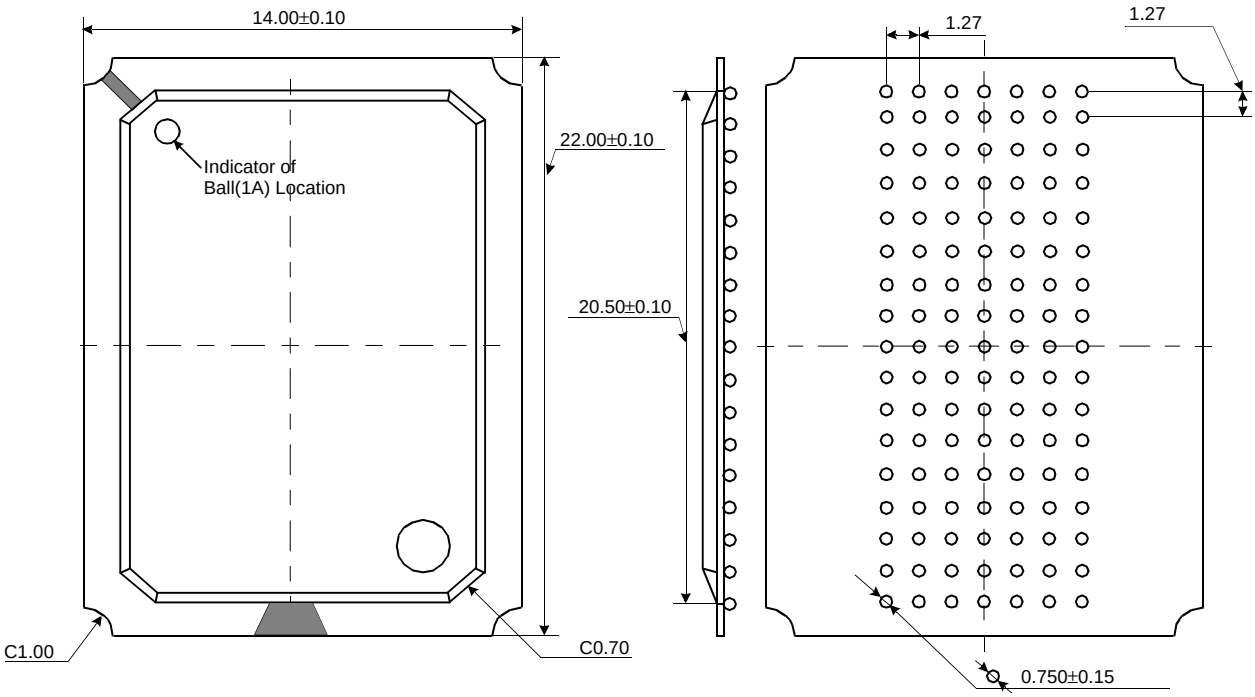
PACKAGE DIMENSIONS

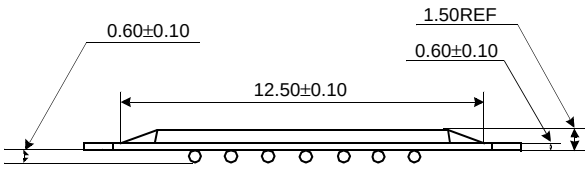
100-TQFP-1420A

Units ; millimeters/Inches



119BGA PACKAGE DIMENSIONS





NOTE :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.