

# K9K2G08U0A

# Preliminary FLASH MEMORY

## Document Title

256M x 8 Bit NAND Flash Memory

## Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	May. 31. 2004	Advance
0.1	1. Technical note is changed 2. Notes of AC timing characteristics are added 3. The description of Copy-back program is changed 4. TSOP package is deleted	Oct. 25. 2004	Preliminary
0.2	1. $\overline{CE}$ access time : 23ns->35ns (p.9)	Feb. 14. 2005	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions about device. If you have any questions, please contact the SAMSUNG branch office near your office.



**256M x 8 Bit NAND Flash Memory****PRODUCT LIST**

Part Number	Vcc Range	Organization	PKG Type
K9K2G08U0A-V,F	2.7 ~ 3.6V	X8	WSOP1

**FEATURES**

- Voltage Supply
  - 2.7 V ~3.6 V
- Organization
  - Memory Cell Array
    - (256M + 8,192K)bit x 8bit
  - Data Register
    - (2K + 64)bit x8bit
  - Cache Register
    - (2K + 64)bit x8bit
- Automatic Program and Erase
  - Page Program
    - (2K + 64)Byte
  - Block Erase
    - (128K + 4K)Byte
- Page Read Operation
  - Page Size
    - 2K-Byte
  - Random Read : 25µs(Max.)
  - Serial Access : 30ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Cache Program Operation for High Performance Program
- Intelligent Copy-Back Operation
- Unique ID for Copyright Protection
- Package :
  - K9K2G08U0A-VIB0
    - 48 - Pin WSOP I (12X17X0.7mm)
  - K9K2G08U0A-FIB0
    - 48 - Pin WSOP I (12X17X0.7mm)- Pb-free Package

**GENERAL DESCRIPTION**

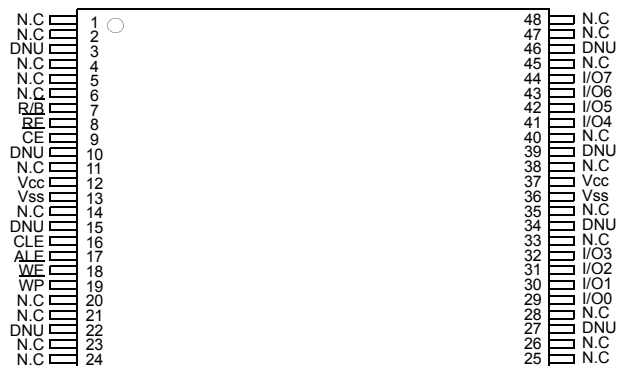
Offered in 256Mx8bit the K9K2G08U0A is 2G bit with spare 64M bit capacity. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 200µs on the 2112byte page and an erase operation can be performed in typical 2ms on a 128K-byte block. Data in the data page can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9K2G08U0A's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9K2G08U0A is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

# K9K2G08U0A

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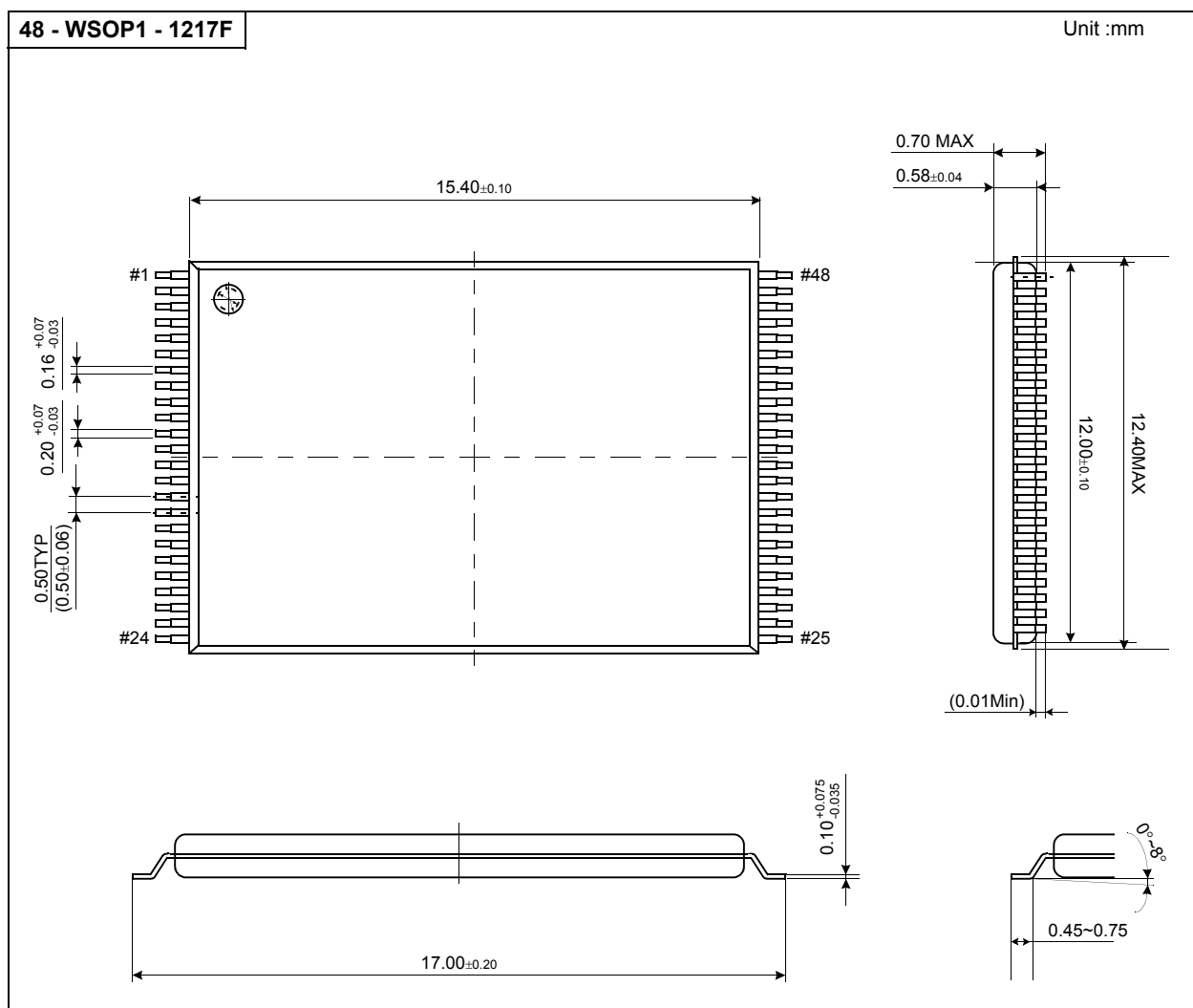
## PIN CONFIGURATION (WSOP1)

K9K2G08U0A-VIB0,FIB0



## PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)



## PIN DESCRIPTION

Pin Name	Pin Function
I/O <sub>0</sub> ~ I/O <sub>7</sub>	<b>DATA INPUTS/OUTPUTS</b> The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	<b>COMMAND LATCH ENABLE</b> The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	<b>ADDRESS LATCH ENABLE</b> The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	<b>CHIP ENABLE</b> The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ control during read operation, refer to 'Page read' section of Device operation .
$\overline{RE}$	<b>READ ENABLE</b> The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	<b>WRITE ENABLE</b> The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	<b>WRITE PROTECT</b> The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/ $\overline{B}$	<b>READY/BUSY OUTPUT</b> The R/ $\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	<b>POWER</b> Vcc is the power supply for device.
Vss	<b>GROUND</b>
N.C	<b>NO CONNECTION</b> Lead is not internally connected.

**NOTE:** Connect all Vcc and Vss pins of each device to common power supply outputs.  
Do not leave Vcc or Vss disconnected.

Figure 1-1. Functional Block Diagram

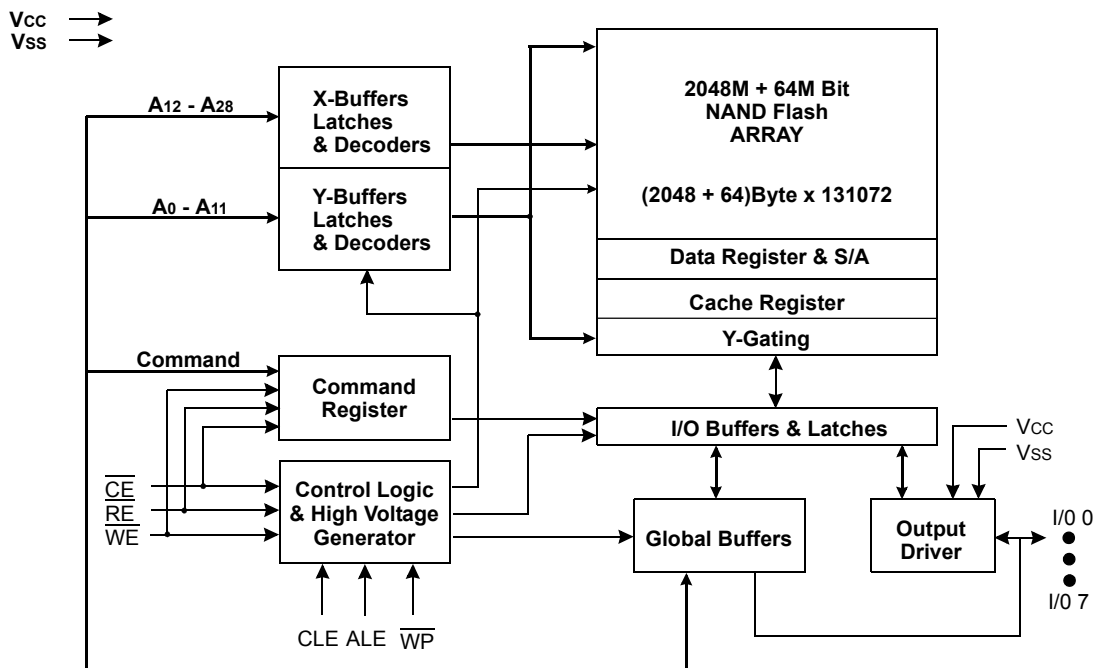
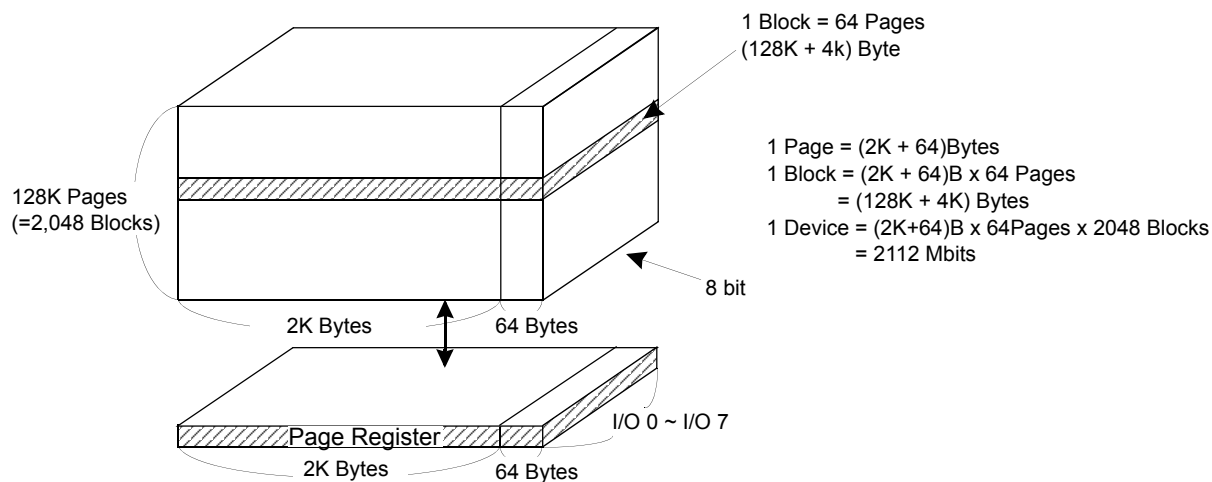


Figure 2-1. Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	Column Address
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	Row Address
5th Cycle	A28	*L	*L	*L	*L	*L	*L	*L	Row Address

NOTE : Column Address : Starting Address of the Register.

\* L must be set to "Low".

\* The device ignores any additional input of address cycles than required.

**Product Introduction**

The K9K2G08U0A is a 2112Mbit(2,214,592,512 bit) memory organized as 131,072 rows(pages) by 2112x8 columns. Spare 64 columns are located from column address of 2048~2111. A 2112-byte data register and a 2112-byte cache register are serially connected to each other. Those serially connected registers are connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structures. A NAND structure consists of 32 cells. Total 135168 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2048 separately erasable 128K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9K2G08U0A.

The K9K2G08U0A has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 256M byte physical space requires 29 addresses, thereby requiring five cycles for addressing: 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9K2G08U0A.

The device provides cache program in a block. It is possible to write data into the cache registers while data stored in data registers are being programmed into memory cells in cache program mode. The program performance may be dramatically improved by cache program when there are lots of pages of data to be programmed.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory. Since the time-consuming serial access and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

**Table 1. Command Sets**

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Cache Program <sup>2</sup>	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input <sup>1</sup>	85h	-	
Random Data Output <sup>1</sup>	05h	E0h	
Read Status	70h		O

**NOTE** : 1. Random Data Input/Output can be executed in a page.

**Caution** : Any undefined command inputs are prohibited except for above command set of Table 1.

**ABSOLUTE MAXIMUM RATINGS**

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to Vss		V <sub>IN/OUT</sub>	-0.6 to + 4.6	V
		V <sub>CC</sub>	-0.6 to + 4.6	
Temperature Under Bias	K9K2G08U0A-VCB0	T <sub>BIAS</sub>	-10 to +125	°C
	K9K2G08U0A-VIB0		-40 to +125	
Storage Temperature	K9K2G08U0A-VCB0	T <sub>STG</sub>	-65 to +150	°C
	K9K2G08U0A-VIB0			
Short Circuit Current		I <sub>OS</sub>	5	mA

**NOTE :**

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V<sub>CC</sub>+0.3V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

(Voltage reference to GND, :T<sub>A</sub>=0 to 70°C, K9K2G08U0A-VIB0:T<sub>A</sub>=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V <sub>CC</sub>	2.7	3.3	3.6	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V

**DC AND OPERATING CHARACTERISTICS**(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	I <sub>CC1</sub>	t <sub>RC</sub> =30ns, $\overline{CE}=V_{IL}$ I <sub>OUT</sub> =0mA	-	10	30	mA
	Program	I <sub>CC2</sub>	-	-	10	30	
	Erase	I <sub>CC3</sub>	-	-	10	30	
Stand-by Current(TTL)		I <sub>SB1</sub>	$\overline{CE}=V_{IH}$ , $\overline{WP}=0V/V_{CC}$	-	-	1	
Stand-by Current(CMOS)		I <sub>SB2</sub>	$\overline{CE}=V_{CC}-0.2$ , $\overline{WP}=0V/V_{CC}$	-	20	100	μA
Input Leakage Current		I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub> (max)	-	-	±10	
Output Leakage Current		I <sub>LO</sub>	V <sub>OUT</sub> =0 to V <sub>CC</sub> (max)	-	-	±10	
Input High Voltage		V <sub>IH</sub>	-	0.8xV <sub>CC</sub>	-	V <sub>CC</sub> +0.3	
Input Low Voltage, All inputs		V <sub>IL</sub>	-	-0.3	-	0.2xV <sub>CC</sub>	V
Output High Voltage Level		V <sub>OH</sub>	I <sub>OH</sub> =-400μA	2.4	-	-	
Output Low Voltage Level		V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	
Output Low Current(R/B)		I <sub>OL</sub> (R/B)	V <sub>OL</sub> =0.4V	8	10	-	

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## VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	NvB	2008	-	2048	Blocks

### NOTE :

- The K9K2G08U0A may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
- The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block and does not require Error Correction up to 1K Program/ Erase cycles..

## AC TEST CONDITION

(K9K2G08U0A-VCB0 :TA=0 to 70°C, K9K2G08U0A-VIB0:TA=-40 to 85°C

K9K2G08U0A : Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9K2G08U0A
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load (Vcc:3.3V +/-10%)	1 TTL GATE and CL=50pF

## CAPACITANCE(TA=25°C, VCC=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>IL</sub> =0V	-	20	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	20	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

## MODE SELECTION

CLE	ALE	CE	WE	RE	WP	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(5clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(5clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X <sup>(1)</sup>	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc <sup>(2)</sup>	Stand-by	

NOTE : 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.

2. WP should be biased to CMOS high or CMOS low for standby.

## Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t <sub>PROG</sub> <sup>1</sup>	-	200	700	μs
Dummy Busy Time for Cache Program	t <sub>CBSY</sub> <sup>2</sup>	-	3	700	μs
Number of Partial Program Cycles in the Same Page	Main Array	-	-	4	cycles
	Spare Array	-	-	4	cycles
Block Erase Time	t <sub>BERS</sub>	-	2	3	ms

NOTE : 1. Typical program time is defined as the time within which more than 50% of whole pages are programmed at Vcc of 3.3V and 25°C

2. Max. time of t<sub>CBSY</sub> depends on timing between internal program completion and data in



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## AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min		Max		Unit
		K9K2G08U0A*	K9K2G08U0A	K9K2G08U0A*	K9K2G08U0A	
CLE setup Time	tCLS <sup>1</sup>	25	15	-	-	ns
CLE Hold Time	tCLH	10	5	-	-	ns
$\overline{\text{CE}}$ setup Time	tCS <sup>1</sup>	35	20	-	-	ns
$\overline{\text{CE}}$ Hold Time	tCH	10	5	-	-	ns
$\overline{\text{WE}}$ Pulse Width	tWP	25	15	-	-	ns
ALE setup Time	tALS <sup>1</sup>	25	15	-	-	ns
ALE Hold Time	tALH	10	5	-	-	ns
Data setup Time	tDS <sup>1</sup>	20	15	-	-	ns
Data Hold Time	tDH	10	5	-	-	ns
Write Cycle Time	tWC	45	30	-	-	ns
$\overline{\text{WE}}$ High Hold Time	tWH	15	10	-	-	ns
ALE to Data Loading Time	tADL <sup>2</sup>	100 <sup>2</sup>	100 <sup>2</sup>	-	-	ns

NOTE : 1. The transition of the corresponding control pins must occur only once while  $\overline{\text{WE}}$  is held low.

2. tADL is the time from the  $\overline{\text{WE}}$  rising edge of final address cycle to the  $\overline{\text{WE}}$  rising edge of first data cycle.

3. For cache program operation, the whole AC Characteristics must be same as that of K9K2G08U0A\*.

## AC Characteristics for Operation

Parameter	Symbol	Min		Max		Unit
		K9K2G08U0A*	K9K2G08U0A	K9K2G08U0A*	K9K2G08U0A	
Data Transfer from Cell to Register	tR	-	-	25	25	μs
ALE to $\overline{\text{RE}}$ Delay	tAR	10	10	-	-	ns
CLE to $\overline{\text{RE}}$ Delay	tCLR	10	10	-	-	ns
Ready to $\overline{\text{RE}}$ Low	tRR	20	20	-	-	ns
RE Pulse Width	tRP	25	15	-	-	ns
WE High to Busy	tWB	-	-	100	100	ns
Read Cycle Time	tRC	50	30	-	-	ns
$\overline{\text{RE}}$ Access Time	tREA	-	-	30	18	ns
$\overline{\text{CE}}$ Access Time	tCEA	-	-	45	35	ns
$\overline{\text{RE}}$ High to Output Hi-Z	tRHZ	-	-	30	30	ns
$\overline{\text{CE}}$ High to Output Hi-Z	tCHZ	-	-	20	20	ns
$\overline{\text{RE}}$ or $\overline{\text{CE}}$ High to Output hold	tOH	15	15	-	-	ns
$\overline{\text{RE}}$ High Hold Time	tREH	15	10	-	-	ns
Output Hi-Z to $\overline{\text{RE}}$ Low	tIR	0	0	-	-	ns
$\overline{\text{RE}}$ High to $\overline{\text{WE}}$ Low	tRHW	100	100	-	-	ns
$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low	tWHR	60	60	-	-	ns
Device Resetting Time (Read/Program/Erase)	tRST	-	-	5/10/500 <sup>1</sup>	5/10/500 <sup>1</sup>	μs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

2. For cache program operation, the whole AC Characteristics must be same as that of K9K2G08U0A\*.

**NAND Flash Technical Notes**

**Initial Invalid Block(s)**

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is so called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction up to 1K Program/Erase cycles.

**Identifying Initial Invalid Block(s)**

All device locations are erased except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

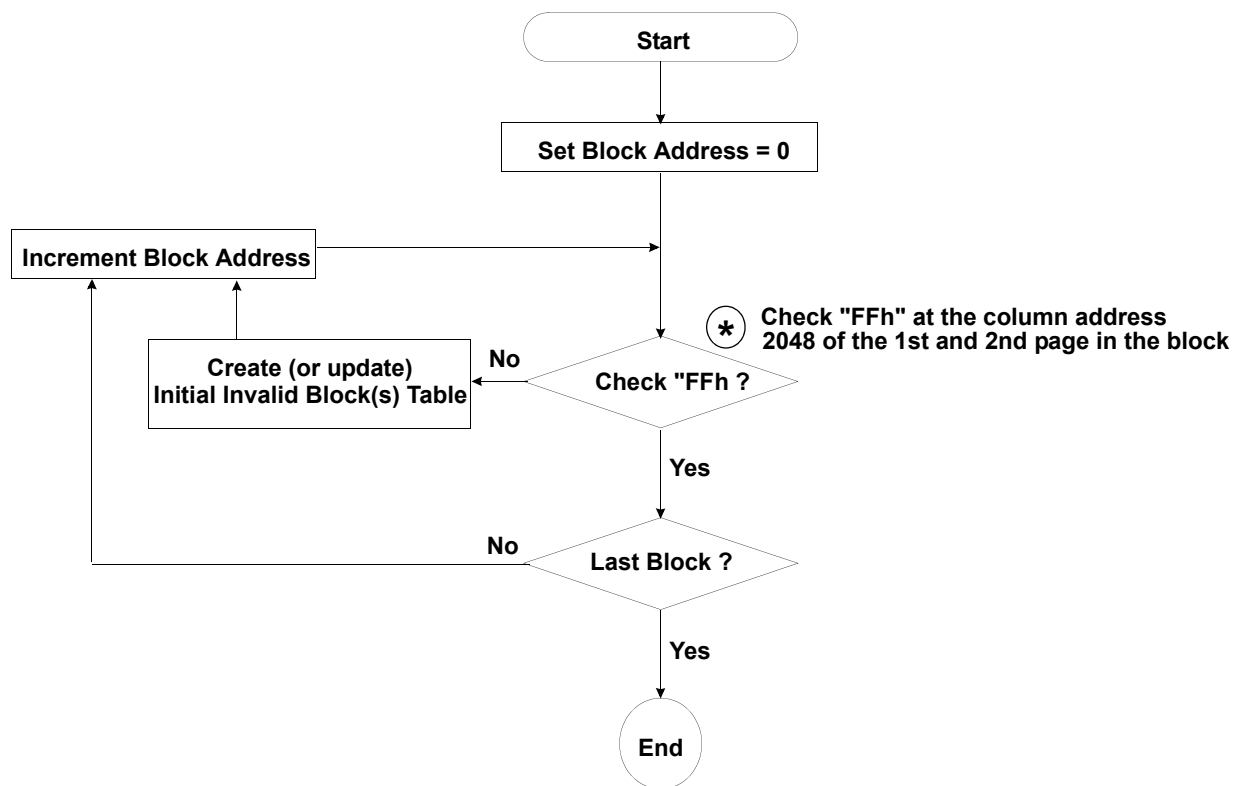


Figure 3. Flow chart to create initial invalid block table.

**NAND Flash Technical Notes (Continued)**

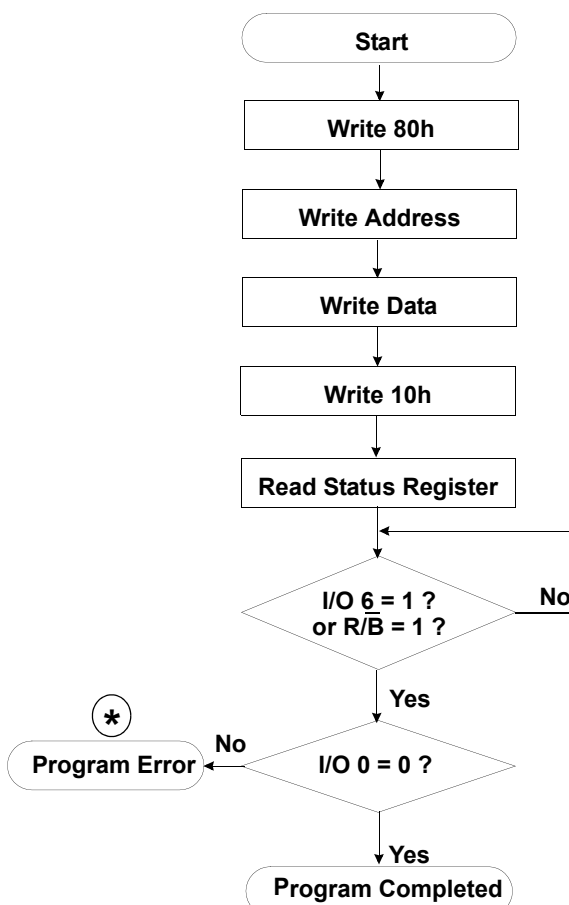
**Error in write or read operation**

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure rate in the qualification report does not include those reclaimed blocks.

	Failure Mode	Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

**ECC** : Error Correcting Code --> Hamming Code etc.  
Example) 1bit correction & 2bit detection

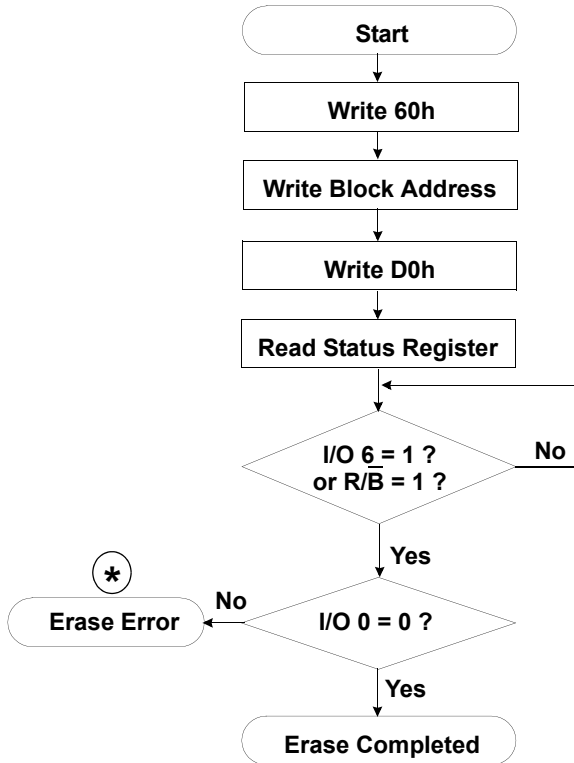
**Program Flow Chart**



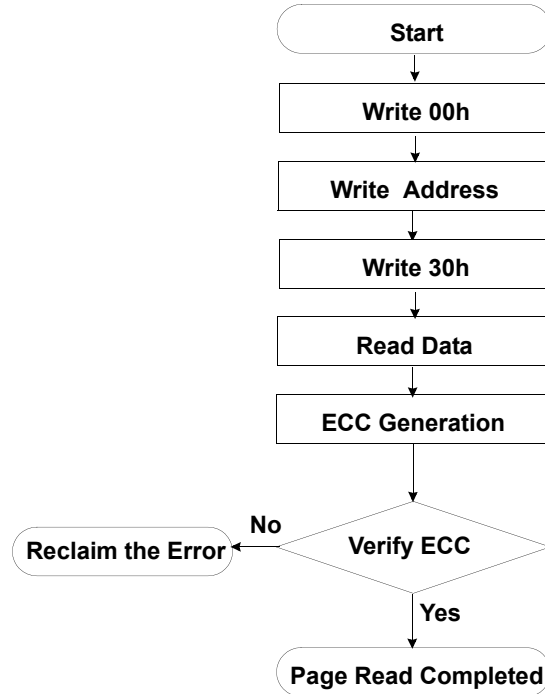
**\*** : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes (Continued)

Erase Flow Chart

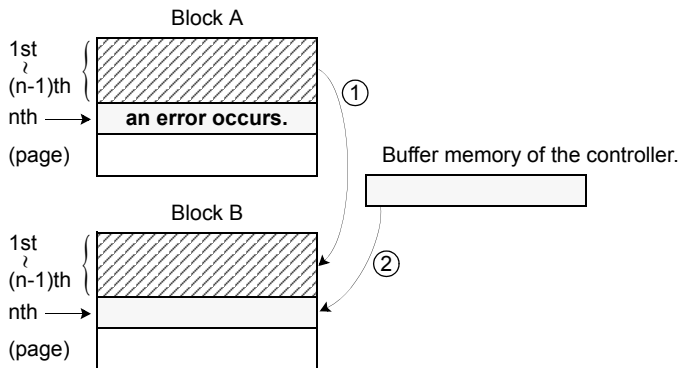


Read Flow Chart



\* : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement

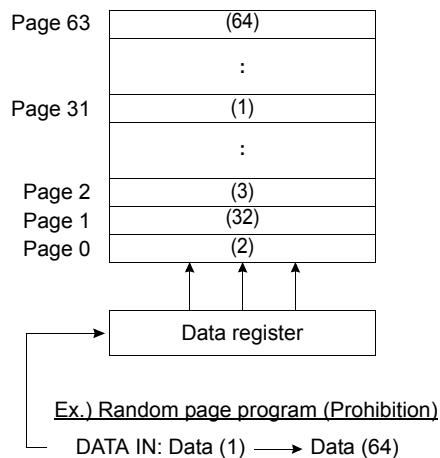
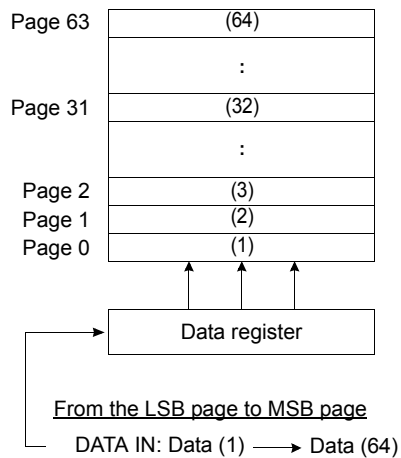


- \* Step1  
When an error happens in the nth page of the Block 'A' during erase or program operation.
- \* Step2  
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
- \* Step3  
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
- \* Step4  
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

**NAND Flash Technical Notes** (Continued)

**Addressing for program operation**

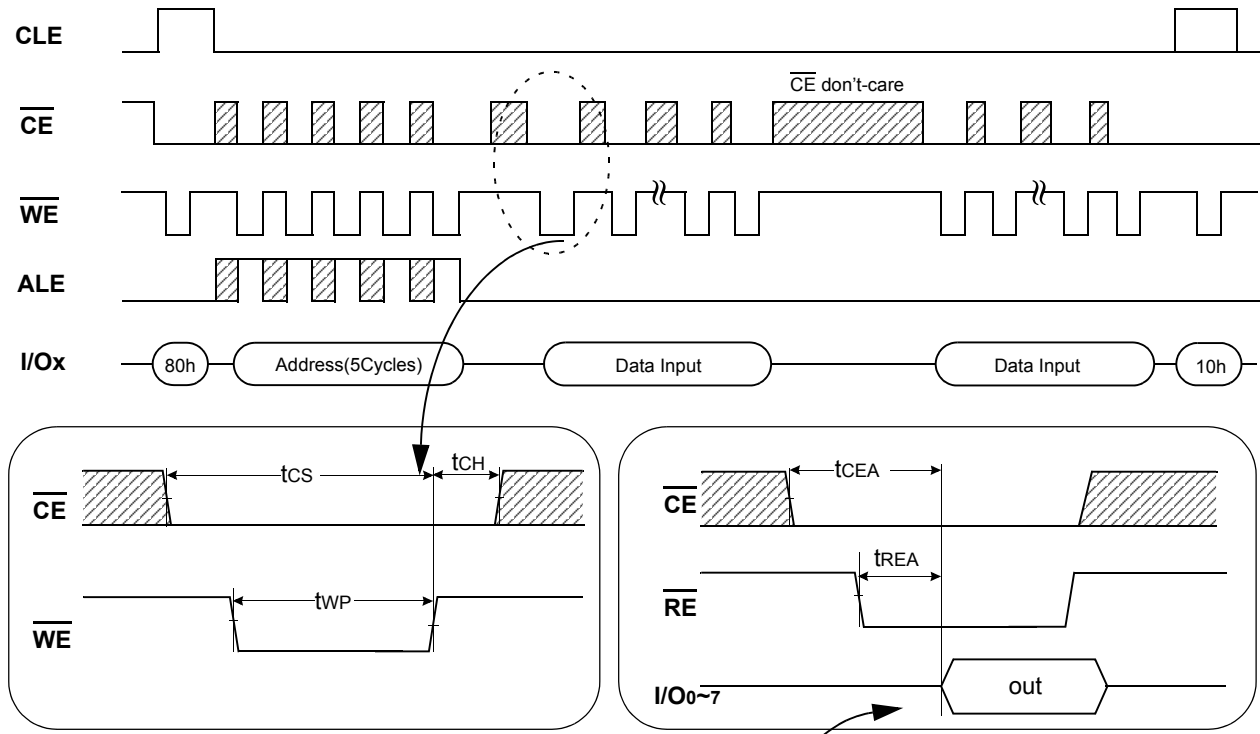
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited.



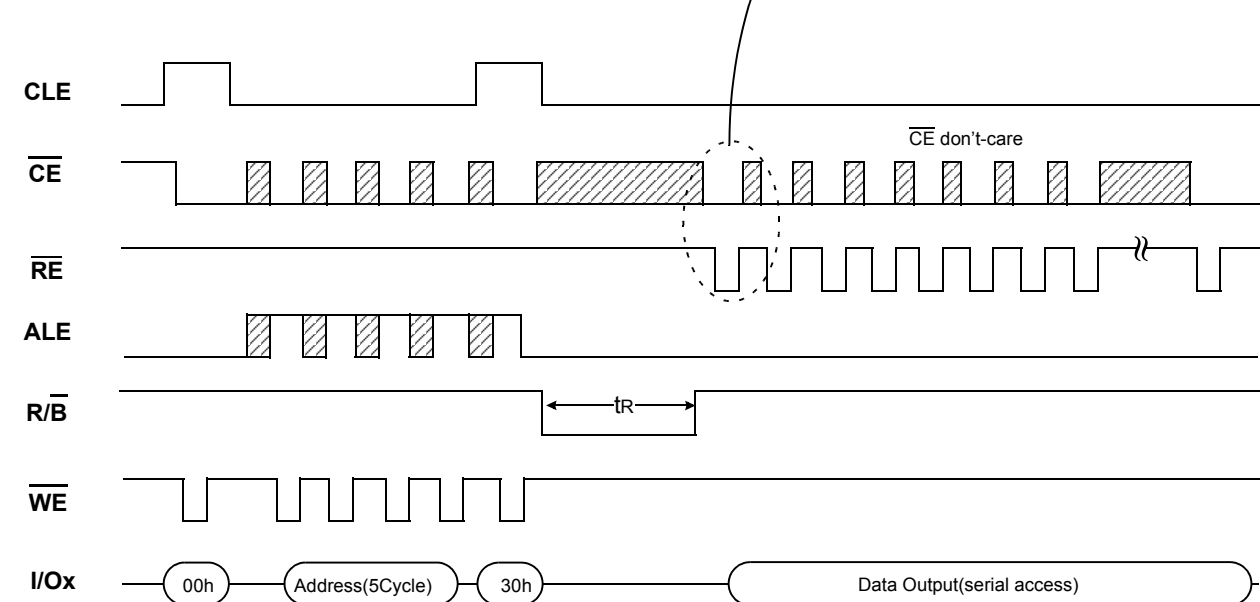
**System Interface Using  $\overline{\text{CE}}$  don't-care.**

For an easier system interface,  $\overline{\text{CE}}$  may be inactive during the data-loading or serial access as shown below. The internal 2112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating  $\overline{\text{CE}}$  during the data-loading and serial access would provide significant savings in power consumption.

**Figure 4. Program Operation with  $\overline{\text{CE}}$  don't-care.**



**Figure 5. Read Operation with  $\overline{\text{CE}}$  don't-care.**



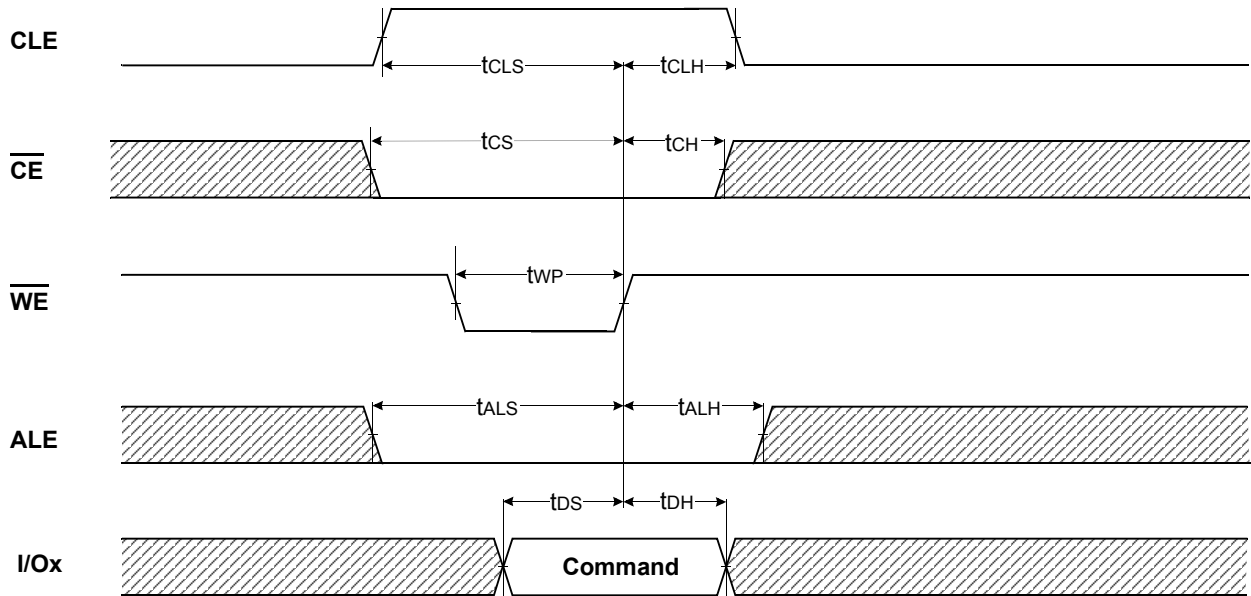
# K9K2G08U0A

# Preliminary FLASH MEMORY

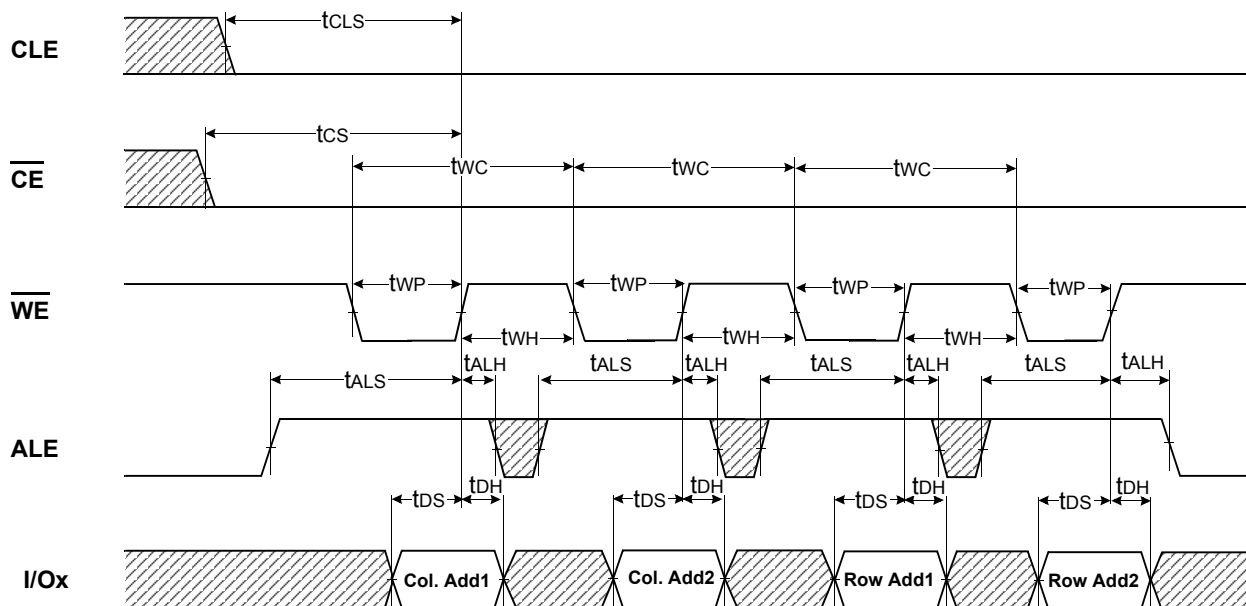
NOTE

Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
K9K2G08U0A	I/O 0 ~ I/O 7	~2112byte	A0~A7	A8~A11	A12~A19	A20~A27	A28

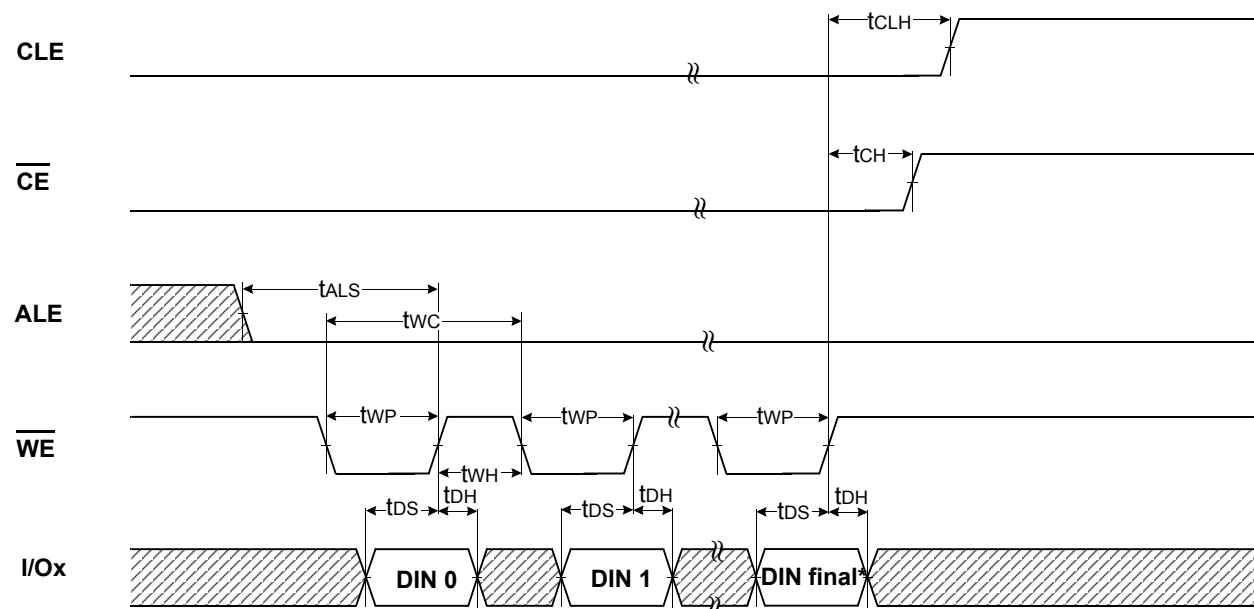
## Command Latch Cycle



## Address Latch Cycle

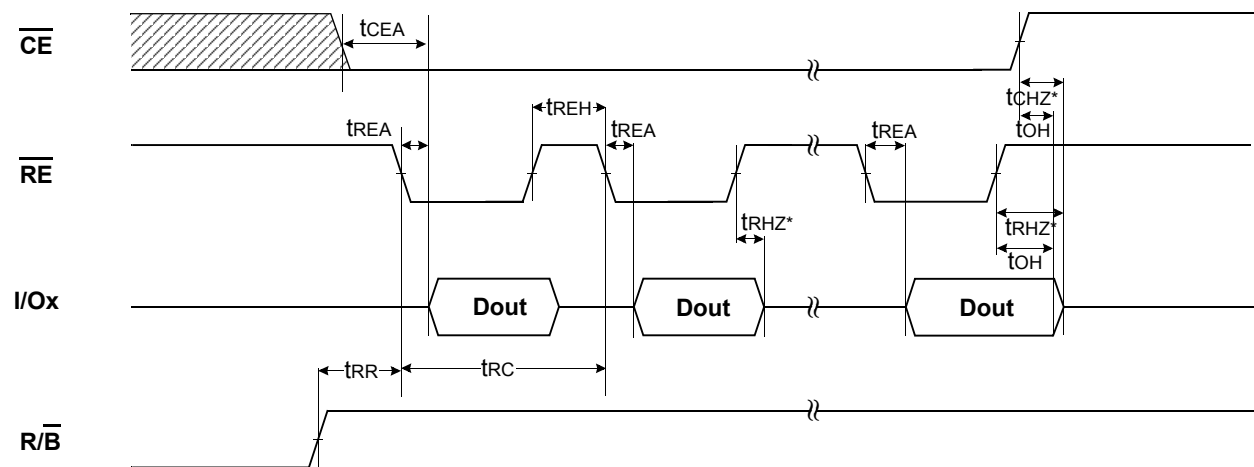


Input Data Latch Cycle



NOTES : DIN final means 2112

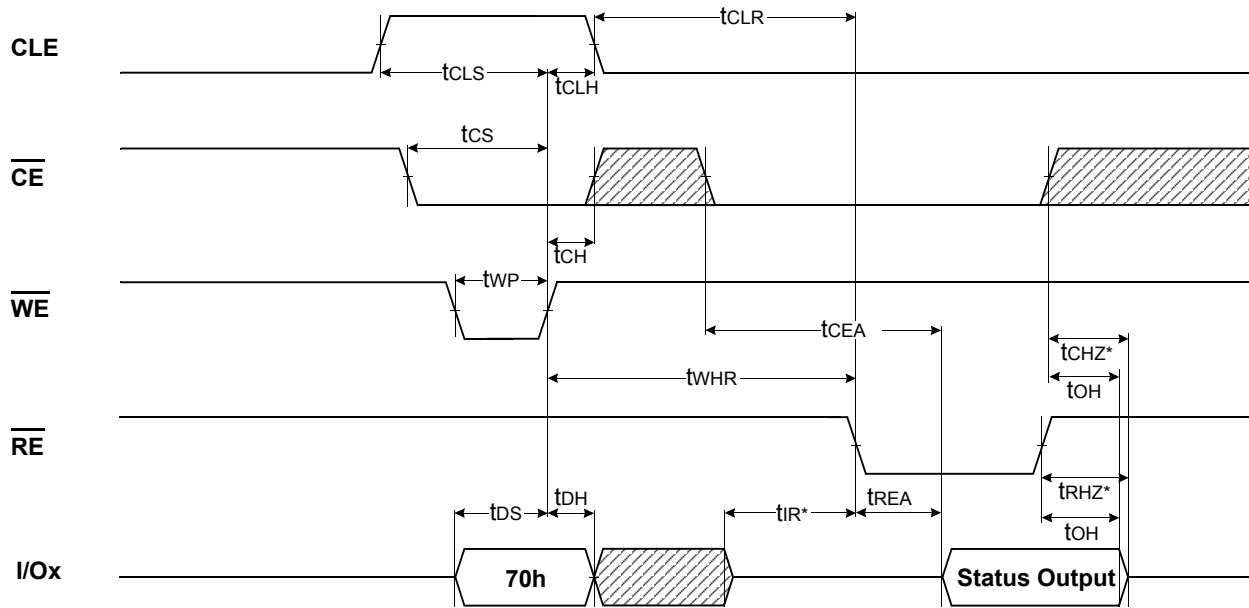
Serial Access Cycle after Read (CLE=L, WE=H, ALE=L)



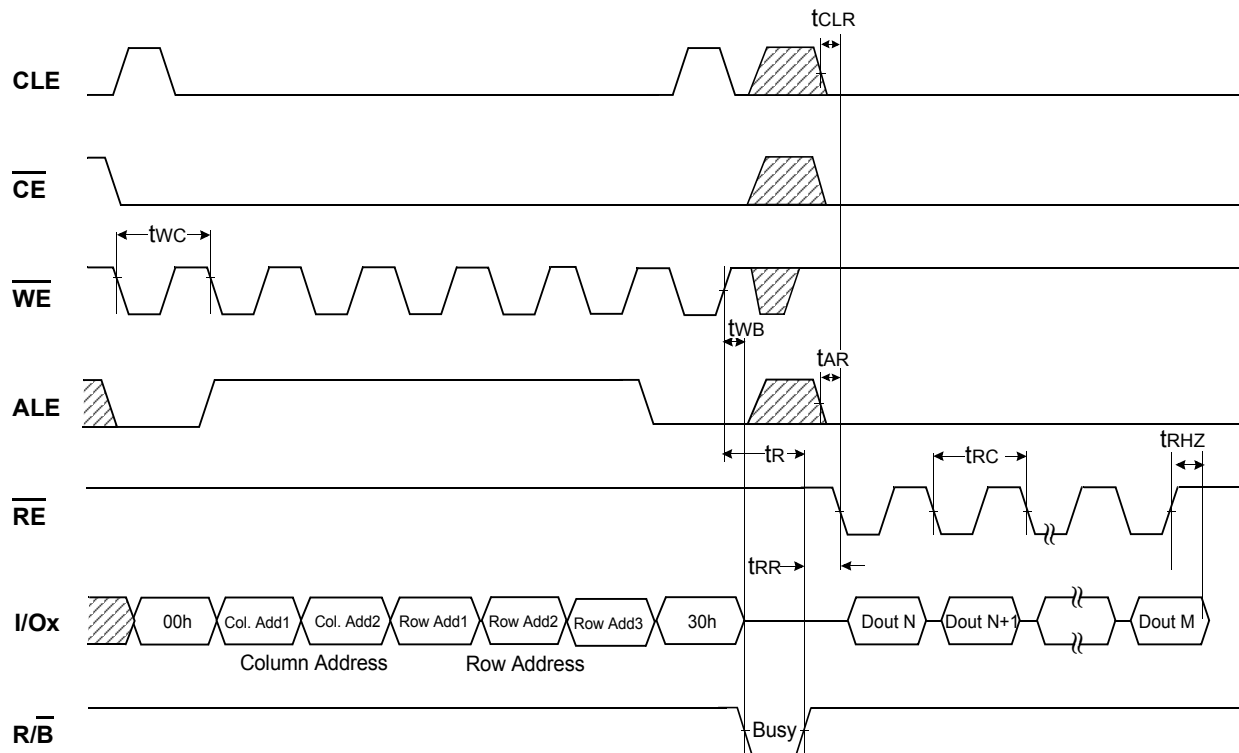
NOTES : Transition is measured  $\pm 200\text{mV}$  from steady state voltage with load.  
This parameter is sampled and not 100% tested.



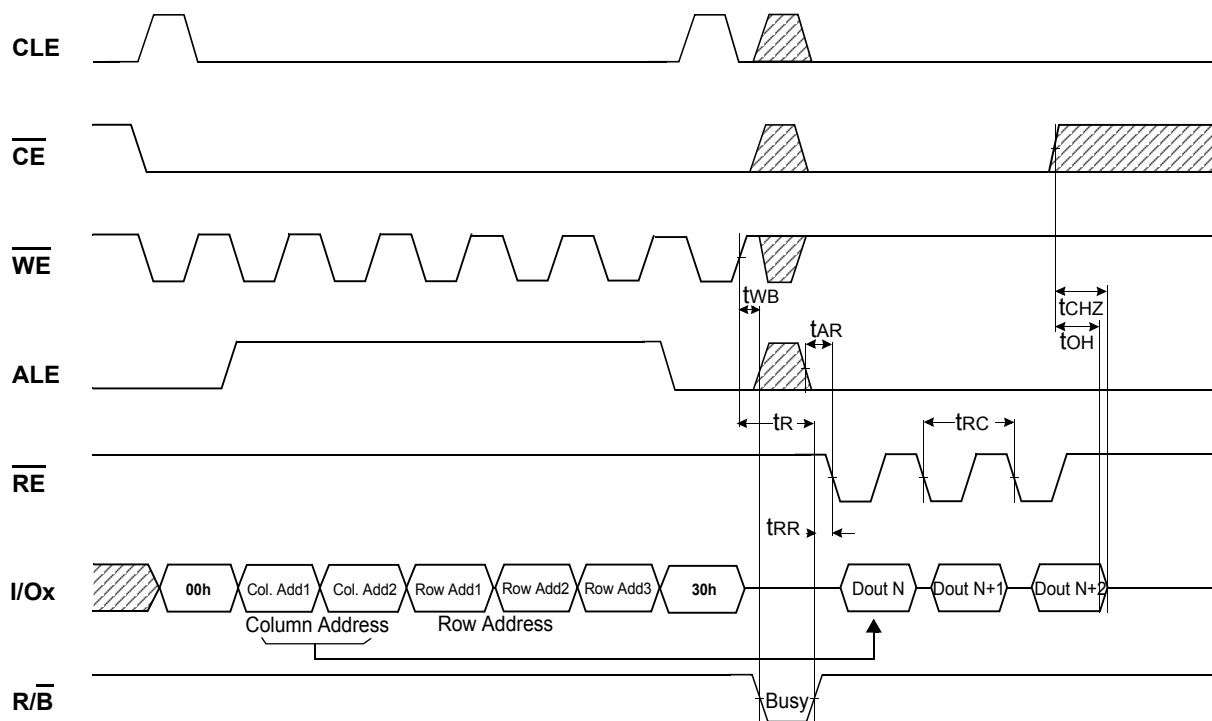
Status Read Cycle



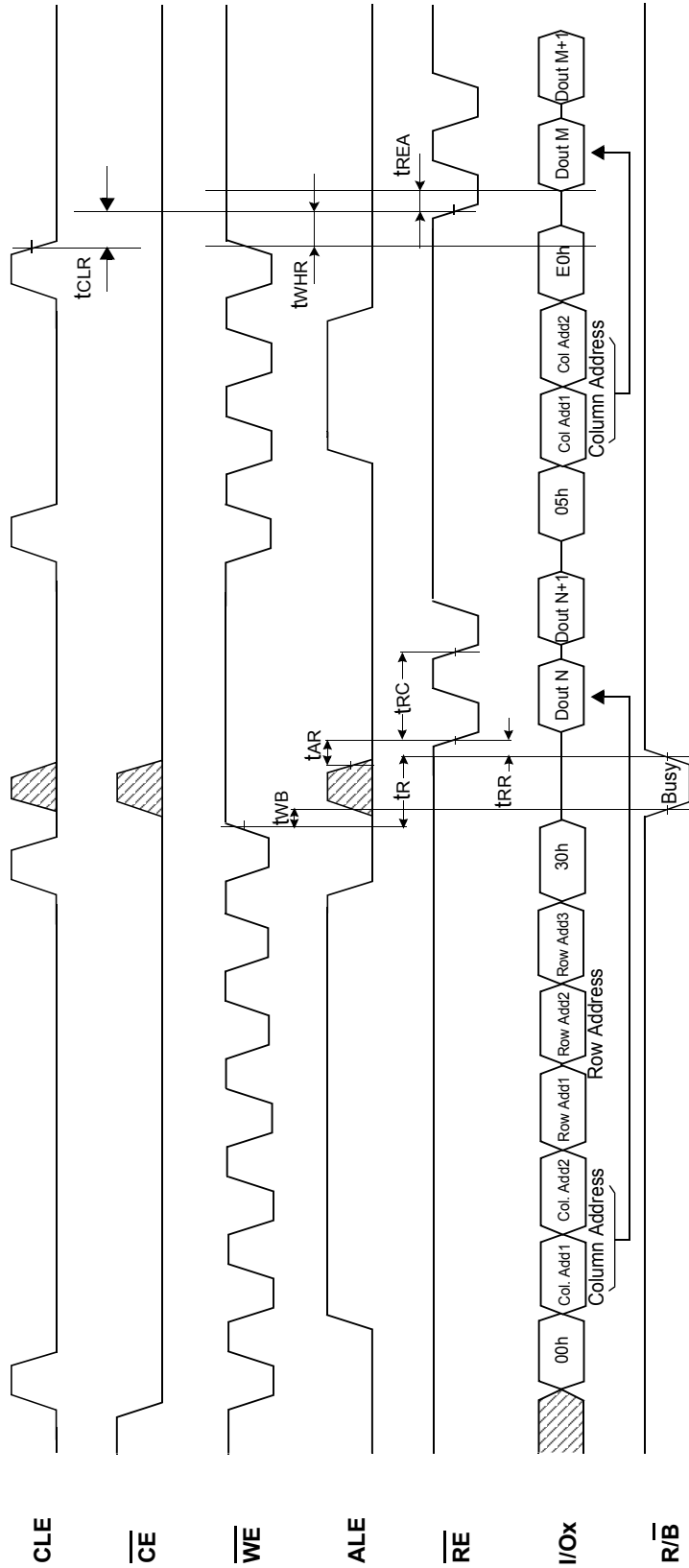
Read Operation



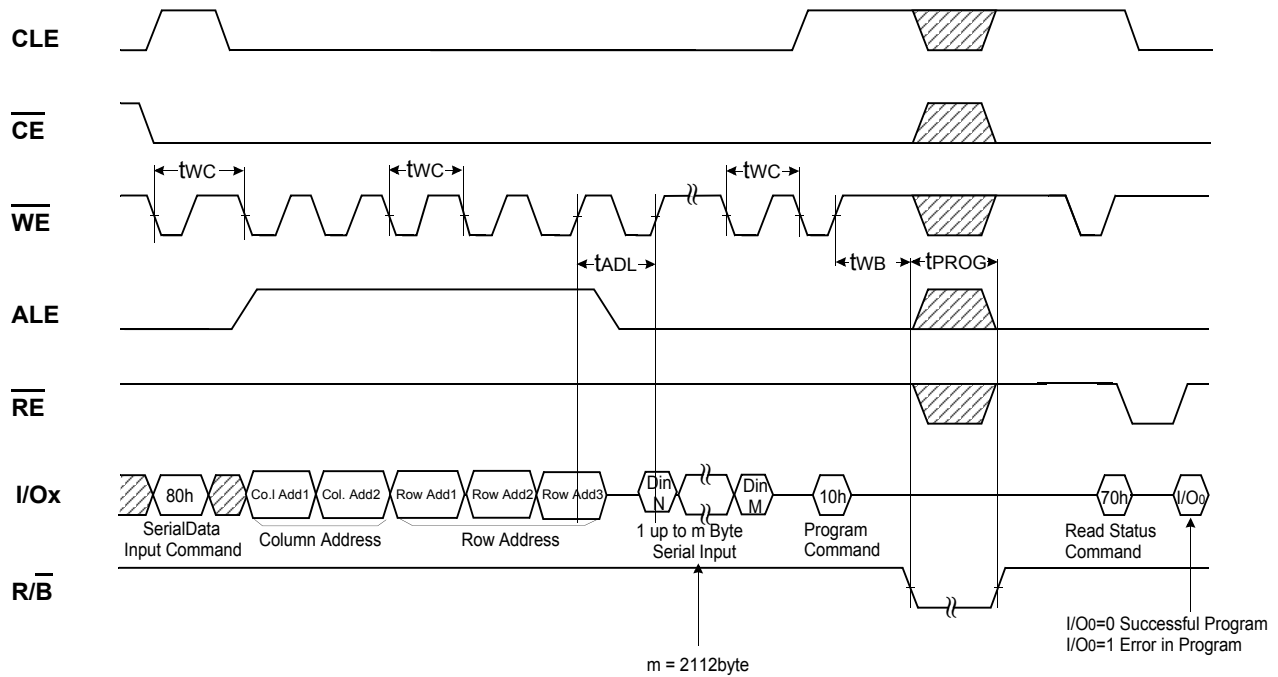
Read Operation (Intercepted by  $\overline{CE}$ )



Random Data Output in a Page

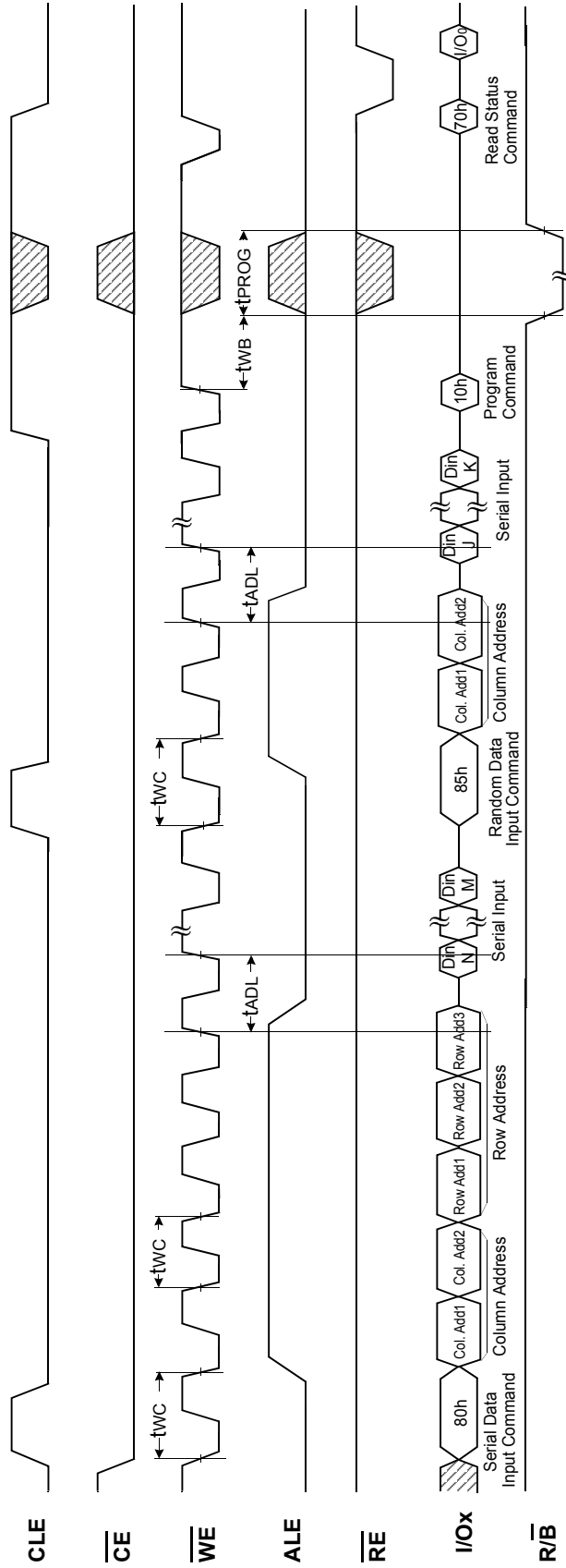


**Page Program Operation**



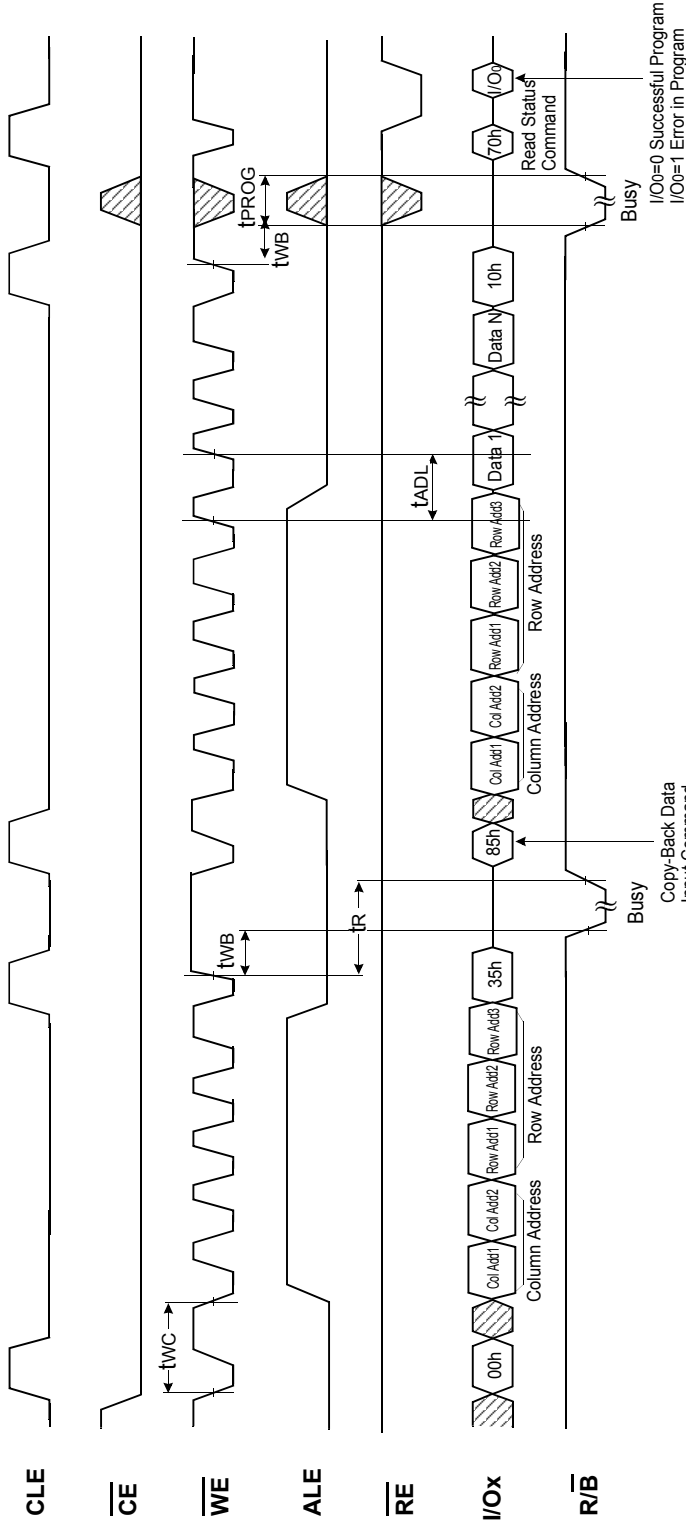
**NOTES** : tADL is the time from the  $\overline{WE}$  rising edge of final address cycle to the  $\overline{WE}$  rising edge of first data cycle.

Page Program Operation with Random Data Input



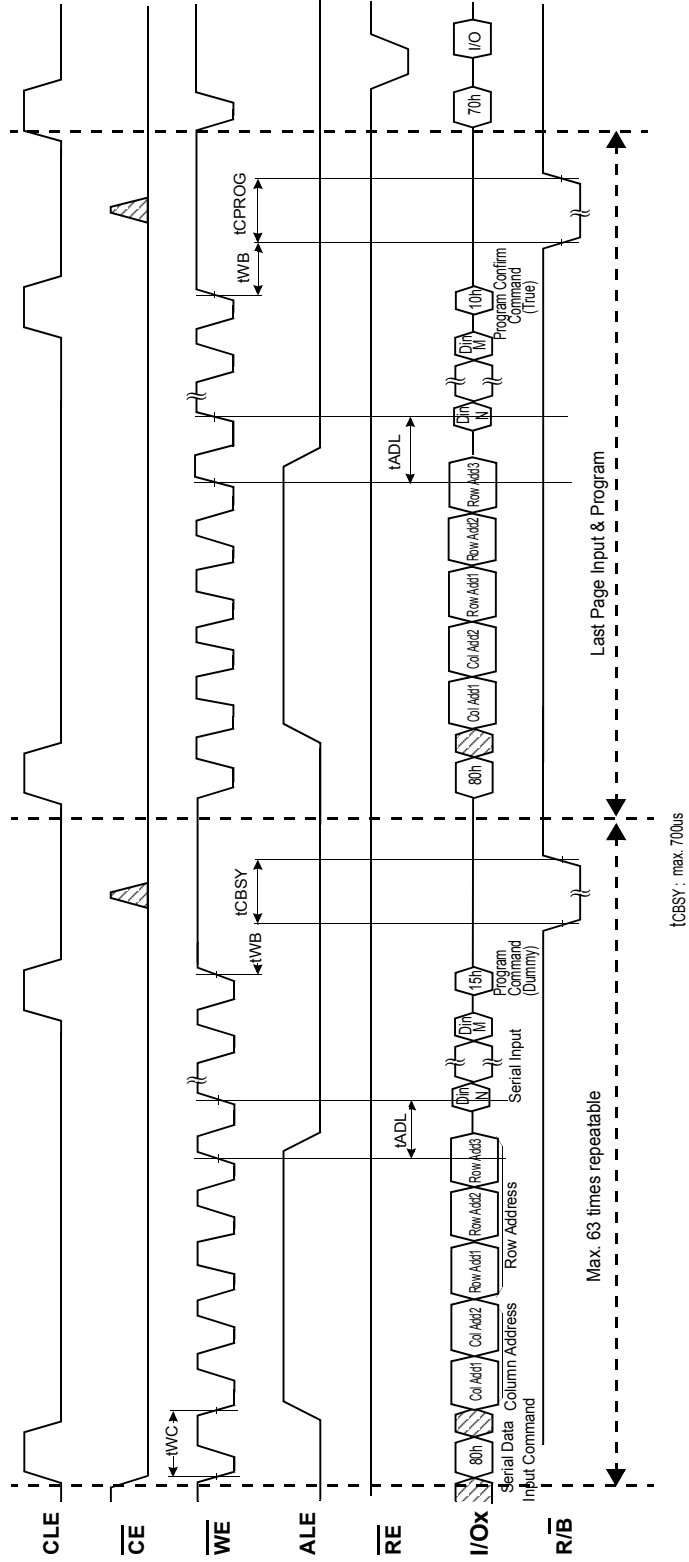
NOTES : tADL is the time from the  $\overline{WE}$  rising edge of final address cycle to the  $\overline{WE}$  rising edge of first data cycle.

Copy-Back Program Operation With Random Data Input



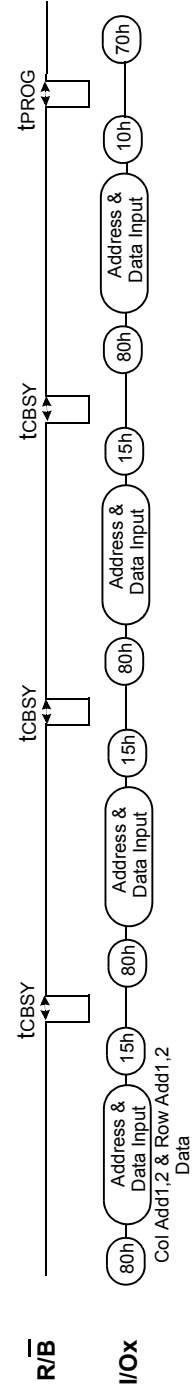
NOTES :  $t_{ADL}$  is the time from the  $\overline{WE}$  rising edge of final address cycle to the  $\overline{WE}$  rising edge of first data cycle.

Cache Program Operation (available only within a block)

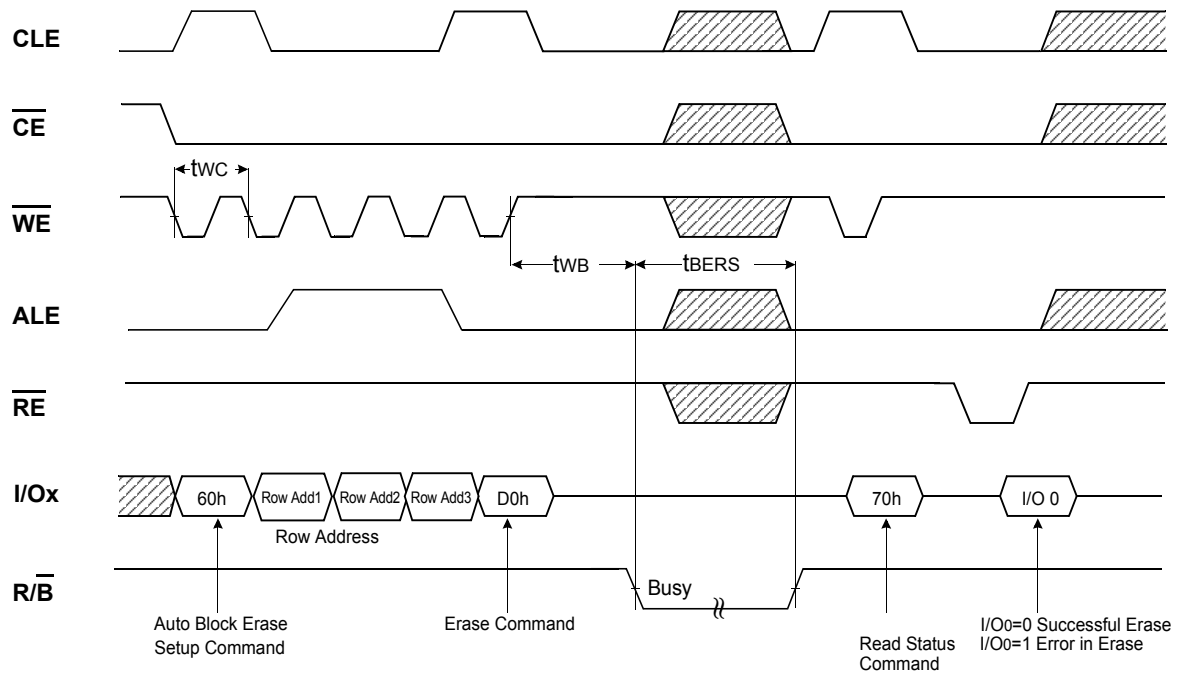


NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Ex.) Cache Program

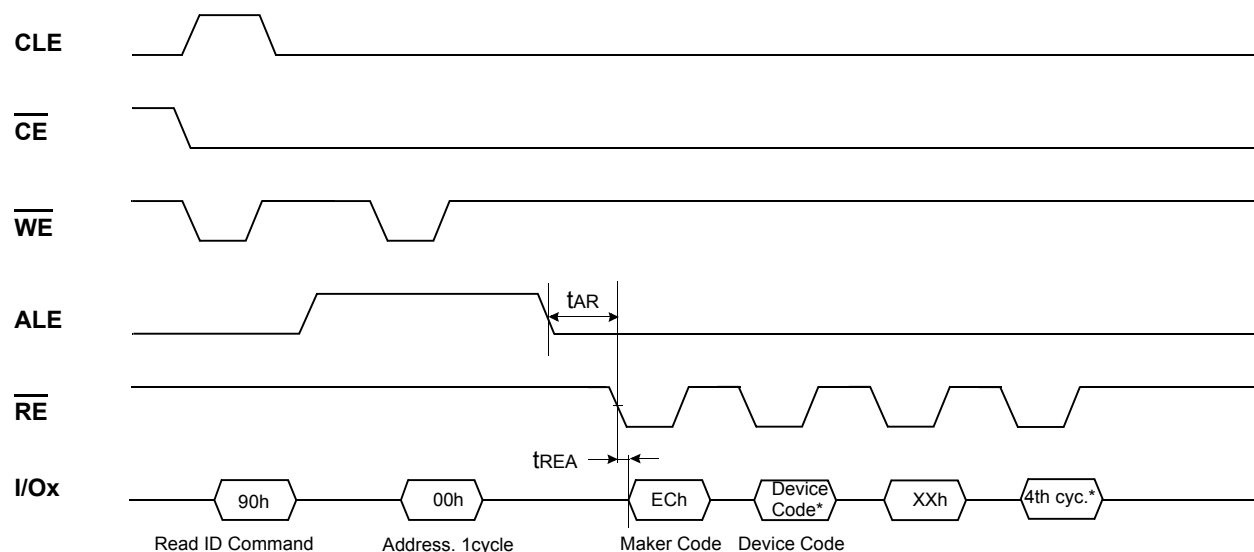


BLOCK ERASE OPERATION





**Read ID Operation**



Device	Device Code*(2nd Cycle)	4th Cycle*
K9K2G08U0A	DAh	15h

**ID Defintion Table**

**90 ID : Access command = 90H**

	Description
1 <sup>st</sup> Byte	Maker Code
2 <sup>nd</sup> Byte	Device Code
3 <sup>rd</sup> Byte	Don't care
4 <sup>th</sup> Byte	Page Size, Block Size, Spare Size, Organization

**K9K2G08U0A**

**Preliminary  
FLASH MEMORY**

**4th ID Data**

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area )	1KB							0	0
	2KB							0	1
	Reserved							1	0
	Reserved							1	1
Block Size (w/o redundant area )	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	Reserved			1	1				
Redundant Area Size ( byte/512byte)	8						0		
	16						1		
Organization	x8		0						
	x16		1						
Serial AccessMinimum	50ns/30ns/25ns	0				0			
	Reserved	1				0			
	Reserved	0				1			
	Reserved	1				1			

Device Operation

PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25μs( $t_R$ ). The system controller can detect the completion of this data transfer( $t_R$ ) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 30ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

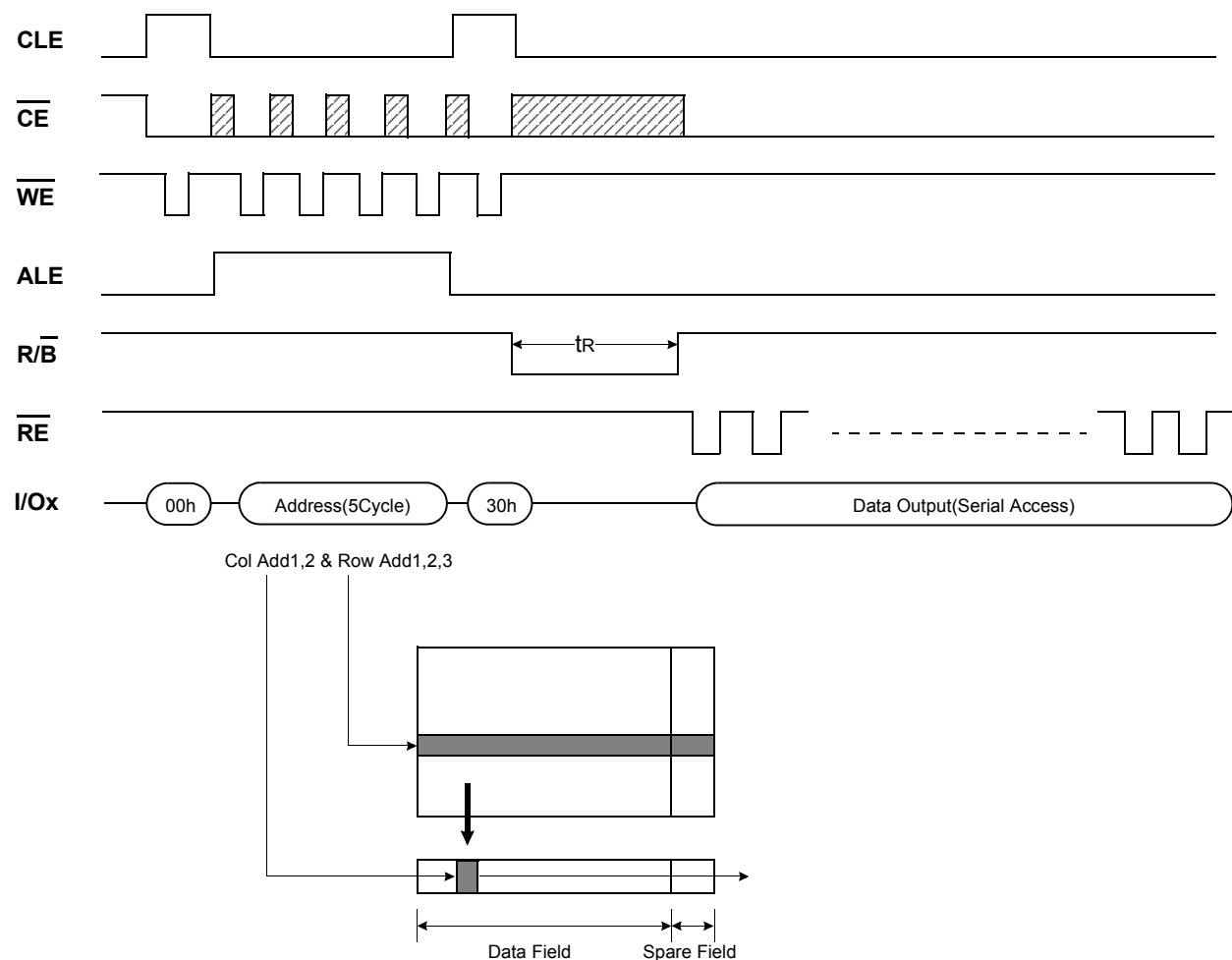
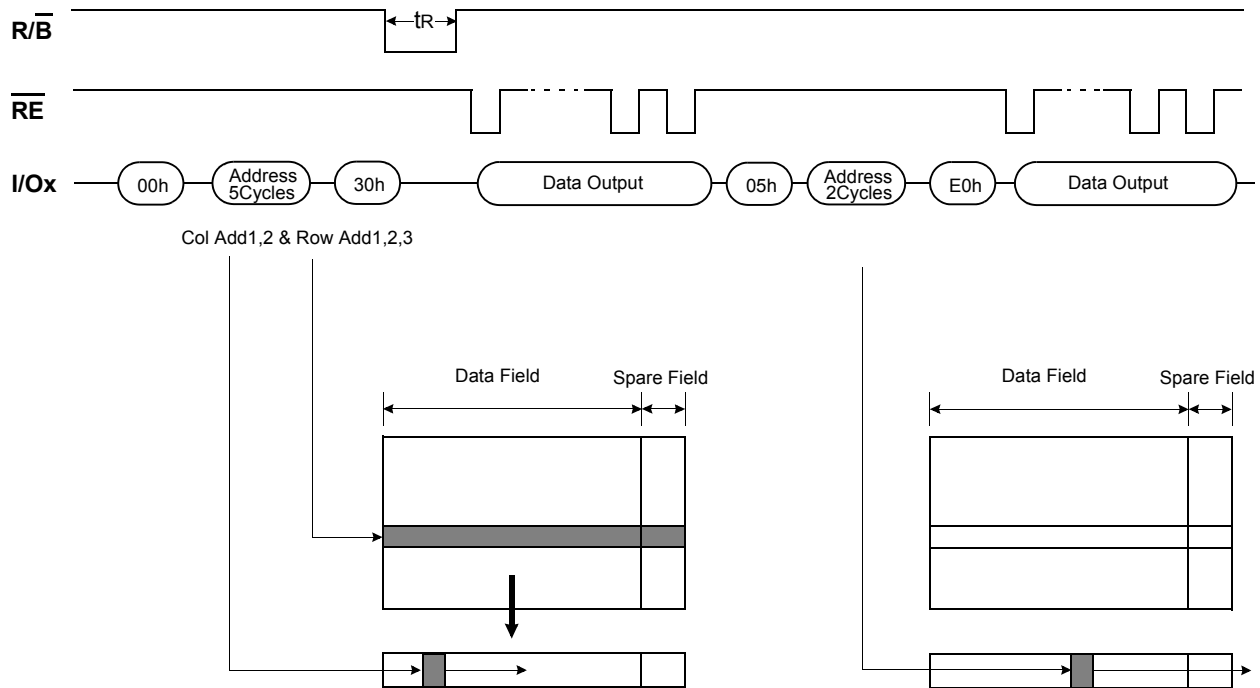


Figure 7. Random Data Output In a Page



**PAGE PROGRAM**

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a word or consecutive bytes up to 2112, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for main array(1time/512byte) and 4 times for spare array(1time/16byte). The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the  $\overline{R/B}$  output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation

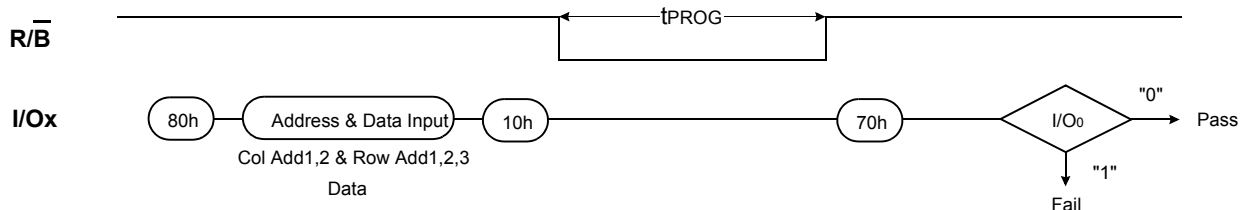
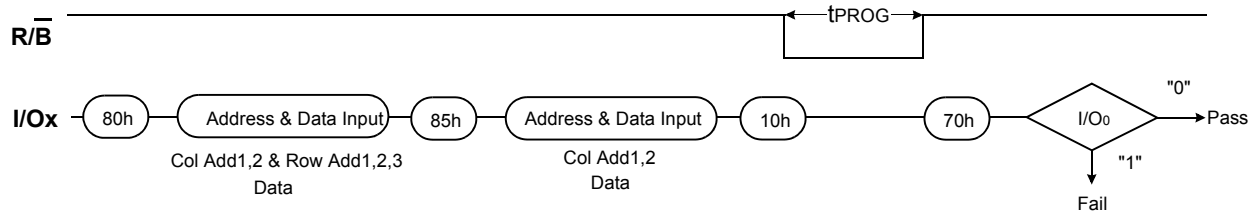


Figure 9. Random Data Input In a Page

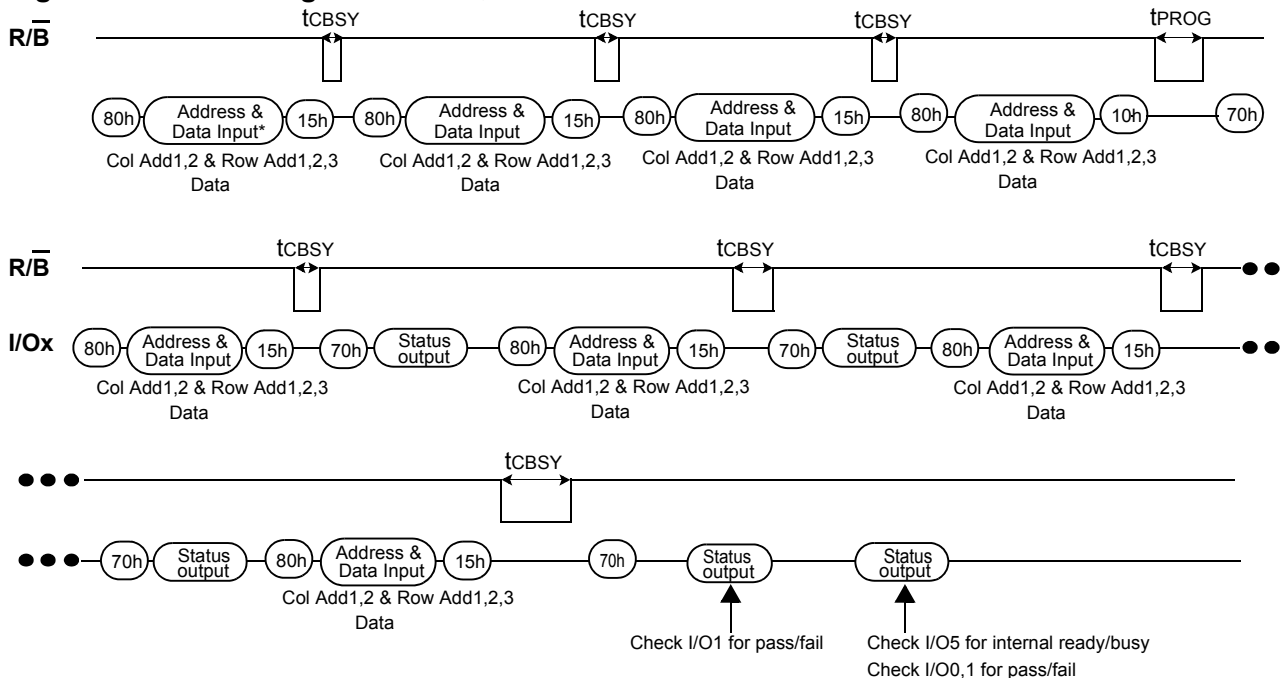


**Cache Program**

Cache Program is an extension of Page Program, which is executed with 2112byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2112byte into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time( $t_{CBSY}$ ) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command,  $t_{CBSY}$  is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O 5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B, the last page of the target programming sequence must be programmed with actual Page Program command (10h). If the Cache Program command (15h) is used instead, status bit (I/O5) must be polled to find out when the last programming is actually finished before starting other operations such as read. Pass/fail status is available in two steps. I/O 1 returns with the status of the previous page upon Ready or I/O6 status bit changing to "1", and later I/O 0 with the status of current page upon true Ready (returning from internal programming) or I/O 5 status bit changing to "1". I/O 1 may be read together when I/O 0 is checked.

Figure 10. Cache Program (available only within a block)



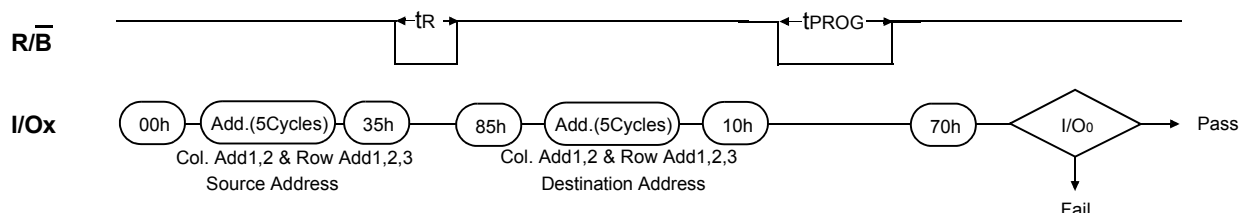
**NOTE :** Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

$$t_{PROG} = \text{Program time for the last page} + \text{Program time for the (last - 1)th page} \\ - (\text{Program command cycle time} + \text{Last page data loading time})$$

### Copy-Back Program

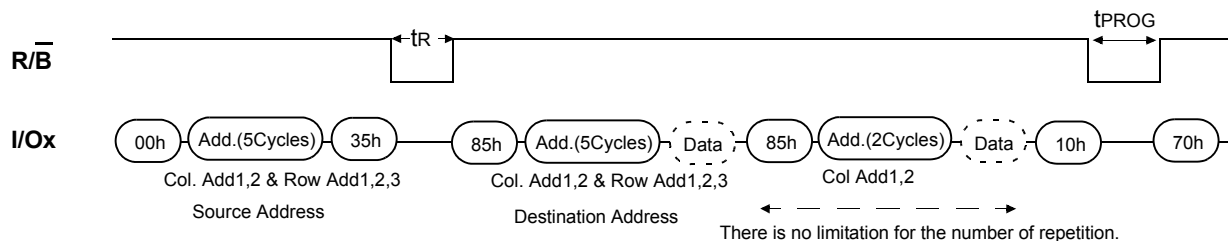
The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (85h) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. A27 must be the same between source and target page. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 11. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But if the source page has an error bit by charge loss, accumulated copy-back operations could also accumulate bit errors. In this case, verifying the source page for a bit error is recommended before Copy-back program"**

Figure 11. Page Copy-Back program Operation



**NOTE:** It's prohibited to operate Copy-Back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the Copy-Back program is permitted just between odd address pages or even address pages.

Figure 12. Page Copy-Back program Operation with Random Data Input

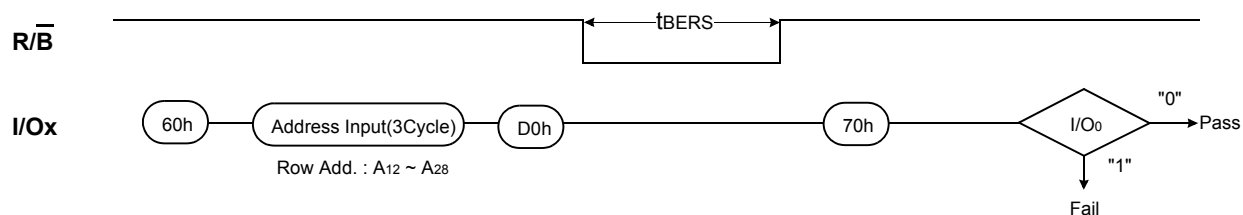


**BLOCK ERASE**

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A18 to A28 is valid while A12 to A17 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

**Figure 13. Block Erase Operation**



**READ STATUS**

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

**Table2. Read Staus Register Definition**

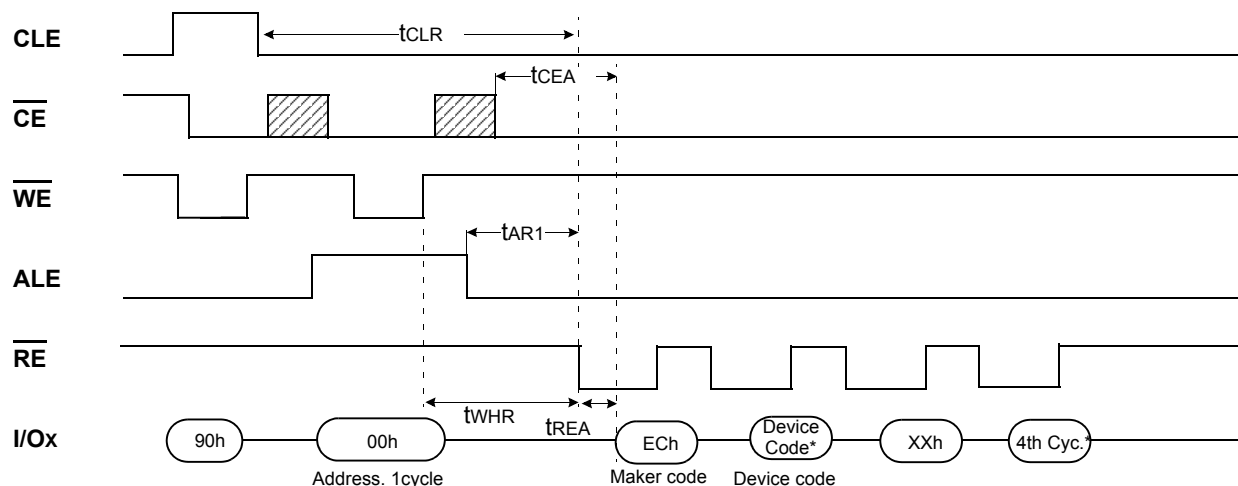
I/O No.	Page Program	Block Erase	Cache Program	Read	Definition	
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not use	Pass : "0"	Fail : "1"
I/O 1	Not use	Not use	Pass/Fail(N-1)	Not use	Pass : "0"	Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Don't -cared	
I/O 3	Not Use	Not Use	Not Use	Not Use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Ready/Busy	Ready/Busy	True Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected

**NOTE :** 1. True Ready/Busy represents internal program operation status which is being executed in cache program mode.  
2. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

**Read ID**

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and XXh, 4th cycle ID, 44h respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 14 shows the operation sequence.

**Figure 14. Read ID Operation**

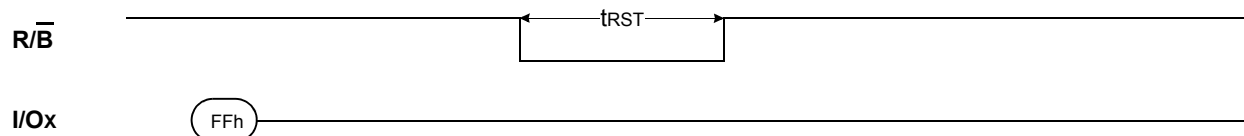


Device	Device Code*(2nd Cycle)	4th Cycle*
K9K2G08U0A	DAh	15h

**RESET**

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 15 below.

**Figure 15. RESET Operation**



**Table3. Device Status**

	After Power-up	After Reset
Operation Mode	00h command is latched	Waiting for next command



**READY/BUSY**

The device has a  $\overline{R/B}$  output that provides a hardware method of indicating the completion of a page program, erase and random read. The  $\overline{R/B}$  pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more  $\overline{R/B}$  outputs to be Or-tied. Because pull-up resistor value is related to  $t_r(\overline{R/B})$  and current drain during busy( $i_{busy}$ ), an appropriate value can be obtained with the following reference chart(Fig 17). Its value can be determined by the following guidance.

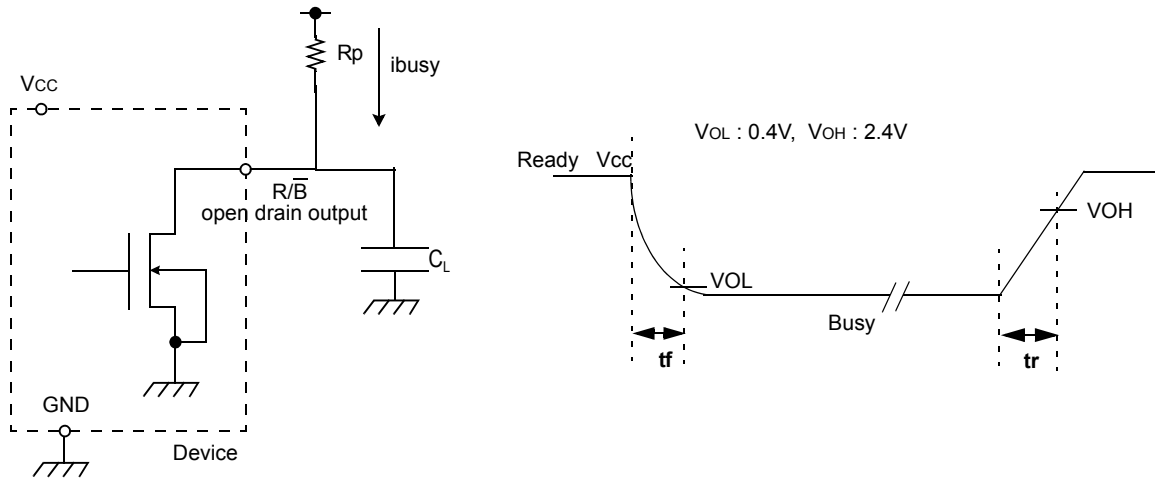
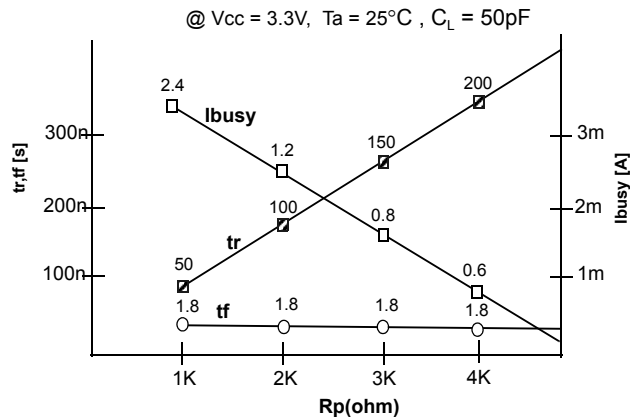


Figure 17. Rp vs tr ,tf & Rp vs ibusy



**Rp value guidance**

$$R_{p(\min)} = \frac{V_{cc(\text{Max.})} - V_{oL(\text{Max.})}}{I_{OL} + \sum I_L} = \frac{3.2V}{8\text{mA} + \sum I_L}$$

where  $I_L$  is the sum of the input currents of all devices tied to the  $\overline{R/B}$  pin.

$R_{p(\max)}$  is determined by maximum permissible limit of  $t_r$

**Data Protection & Power up sequence**

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever  $V_{cc}$  is below about 2V.  $\overline{WP}$  pin provides hardware protection and is recommended to be kept at  $V_{IL}$  during power-up and power-down. A recovery time of minimum  $10\mu s$  is required before internal circuit gets ready for any command sequences as shown in Figure 18. The two step command sequence for program/erase provides additional software protection.

**Figure 18. AC Waveforms for Power Transition**

