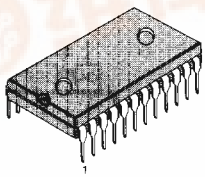
查询KA2914A供应商 捷多邦，专业PCB打样工厂，24小时加急出货

VIDEO IF+SIF SYSTEM

The KA2914A, KA2918 are silicon monolithic integrated circuits designed for the VIF and SIF stage in color and B/W television receivers.

KA2914A: for Reverse AGC type
KA2918: for Forward AGC type

24 DIP



FUNCTIONS

VIF

- Three controlled IF amplifier stages
- Video demodulator controlled by picture carrier
- Black noise and white noise inverter
- Peak AGC.
- DC amplifier for RF AGC out

SIF

- Three differential IF amplifier stages
- Phase detector
- DC controlled attenuator
- Audio amplifier stage with NFB terminal

FEATURES

- **PIF, SIF, ATT audio driver**
- **2 chip color TV system is possible with** the KA2153 or KA2154

VIF

- **High gain, wide band IF amplifier**
- **AGC characteristics with excellent stability**
- **Excellent DG/DP characteristics**
- Excellent S/N characteristics due to delayed 3-stage AGC action
- **Negative video output signal**
- **Switch off the video part with VTR SW**

SIF

- **Excellent limiter characteristics**
- **Excellent attenuator characteristics**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2914A	24 DIP	−20 ~ +65°C
KA2918		

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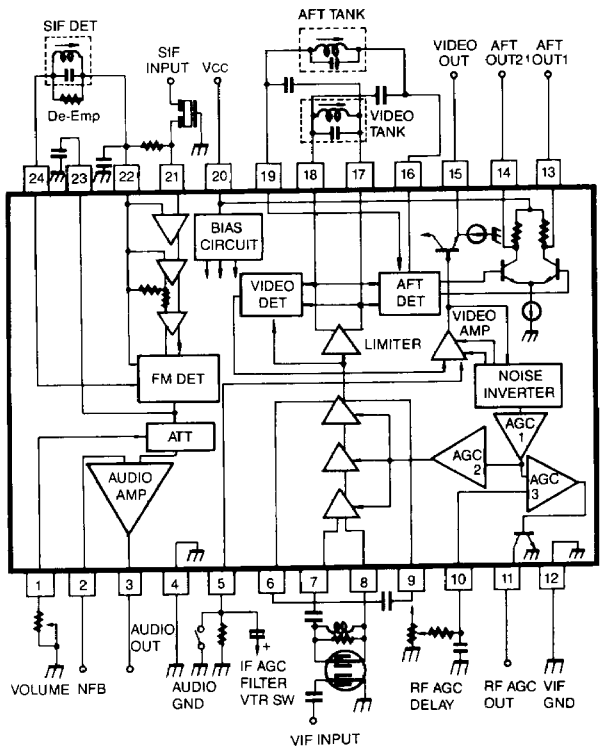
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Terminal 11 Open Voltage	V_{11}	15	V
Video DC Output Current	I_{15}	6	mA
Audio DC Output Current	I_3	3	mA
Terminal 2 Voltage	V_2	15	V
Power Dissipation (Note)	P_d	1.6	W
Operating Temperature	T_{opr}	−20 ~ 65	°C
Storage Temperature	T_{stg}	−55 ~ 150	°C

Note: Derated above T_a =25°C in the proportion of 12.8 mW/°C.

ELECTRICAL CHARACTERISTICS
PIF Section (T_a =25°C, V_{CC} =12V f_p =45.75MHz, f_s =41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	V_{CC}	—	10.8	12.0	13.2	V	—
Supply Current	I_{CC}	—	50	72	95	mA	1
Video DC Output Voltage	V_{15}	SW_1: 1 (KA2914A) 2 (KA2918) SW_2: 2	5.2	5.5	5.8	V	1
AFT DC Output Voltage	V_{13}	SW_1: 1 (KA2914A) 2 (KA2918) SW_2: 2	5.3	6.8	8.3	V	1
	V_{14}	SW_1: 1 (KA2914A) 2 (KA2918) SW_2: 2	5.3	6.8	8.3	V	1
AFT DC Offset Voltage	$\Delta V_{13\text{-}14}$	SW: 1 (KA2914A) 2 (KA2918) SW: 2	−1.5	0	1.5	V	1
RF AGC Residual Output Voltage	V_{11} Sat	SW_1: 1 (KA2914A) 2 (KA2918) SW_2: 2	—	—	0.5	V	1
RF AGC Leak Current	$I_{11\ LEAK}$	SW_1: 1 (KA2918) 2 (KA2914A) SW_2: 1	—	—	1	uA	1
Video Sensitivity	v_I Pin 7-8	(Note 1)	60	150	250	μV_{rms}	2
AGC Range	ΔA_{VIF}	(Note 2)	60	64	—	dB	2
SYNC TIP Level Voltage	V_{SYNC} (V_{15})	(Note 3)	2.3	2.5	2.7	V	2
Max. IF Input Voltage	v_{IN} Max PIF	(Note 4)	100	120	—	mV_{rms}	2
White Noise Threshold Level	V_{WTH} (V_{15})	(Note 5)	5.8	6.2	6.6	V	2
White Noise Clamp Level	V_{WCL} (V_{15})	(Note 5)	3.7	4.1	4.5	V	2

ELECTRICAL CHARACTERISTICS
PIF Section (T_a=25°C, V_{CC}=12V, f_P=45.75MHz, f_S=41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Black Noise Threshold Level	V_{BTH} (V_{15})	(Note 5)	1.4	1.6	1.8	V	2
Black Noise Clamp Level	V_{BCL} (V_{15})	(Note 5)	2.9	3.3	3.7	V	2
Video Frequency Response	f_{BW}	(Note 6)	4.5	5.5	—	MHz	3
Suppression of Carrier	CL	(Note 7)	40	50	—	dB	4
Suppression of 2nd Carrier	I_{2nd}	(Note 8)	40	50	—	dB	4
920KHz Beat Level	I_{920}	(Note 9)	33	38	—	dB	4
Differential Phase	DP	(Note 10)	—	3.5	5	deg	5
Differential Gain	DG	(Note 10)	—	7	10	%	5
VIF Input Impedance	R_{IN} (VIF)	(Note 11)	1.5	3.0	6.0	KΩ	6
	C_{IN} (VIF)		—	3.0	10.0	pF	
AFT Sensitivity	$\Delta F/V_{13\text{-}14}$	(Note 12)	—	16	—	kHz/V	2
AFT Output Voltage Upper	V_{13U} V_{14U}	(Note 13)	11.7	11.9	12.0	V	2
AFT Output Voltage Lower	V_{13L} V_{14L}	(Note 13)	1.8	2.3	2.8	V	2
RF AGC Max Available Current	I_4 Max	SW_1: 1 SW_2: 1 (KA2914A)	0.3	—	—	mA	1
		SW_1: 2 SW_2:1(KA2918)	7.0	—	—		
RF AGC Delay Setting Range	V_{IN} Delay	(Note 14)	5	7	9	V	
AFT Band width	ΔF_W	(Note 13)	1.4	—	—	MHz	2
Video Output Voltage	V_{OUT}	(Note 15)	2.25	2.50	2.75	V	2

ELECTRICAL CHARACTERISTICS
SIF Section (T_a =25°C, V_{CC} =12V, f_p =45.75MHz, f_s =41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
SIF Output Voltage	S_{OUT}	(Note 16)	200	400	600	mV_{rms}	3
Input Limiting Voltage	$v_{IN(LIM)}$	(Note 17) $R_D = \infty$	—	200	400	uV_{rms}	8
AM Rejection Ratio	AMR	SIF IN: f = 4.5 MHz fm = 400Hz, Δf = ±25kHz AM 30%, V_{IN} = 100dBu	40	45	—	dB	8
Recovered Output Voltage	V_{OD}	SIF IN: f=4.5MHz fm=400Hz, Δf= ±25kHz V_{IN} =80dBu, R_D =12kΩ	0.5	0.75	—	V_{rms}	8
Total Harmonic Distortion	THD_{DET}	SIF IN: f=4.5MHz fm=400Hz, Δf= ±25kHz V_{IN} =80dBu	—	1.0	—	%	8
Max. Audio Output Voltage	v_{OM}	SIF IN: f=4.4 ~ 4.6MHz	4.0	—	—	V_{p-p}	8
SIF Input Impedance	$R_{IN(SIF)}$	f=4.5MHz	10.0	20.0	30.0	KΩ	7
	$C_{IN(SIF)}$		—	3.0	—	pF	
DET Output Impedance	R_O (DET)	(Note 18)	10.0	15.0	20.0	KΩ	9
DC Voltage — Terminal 21	V_{21}	SW_1: 1 (KA2914A) 2 (KA2918) SW_2: 2	3.5	4.4	5.3	V	1
DC Voltage — Terminal 23	V_{23}		4.8	6.0	7.2	V	
DC Voltage — Terminal 1	V_1		6.0	6.7	7.4	V	
Max. Attenuation	ATT Max	(Note 19)	60	—	—	dB	10
DC Volume Gain	G_{ATT} Min	R_A =0 G_{ATT} Min=20log $\frac{v_2}{v_{23}}$	−5.5	−3.5	−1.5	dB	10
ATT Characteristics 1	V_1 (1)	*	3.4	3.8	4.2	V	10
ATT Characteristics 2	V_1 (2)	**	4.5	4.9	5.3	V	10
Signal Leakage	V_{PT}	(Note 20)	—	1.0	3.0	mV_{rms}	11
AF AMP. Gain	G_V AF	(Note 21)	—	20	—	dB	13
AF AMP. Distortion	THD AF	P_{23A} =1V_{pp}, 400Hz SW_3: On ATT: −26dB Setting	—	1.5	—	%	12
AF AMP. Max. Output Voltage	v_{OAF} Max	(Note 21) THD_{AF} 5%	1.5	2.0	—	V_{rms}	13
AF Output DC Voltage	V_3	SW_1: 1 (KA2914A) 2 (KA2918) SW_2: 2	6.7	7.7	8.8	V	1

* Read the 400Hz component of V_{AI} at P_2 with R_A =0, set R_A so that $V_{AI'}$ =1/2 V_{AI} (−6dB), then read DC voltage of terminal 1 (V_1).

** Read the 400Hz component of V_{AI} at P_2 with R_A =0. Set R_A so that $V_{AI'}$ =3.16×10^{-3} V_{AI} (−50dB) then read DC voltage of terminal 1 (V1).

TEST CIRCUIT

1. DC Characteristic

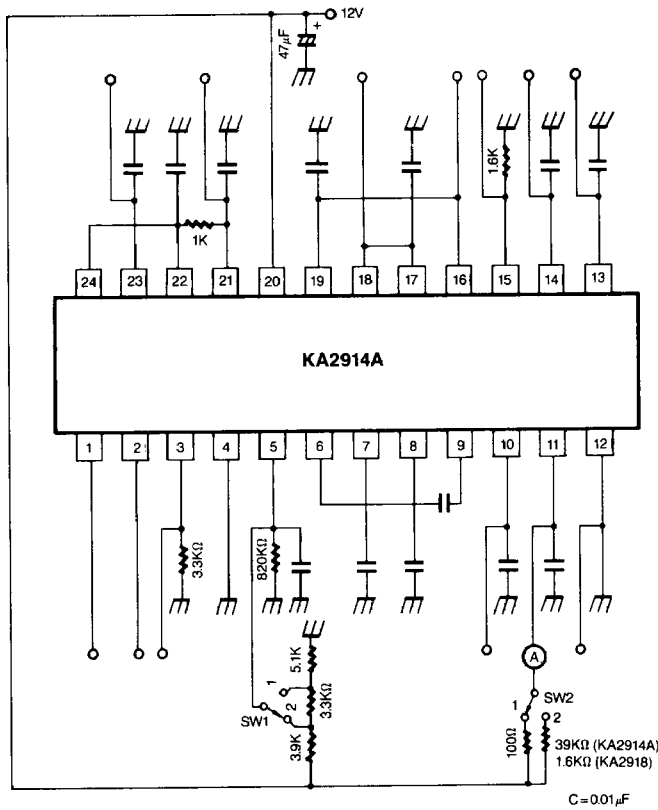


Fig. 1

2. AC Characteristic

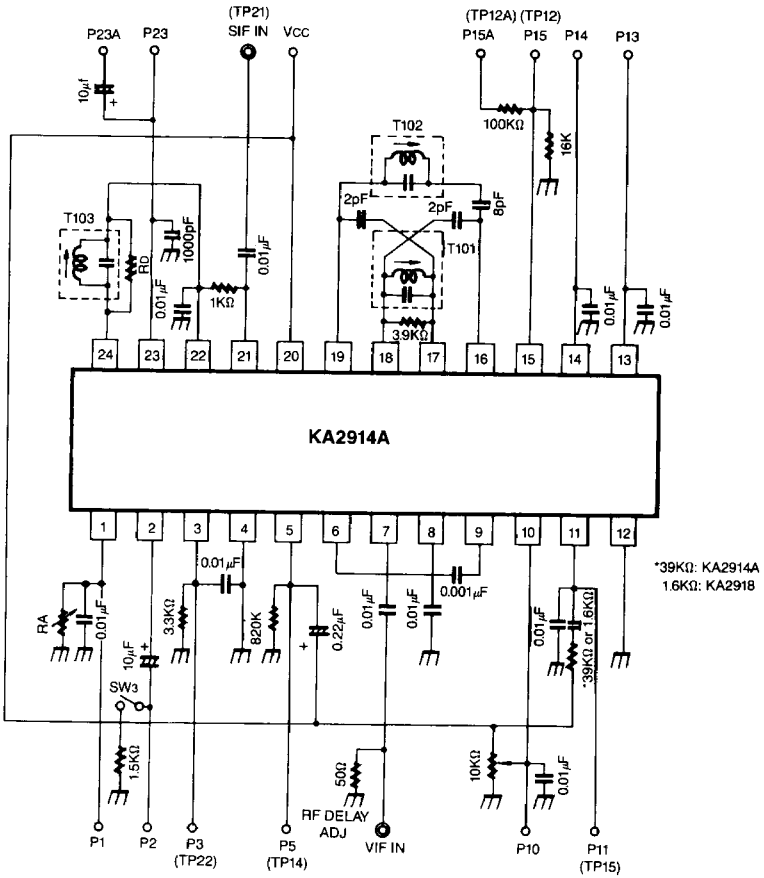


Fig. 2

3. Video Frequency Response and SIF Output Voltage

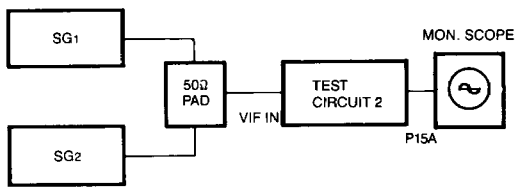


Fig. 3

4. Inter Modulation

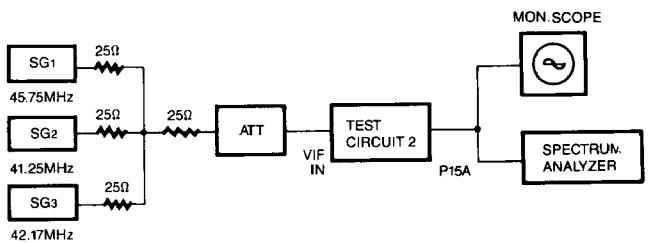
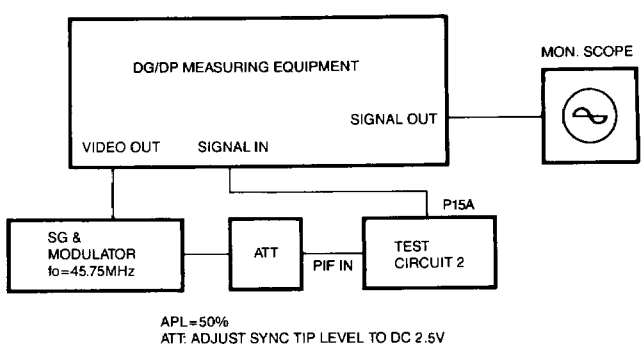


Fig. 4

5. DG, DP



APL=50%
ATT: ADJUST SYNC TIP LEVEL TO DC 2.5V

Fig. 5

6. VIF Input Impedance

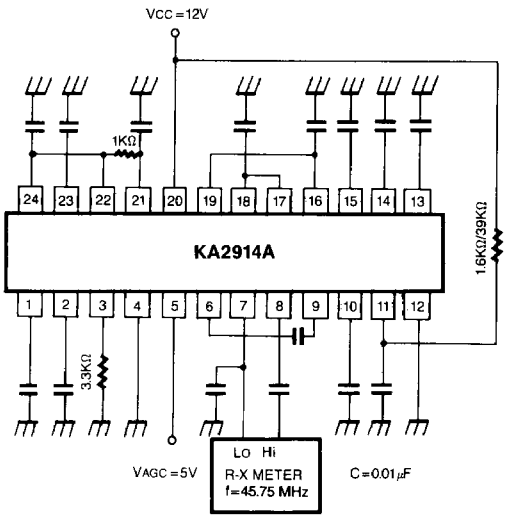


Fig. 6

7. SIF Input Impedance

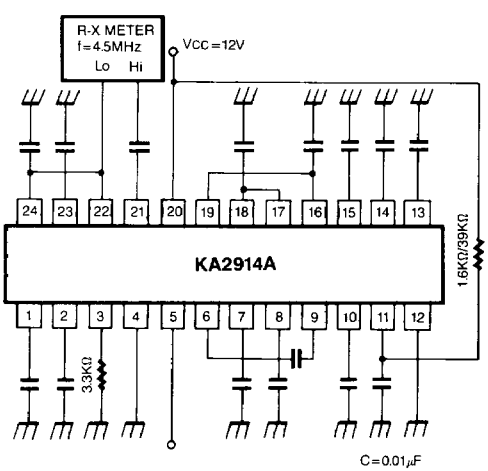


Fig. 7

8. $v_{IN\,(LIM)}$, AMR, V_{OD}, THD, v_{OM}

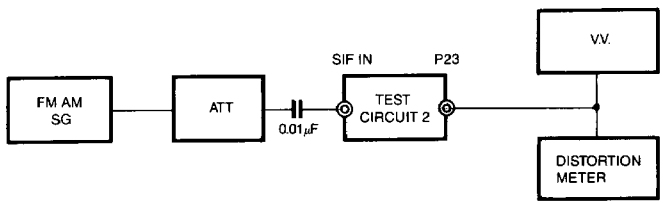


Fig. 8

9. Audio Output Impedance

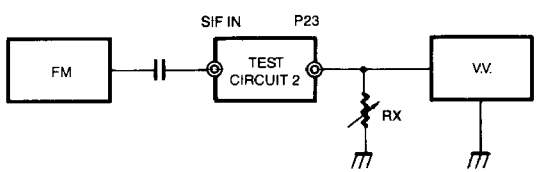


Fig. 9

10. ATT MAX., G_{ATT} MIN, $V_{1\,(1)}$, $V_{1\,(2)}$

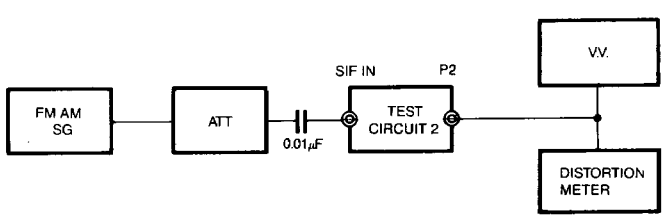


Fig. 10

11. v_{PT}

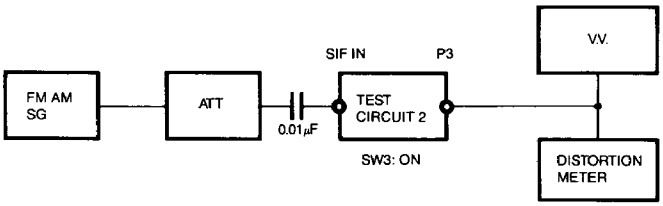


Fig. 11

12. THD_{AF}

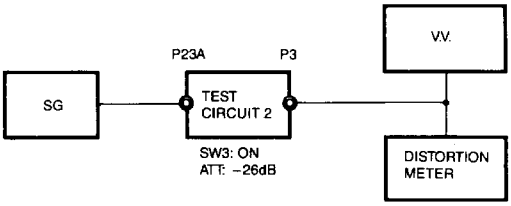


Fig. 12

13. G_V AF, $v_{OAF\ MAX}$

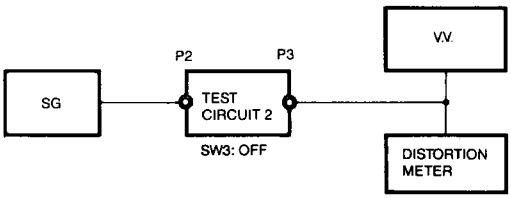


Fig. 13

TEST CONDITIONS

Note 1) V_{AGC} (P5 EXT. Applying voltage)=11.5V
VIF in: f=45.75MHz 1kHz 30% AM modulation
Adjust the VIF input level υ so that the detected output of P15A with high impedance probe will be $0.8V_{p\text{-}p}$ and measure the input level.

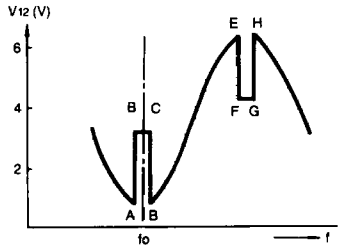
Note 2) V_{AGC}=4V
Measure VIF input level υ same as note 1

$$\Delta A = 20 \log \frac{\upsilon}{\upsilon} \text{(dB)}$$

Note 3) VIF IN: f=45.75MHz CW 15mVrms
Measure the DC level of P15

Note 4) VIF IN: f=45.75MHZ APL 100%, 87.5% AM modulation.
P5: open
(1) Adjust the VIF input level $50mV_{p\text{-}p}$ and measure the detected output level $\upsilon_{01p\text{-}p}$
(2) Then increase the input level so that the detected output level will be $1.1\times \upsilon_{01p\text{-}p}$ and measure the input level.

Note 5) V_{AGC}=8V
VIF in: f=45.75MHz±10MHz variable or sweep 15mVrms measure the DC level of P15.



Note 6) V_{AGC}=8V (GR≈30dB)
SG_1: 45.75MHz CW
SG_2: 45.75~40MHz variable
(1) Setting output of SG_1 so that the DC level of P15 will be 4.0V
(2) Setting output off SG_2 (45.75MHz) so that the AC level of P15 will be $0.5V_{p\text{-}p}$
(3) Decreasing frequency of SG_2 until the AC level of P15 will be $0.35V_{p\text{-}p}$ (−3dB of $0.5V_{p\text{-}p}$) then read f_{SG2}=F f_{BW}=45.75-F MHz

Note 7) SG_1: 45.75MHz, 1kHz 80% AM modulation 100mVrms
SG_2, SG_3; off
Setting V_{AGC} so that the output AC level of P15 will be $2.7V_{p\text{-}p}$
Measure CL of P15 after setting to 0% AM of SG_1

$$CL = 20 \log \frac{2.7}{\upsilon_{CR}\,(V_{P\text{-}P})} \text{ (dB)}$$

Note 8) Measure I_{2nd} of P15 the same as note 7

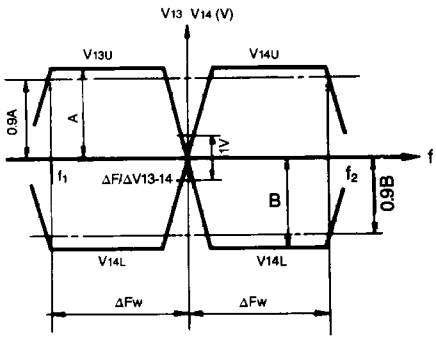
Note 9) V_{AGC}=8V
SG_1: 45.75MHz (P: picture) 100mVrms
SG_2: 41.25MHz (S: sound) 32mVrms (−10dB of SG_1)
SG_3: 42.17MHz (C: chroma) 32mVrms (−10dB of SG_1)
(1) Setting V_{AGC} so that the output tip level (lower) of P15 will be 3.0V DC
(2) Measure the level difference (dB) between the C-level and 920kHz level

Note 10) V_{AGC}=8V
VIF IN: f=45.75MHz video signal (RAMP) 87.5% AM $100mV_{p\text{-}p}$
Setting ATT so that the SYNC TIP level of P15 will be 2.5V DC.
Measure DP and DG

Note 11) V_{AGC}=5V f=45.75MHz
Measure R_{IN}, C_{IN}

Note 12) AFT sensitivity $\Delta F/\Delta\,(V_{13}\text{-}V_{14})$
(1) INT, AGC (P5 open)
(2) VIF input: 45.75MHz ± 1.0MHz, CW 15mVrms
(3) Read the frequency (f_1) of VIF when $V_{13}\text{-}V_{14}$ = −IV
(4) Read the frequency (f_2) of VIF when $V_{13}\text{-}V_{14}$ = 1V then calculate
$\Delta F/\Delta(V_{13}\text{-}V_{14}) = |f_1\text{-}f_2|$

Note 13) ΔF_W, V_{13U}, V_{14U}, V_{13L}, V_{14L}
(1) INT AGC (P5 open)
(2) VIF IN: 45.75MHz±10MHz CW 15MVrms
(3) 8pF at Pin 16 should be shorted
(4) Read the frequency (f_1 or f_2) when the V_5 or V_6 is reduced to 90% of the level of A or B with varying the frequency. Then the band width is the difference from center frequency (f_0).



Note 14) P5: Open
VIF IN: 45.75MHz CW 20mVrms
(1) Adjust the voltage of Terminal 3 so that the voltage of Terminal 4 will be 6.0V DC
(2) Measure the voltage of Terminal 3

Note 15) P5: Open
VIF in: 45.75MHz 100% APL 87.5% AM modulation signal amplitude $50mV_{p-p}$ Measure the detected output voltage (White peak to sync tip)

Note 16) P5: Open
SG_1: 45.75MHz CW 100mVrms
SG_2: 41.25MHz CW 25mVrms
Measure SIF (4.5MHz) output voltage at P15

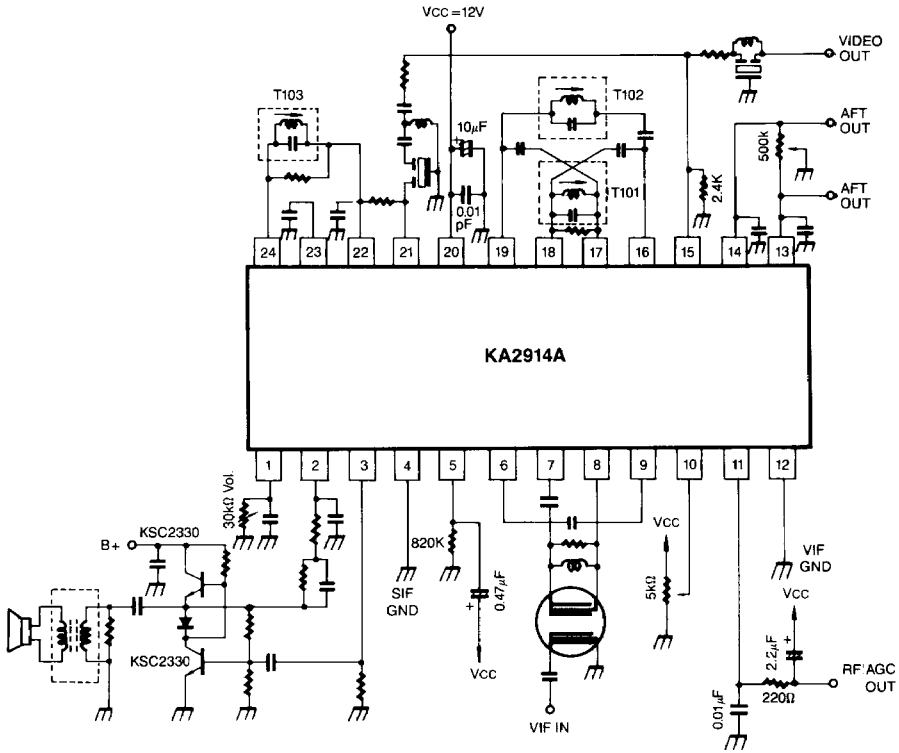
Note 17) SIF IN: f=4.5MHz FM f_{MOD}=400Hz $\Delta f=\pm 25kHz$,
(1) Adjust the SIF input level $100mV_{p-p}$ and measure the detected output level v_{OS}
(2) Then decrease the input level so that the detected output level will be 3dB down of V_{OS} and measure the input level

Note 18) Output impedance
(1) SIF IN: f=4.5MHz f_{MOD}=400Hz, $\Delta f=\pm 25kHz$, 80dBμ
(2) At P23 read the V_{01} at R_X= , then read the R_X when the recovered output becomes $V_{01/2}$ by varying the R_X. The R_X is the output impedance.

Note 19) ATT MAX
(1) SIF in: f=4.5MHz, f_{MOD}=400Hz, f=±25kHz, 80dBμ
(2) Read the 400Hz component of V_{AI} at P2 with R_A=0, then read V_{AI}' with R_A=|∞

$$\text{ATT MAX}=20\log\frac{V_{AI}}{V_{AI}'}$$

Note 20) v_{PT}
(1) SIF IN: f=4.5MHz, f_{MOD}=400Hz, $\Delta f=\pm 25kHz$, 80dBμ
(2) Read the 400Hz component at P3

Note 21) G_V AF
(1) Apply 400Hz 0.1Vrms signal to P2
(2) Read the output voltage at P3

TYPICAL APPLICATION CIRCUIT