SAMSUNG ELECTRONICS

KAD0228BD

8-Bit 30 MSPS CMOS A/D Converter

Data Sheet

OVERVIEW

The KAD0228BD is a CMOS 8-bit A/D converter for video applications. It is a two-step ping-pong A/D converter consisting of reference resistor matrix, coarse 4-bit ADC and fine 4-bit ADC. Its maximum conversion rate is 30MSPS and supply voltage is 5V single.

FEATURES

- Resolution: 8-bit
- Differential Linearity Error: ± 0.6 LSB Typ.
- Maximum Conversion Rate: 30MSPS
- Sample and Hold Function Included
- Low Power Consumption: Less than 90mW (at 20MSPS Typ.)
  (Reference Current Excluded)
- Digital Input: CMOS Level
- 3-state TTL Compatible Output
- Built-in Reference Voltage Bias Circuit
- Reference Impedance: 300 Ω
- Power Supply: 5V single

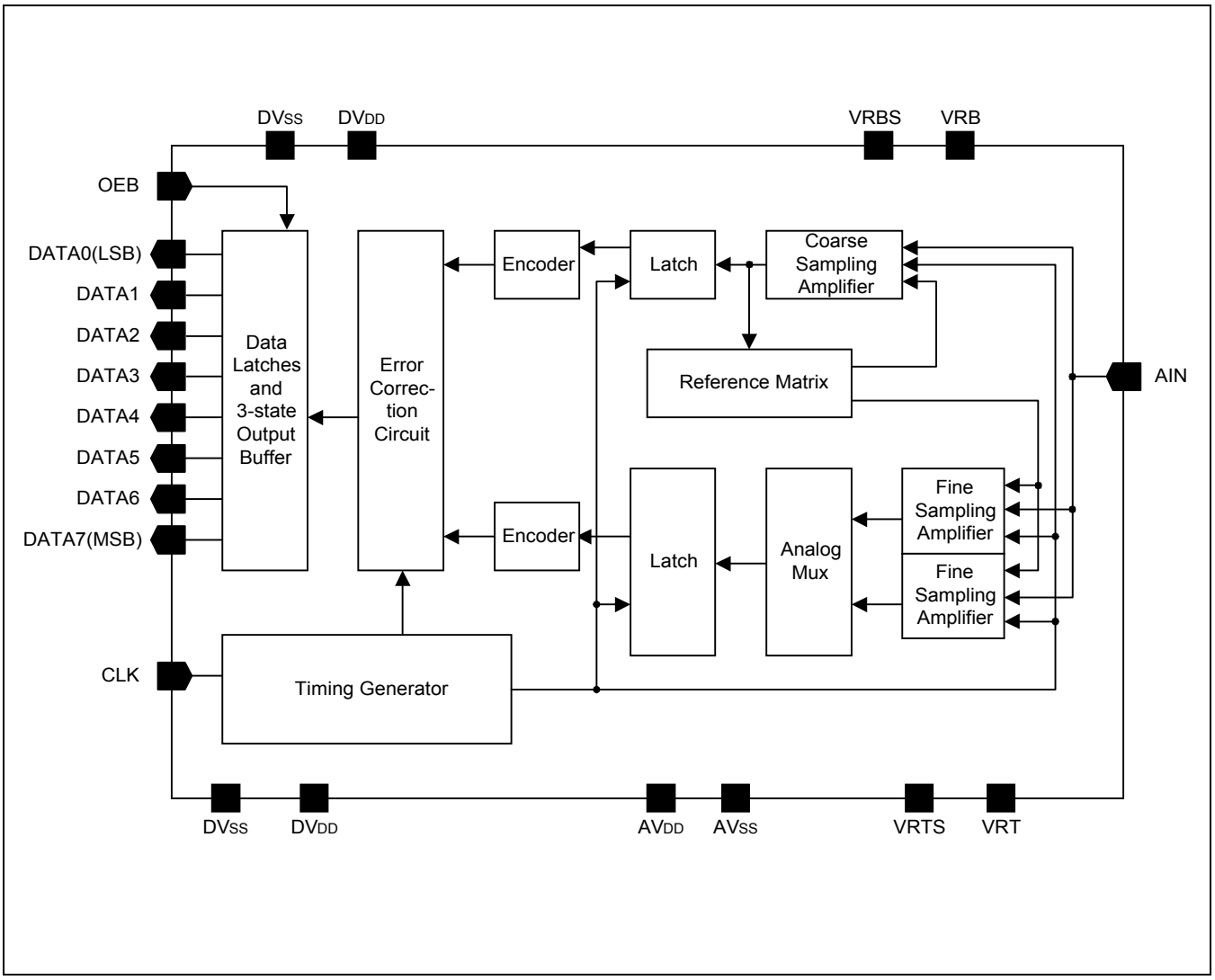
ORDERING INFORMATION

Device	Package	Temperature Range
KAD0228BD	24-SOP-300	0 to +70 °C

TYPICAL APPLICATIONS

- PC or computer based video signal processing such as multi-media, frame-grabber, scanner, etc.
- General purpose video applications including camcorder, digital video (TV/VCR), broadcasting and studio equipments.
- Medical electronics such as ultra-sound, imaging.
- High speed instrumentations such as digital scope, transit recorder, radar.

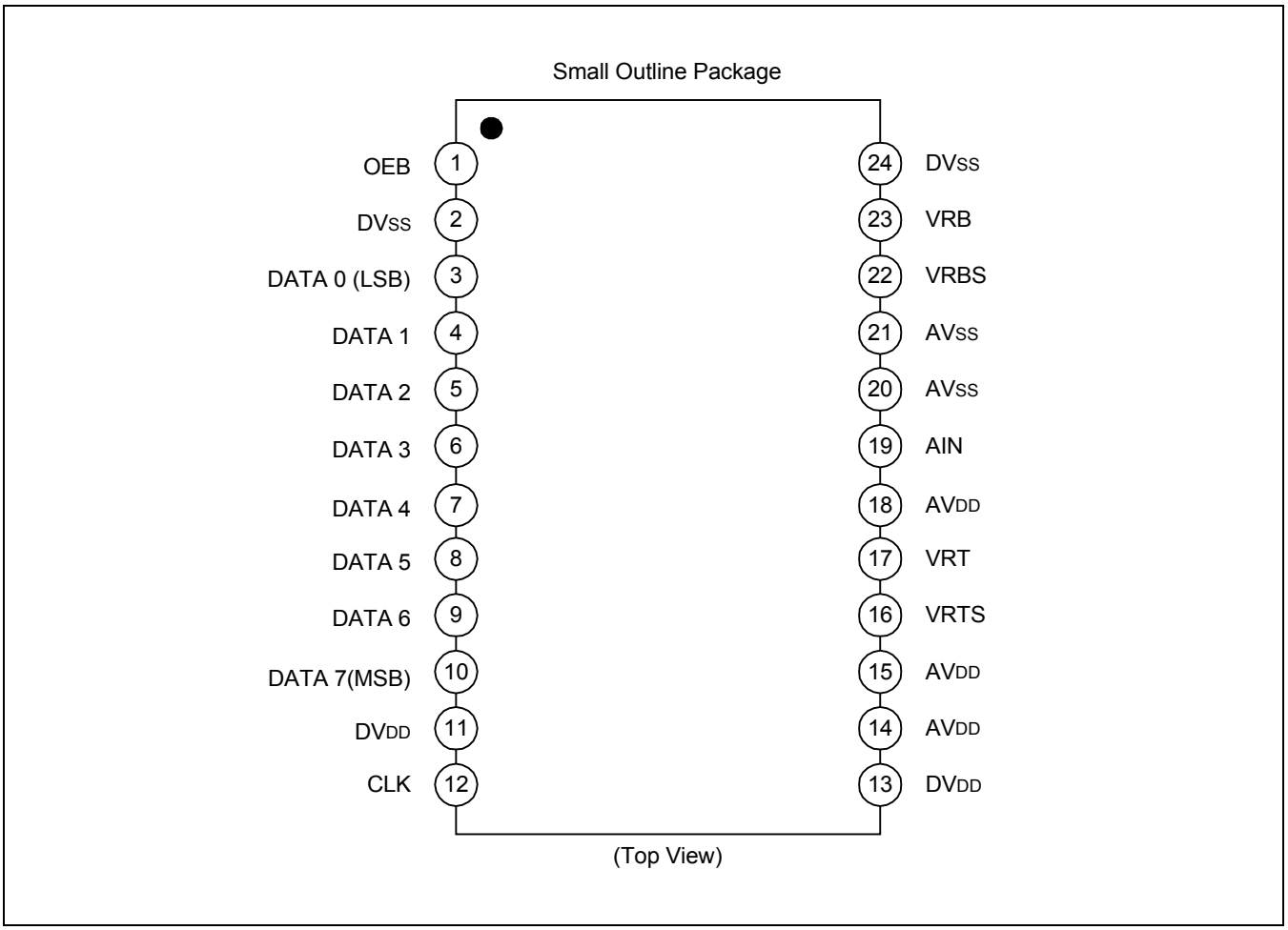
BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Description
1	OEB	I	3-state output enable. 3-state when OEB = V_{DD}, enable when OEB = V_{SS}
2	DV_{SS}	–	Digital ground for digital output buffer
3	DATA 0	O	Digital output data (LSB)
4	DATA 1	O	Digital output data
5	DATA 2	O	Digital output data
6	DATA 3	O	Digital output data
7	DATA 4	O	Digital output data
8	DATA 5	O	Digital output data
9	DATA 6	O	Digital output data
10	DATA 7	O	Digital output data (MSB)
11	DV_{DD}	–	Digital supply for digital output buffer
12	CLK	I	CMOS digital clock input
13	DV_{DD}	–	Digital supply for digital interior circuitry
14	AV_{DD}	–	Analog supply for comparator, reference resistor switch
15	AV_{DD}	–	Same as pin No. 14
16	VRTS	O	Internal self-biased reference top. Shorted with VRT pin (17), generates 2.6 V.
17	VRT	I	Reference resistor top side
18	AV_{DD}	–	Same as pin No. 14
19	AIN	I	Analog input
20	AV_{SS}	–	Analog ground for comparator, reference resistor switch
21	AV_{SS}	–	Same as pin No. 20
22	VRBS	O	Internal self-biased reference bottom. Shorted with VRB pin (23), generates 0.6 V.
23	VRB	I	Reference resistor bottom side
24	DV_{SS}	–	Digital ground for digital interior circuitry

PIN CONFIGURATION (24 SOP)



ABSOLUTE MAXIMUM RATINGS (NOTE 1 & 2)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 7.0	V
Analog Input Voltage	AIN	V_{SS} to V_{DD}	V
Reference Input Voltage	VRT, VRB	V_{SS} to V_{DD}	V
Storage Temperature Range	Tstg	–55 to +125	°C
Operating Temperature Range	Topr	–20 to +75	°C
ESD Susceptibility (note 3)	Vesd	> ± 1500	V

NOTES:

1. ABSOLUTE MAXIMUM RATINGS are those values beyond which the device may be damaged permanently. Normal operation is not guaranteed at or above these extremes.
2. All voltages are measured with respect to the V_{SS} voltage level otherwise specified.
3. 100pF discharged through a 1.5kΩ resistor (Human body model).

RECOMMENDED OPERATING CONDITIONS (NOTE 4)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	AV_{DD} - AV_{SS} DV_{DD} - DV_{SS}	4.75	5.0	5.25	V
Supply Voltage Difference	AV_{DD} - DV_{DD}	–0.1	0.0	0.1	V
Reference Input Voltage (Note 5)	VRB VRT	0 –	0.6 2.6	– 2.8	V
Analog Input Voltage	AIN	VRB	–	VRT	V
Clock High Time Clock Low Time	t_{pwH} t_{pwL}	15 15	– –	– –	ns
Digital Input “L” Voltage Digital Input “H” Voltage	V_{IL} V_{IH}	– 4.0	– –	1.0 –	V
Operating Temperature	T_{opr}	0	–	70	°C

NOTES:

4. It is strongly recommended that all the supply pins (AV_{DD}, DV_{DD}) be powered from the same source.
5. The value of (VRB to VRT) can be moved to the up side (2V to 4V), but characteristics can’t be guaranteed.

STATIC ELECTRICAL CHARACTERISTICS

(Converter Specifications: AV_{DD} = DV_{DD} = 5V, AV_{SS} = DV_{SS} = 0V, Ta = 25°C, VRB = 0.6V, and VRT = 2.6V unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Reference Current	IREF	VRT = 2.6 V, VRB = 0.6 V	5.0	6.7	10	mA
Reference Resistance	RREF	–	200	300	400	Ω
Internal Bias	VRBS VREF	Short VRT and VRTS Short VRB and VRBS	0.55 1.9	0.60 2.0	0.65 2.1	V
Digital Input Low Current	I_{IL}	V_{DD} = 5.25, V_{IL} = V_{SS}	–	–	1	μA
Digital Input High Current	I_{IH}	V_{DD} = 5.25, V_{IH} = V_{DD}	–	–	1	μA
Digital Output Current (Output Enable)	I_{OL} I_{OH}	V_{DD} = 4.75, V_{OL} = 0.4V V_{OH} = V_{DD} - 0.5V OEB = V_{SS}	3.5 –1.1	– –	– –	mA
Digital Output Current (Output High Imp.)	IOZL IOZH	V_{DD} = 5.25, V_{OL} = V_{SS} V_{OH} = V_{DD}, OEB = V_{DD}	– –	– –	16 16	uA
Offset Voltage Error	EOT EOB	V_{EE} = 5.0 VRT = 2.6 V, VRB = 0.6 V	0 0	–25 +20	–68 +40	mV
Difference Linearity Error Integral Linearity Error	ELD ELI	V_{DD} = 5.0 VRT = 2.6 V, VRB = 0.6 V	– –	± 0.6 ± 0.8	± 1.0 ± 1.2	LSB

DYNAMIC CHARACTERISTICS

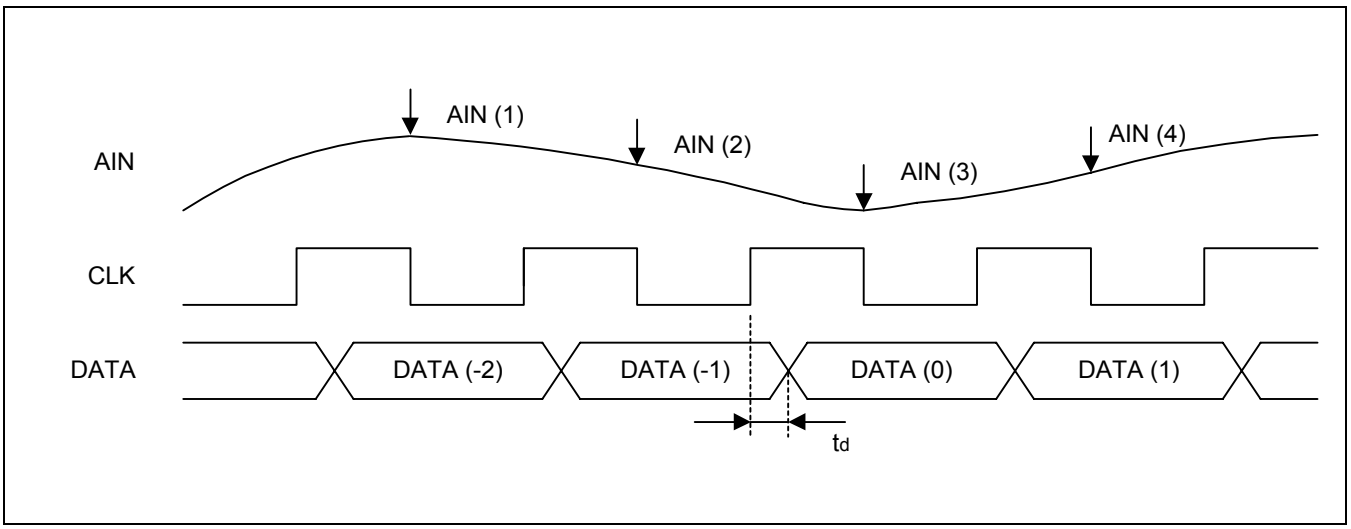
(Converter Specifications: AV_{DD} = DV_{DD} = 5V, AV_{SS} = DV_{SS} = 0V, Ta = 25°C, VRB = 0.6V, and VRT = 2.6V unless otherwise specified.)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Maximum Conversion Rate	fc	AIN = 0.6 to 2.6V 1MHz sine wave	30	–	–	MSPS
Dynamic Supply Current	I_{VDD}	Fs = 20MHz, AIN = NTSC ramp input	–	18	27	mA
Digital Output Data Delay (note 6)	t_d	OEB = V_{SS}	–	18	30	ns
Digital Output Data Delay (Output High Imp.) (Note 7)	t_{disH} t_{disL}	–	– –	– –	100 100	ns
Digital Data Valid Time (note 7)	t_{eneH} t_{eneL}	–	– –	– –	100 100	ns
Signal-to-Noise Ratio	 SNR 1 SNR 2 SNR 3	CK = 20MHz. AIN = 1MHz sine wave 2MHz sine wave 4MHz sine wave	 – – –	 45 45 41	 – – –	 dB dB dB
Differentlal Phase Differentlal Gain	DP DG	NTSC 20 IRE mod Ramp signal, Fs = 14.3MSPS	– –	0.7 1.0	– –	deg %
Sampling Time Offset	t_{sto}	–	–	5	10	ns

NOTES:

6. See “Delay Timing Diagram”
7. See “3-state Output Test Circuit and Timing Diagram”.

DELAY TIMING DIAGRAM



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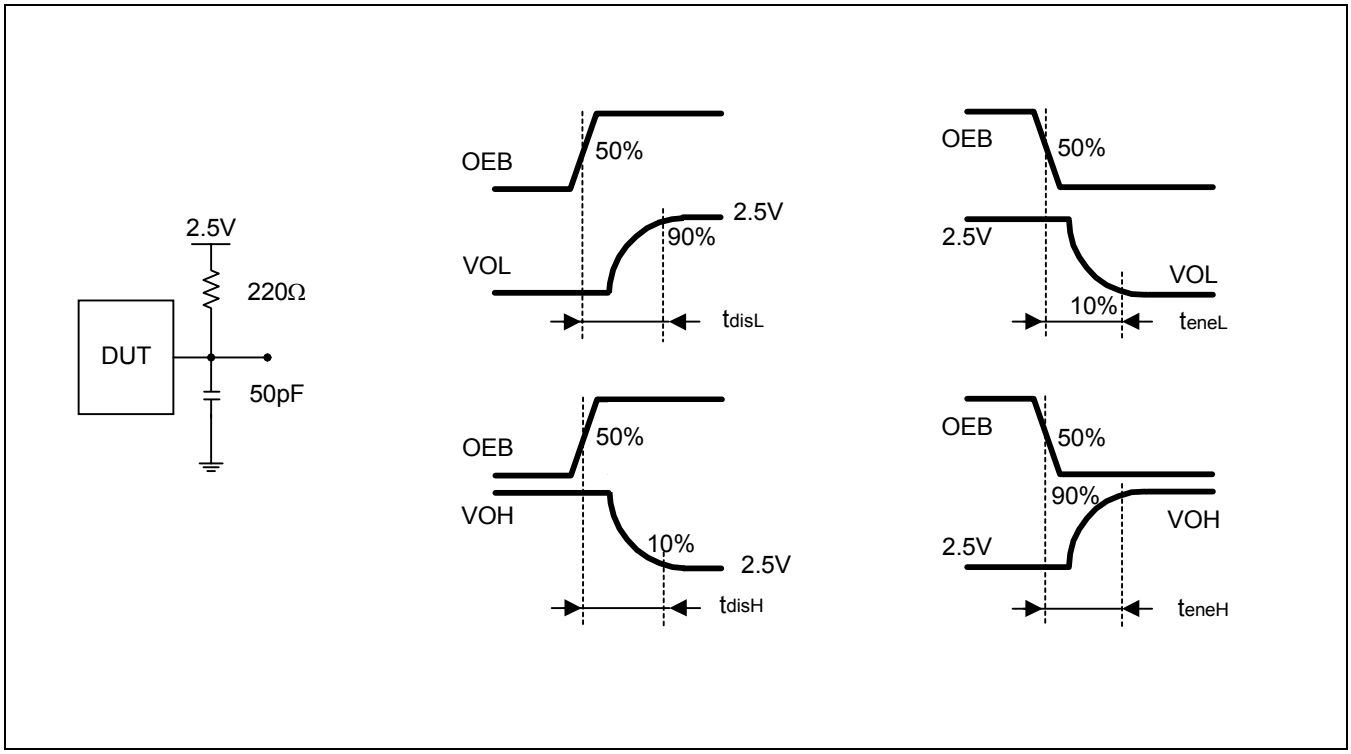
I/O CHART

Index	Analog Input (V)	Digital Output	
0	- 0.6078125	00000000	
1	0.6078125 - 0.6156250	00000001	VRT = 0.6V
2	0.6156250 - 0.6234375	00000010	VRT = 2.6V
…..	…….	…….	
126	1.5921875 - 1.6000000	01111111	1LSB = 7.8125mV
127	1.6000000 - 1.6078125	10000000	
128	1.6078125 - 1.6156250	10000001	
…..	…….	…….	
254	2.5843750 - 2.5921875	11111110	
255	2.5921875 -	11111111	

3-STATE OUTPUT TEST CIRCUIT AND TIMING DIAGRAM



FUNCTION DESCRIPTION

1. KAD0228BD is a two-step ping-pong A/D converter comprising 4-bit coarse ADC and fine ADC of 4.459 bit, approximately. Coarse ADC is composed of 15 auto zero comparators, and fine ADC has 22 sampling amplifier pairs of which the two sampling amplifier operate alternately in a ping-pong manner, and also has 22 analog MUXs and 22 latching comparators.

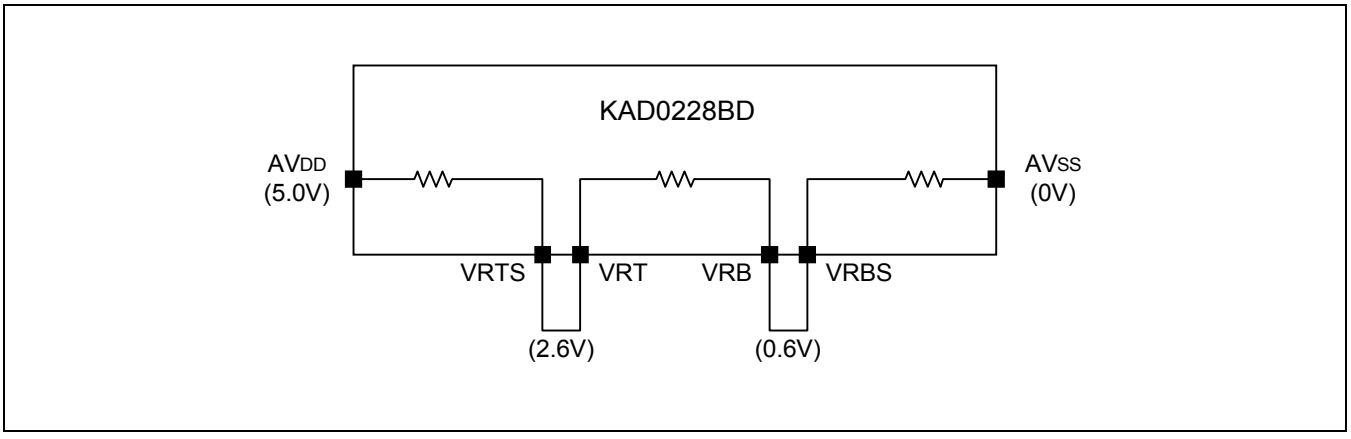
2. Using a CMOS auto zero comparator and switching 1 to 16 different sets of reference voltage to the fine sampling amplifier bank according to the coarse ADC state, the difficulties in implementing high accuracy (more than 8 bits) DAC was eliminated, thus low-power, high-performance, high-speed ADC was achieved. KA0228BD uses an averaging method to reduce the charge injection mismatch in the sampling switches, so the overall differential non-linearity error is enhanced.

3. KAD0228BD operates as follows (see Timing Diagram):
   During the first “H” cycle if external clock the analog input data is sampled and tracked, and the input is held from the falling edge of the CLK (the analog input is abbreviated to AIN in the timing diagram), which is compared with the 16-level coarse reference voltage and latched to result in data CAD. According to the coarse ADC data, the fine reference voltage FRV is set and fed to the fine sampling amplifier bank. This FRV voltage set is compared with the sampled analog input, and resulted in the fine sampling amplifier data. The fine sampling amplifier operates in a ping-pong style to reproduce the analog data with sufficiently large gain, and then MUXed to the latching comparators, Latching comparator bank generates the fine ADC data (FAD), which is used to generate the digital output (DATA) together with the CAD data. The overall pipeline delay is 2.5 clocks.

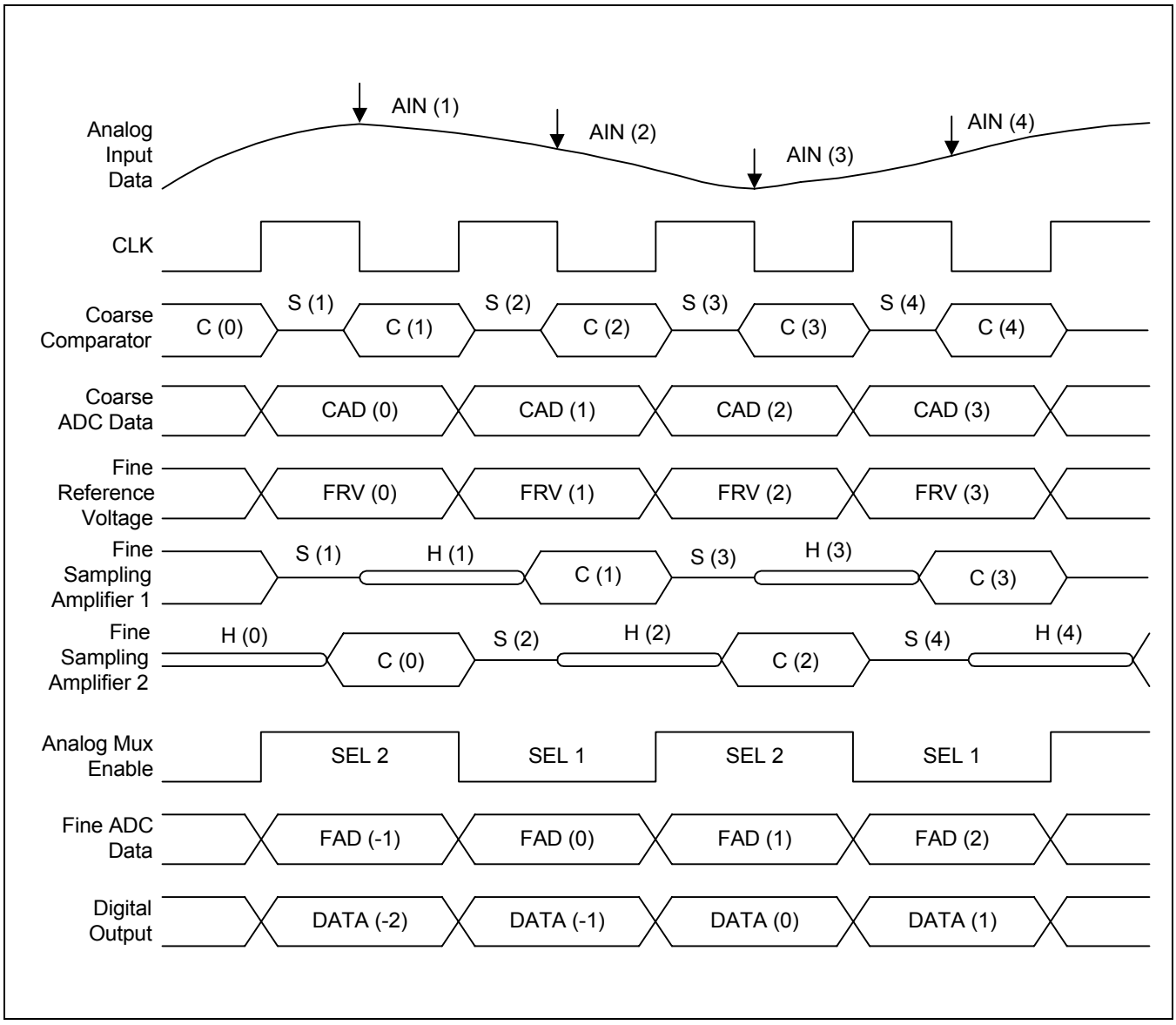
4. KAD0228BD has the correction scheme of the error which comes from the mismatch in the coarse ADC and the fine sampling amplifier offset. This error correction scheme can handle up to 3 LSBs, and hence helps enhance the differential linearity.

5. Inside KAD0228BD, reference resistors are placed between AV_{DD} and VRTS, and between AV_{SS} and VRBS so that VRTS and VRBS generate the 2.6V, and 0.6V reference respectively. In order to utilize the internal self-biased reference voltage, the VRTS pin (16) is to be shorted with VRT pin (17) and the VRBS pin (22) is to be shorted with the VRB pin (23). It is not recommended to take advantage of the self-biased internal reference voltage in case of applying KAD0228BD in a special system which offers high accuracy, though (see reference circuit diagram).

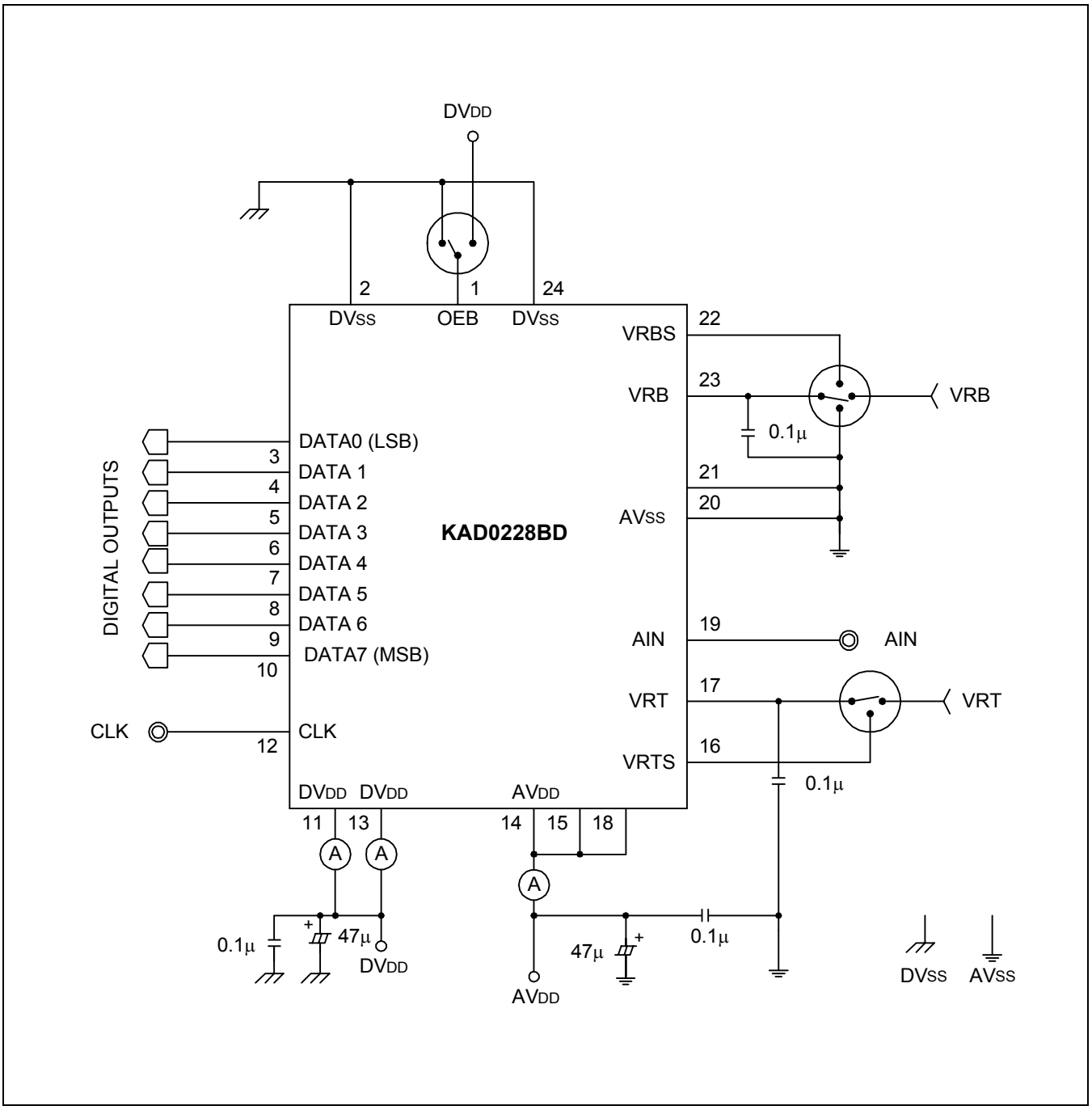
REFERENCE CIRCUIT DIAGRAM



TIMING DIAGRAM

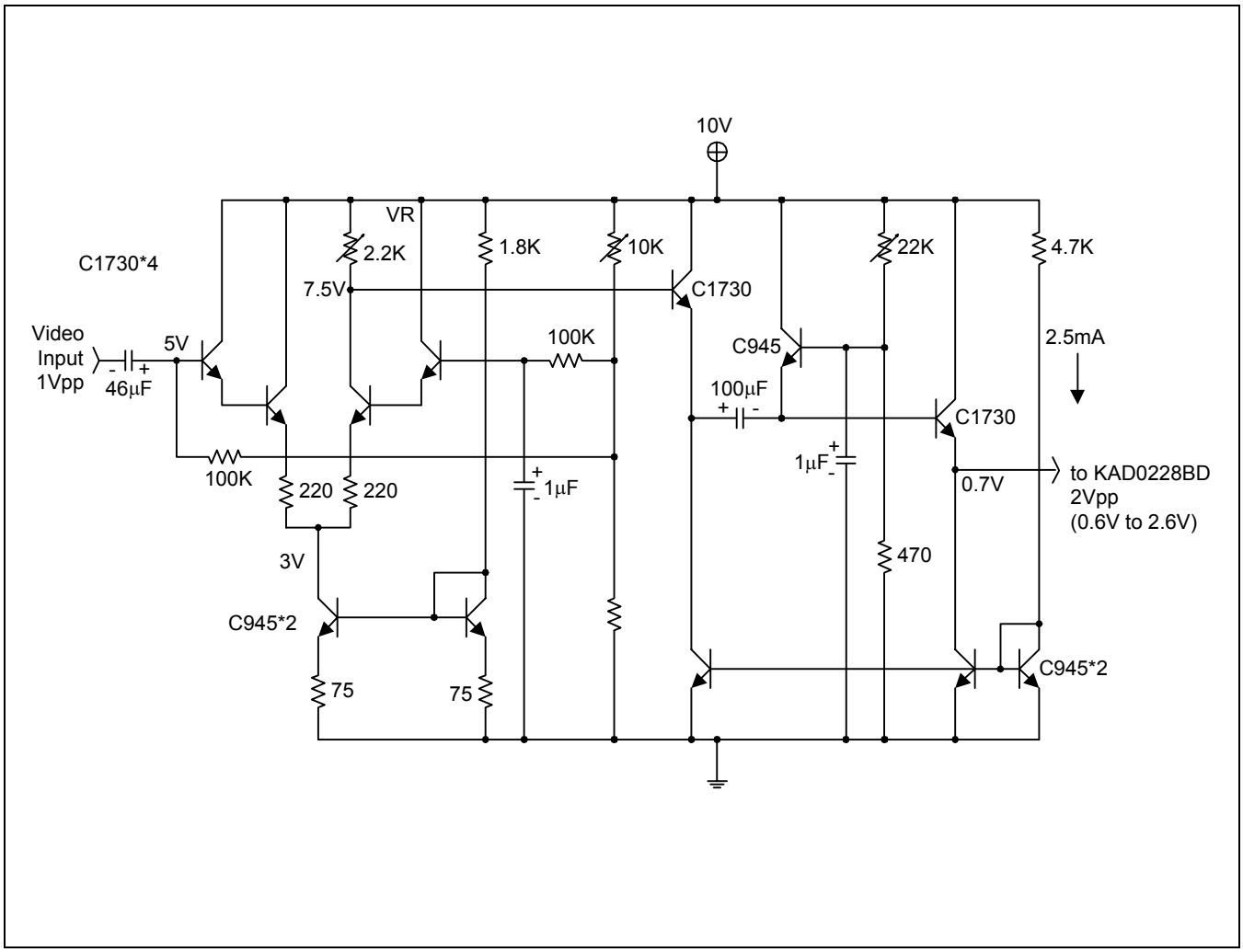


TEST CIRCUIT



NOTE: AV_{DD} and DV_{DD} are needed to be out from common source.
Make the distance between CLK source and CLK DUT pin as short as possible.
Test circuit can be changed because of test equipment and test items.

A/D INPUT AMPLIFIER AND CLAMPING CIRCUIT



PACKAGE DIAGRAM