JUN. 2000

Ver 0.3

DATA SHEET

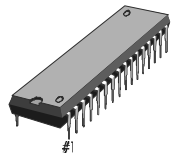
KB2512

Preliminary

SAMSUNG ELECTRONICS

DEFLECTION PROCESSOR

32-SDIP-400



The KB2512 is a monolithic integrated circuit assembled in 32 pins shrunk dual in line plastic package. This IC controls all the functions related to the horizontal and vertical deflection in multi modes or multi-frequency computer display monitors.

The internal sync processor, combined with the very powerful geometry correction block make the KB2512 suitable for very high performance monitors with very few external components. The horizontal jitter level is very low. It is particularly well suited for high-end 17" and 19" monitors.

FUNCTIONS

- Deflection processor
- I^2C bus control
- B+ regulator
- Vertical parabola generator
- Vertical dynamic focus

FEATURES

(HORIZONTAL)

- Self-adaptive
- Dual PLL concept
- 150kHz maximum frequency
- X-RAY protection input
- I^2C controls: Horizontal duty-cycle, H-position, free running frequency, frequency generator for burn-in mode.

(VERTICAL)

- Vertical ramp generator
- 50 to 185Hz AGC loop
- Geometry tracking with V-POS & V-AMP
- I^2C Controls: V-AMP, V-POS, S-CORR, C-CORR
- DC breathing compensation

(I^2C GEOMETRY CORRECTIONS)

- Vertical parabola generator (pincushion-E/W, keystone, corner)

ORDERING INFORMATION

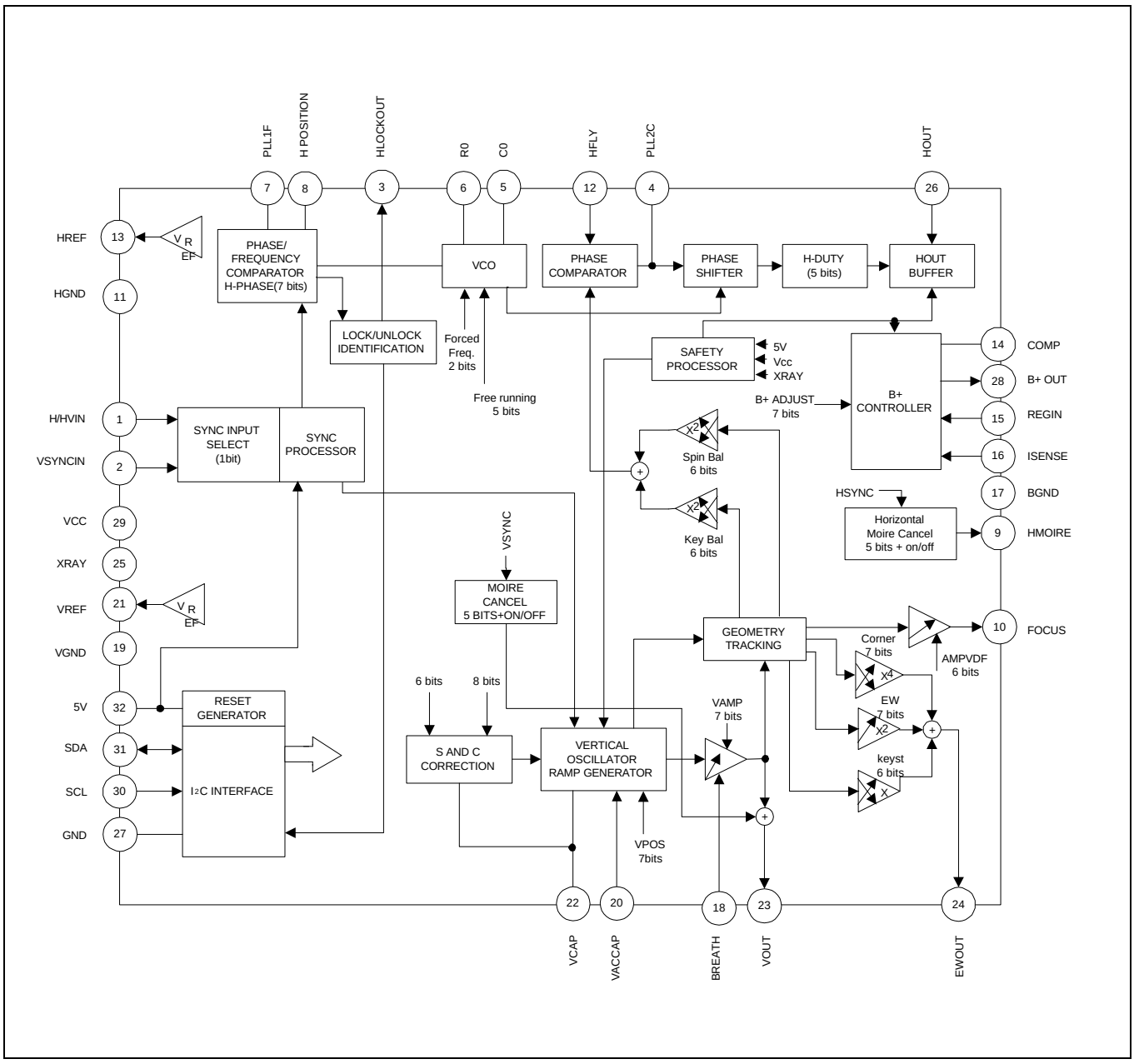
Device	Package	Operating Temperature
KB2512	32-SDIP-400	0 °C ~ 70 °C

- Horizontal dynamic phase (side pin balance & parallelogram)
- Vertical dynamic focus (Vertical focus amplitude)

(GENERAL)

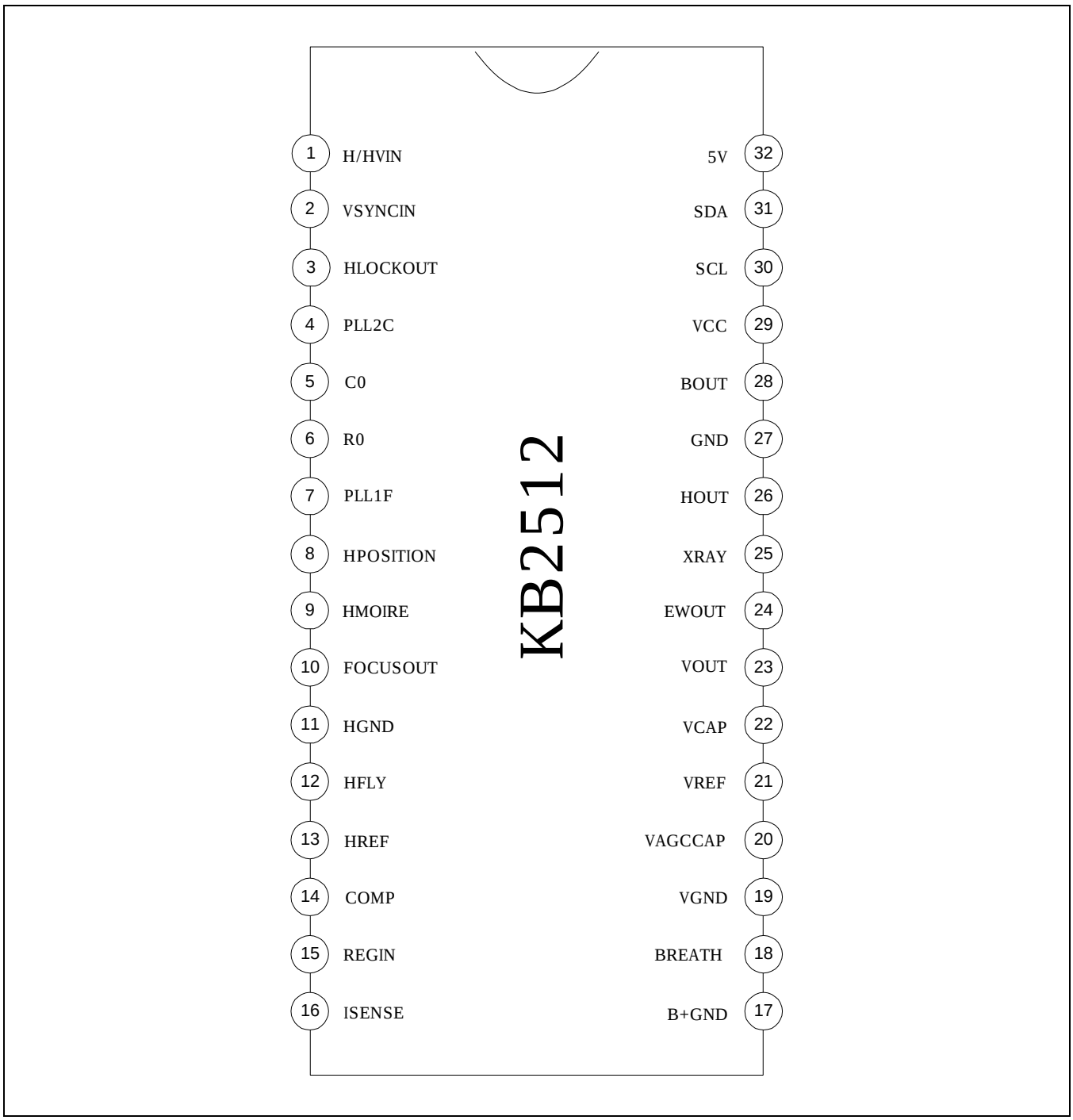
- Sync processor
- 12V supply voltage
- Hor. & Vert. lock/unlock outputs
- Read/Write I^2C interface
- Horizontal and vertical moire
- B+ Regulator
  - Internal PWM generator for B+ current mode step-up converter.
  - I^2C adjustable B+ reference voltage
  - Output pulses synchronized on horizontal frequency
  - Internal maximum current limitation.
  - Soft start
- Compared with the KB2511B, KB2512 HAS:
  - Corner correction
  - Horizontal moire
  - B+ soft start
  - Increased max. Vertical frequency
  - No horizontal focus
  - No step down option for DC/DC converter.

BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATIONS



PIN DESCRIPTION

Table 1. Pin Description

No	Pin Name	Description
1	H/HVIN	TTL compatible horizontal sync input (separate or composite)
2	VSYNCIN	TTL compatible vertical sync input (for separated H&V)
3	HLOCKOUT	First PLL lock/unlock output (0V unlocked - 5V locked)
4	PLL2C	Second PLL loop filter
5	C0	Horizontal oscillator capacitor
6	R0	Horizontal oscillator resistor
7	PLL1F	First PLL loop filter
8	HPOSITION	Horizontal position filter (capacitor to be connected to HGND)
9	HMOIRE	Horizontal moire output (to be connected to PLL2 C through a resistor divider)
10	FOCUSOUT	Vertical dynamic focus output
11	HGND	Horizontal section ground
12	HFLY	Horizontal Flyback input (positive polarity)
13	HREF	Horizontal section reference voltage (to be filtered)
14	COMP	B+ error amplifier output for frequency compensation and gain setting
15	REGIN	Regulation input of B+ control loop
16	ISENSE	Sensing of external B+ switching transistor current
17	B+GND	Ground (related to B+ reference adjustment)
18	BREATH	DC breathing input control (compensation of vertical amplitude against EHV variation)
19	VGND	Vertical section ground
20	VAGCCAP	Memory capacitor for automatic gain control loop in vertical ramp generator
21	VREF	Vertical section reference voltage (to be filtered)
22	VCAP	Vertical sawtooth generator capacitor
23	VOUT	Vertical ramp output (with frequency independent amplitude and S or C corrections if any). It is mixed with vertical position voltage and vertical moire.
24	EWOUT	Pincushion-East/West correction parabola output
25	XRAY	X-RAY protection input (with internal latch function)
26	HOUT	Horizontal drive output (internal transistor, open collector)
27	GND	General ground (referenced to Vcc)
28	BOUT	B+ PWM regulator output
29	Vcc	Supply voltage (12V typ)
30	SCL	I^2C clock input
31	SDA	I^2C data input
32	5V	Supply voltage (5V typ)

REFERENCE DATA

Table 2. Reference Data

Parameter	Value	Unit
Horizontal frequency	15 to 150	kHz
Autosynch frequency (for given R0 and C0)	1 to 4.5FO	FH
± Horizontal sync polarity input	Yes	
Polarity detection (on both horizontal and vertical section)	Yes	
TTL composite sync	Yes	
Lock/unlock identification (on both horizontal 1st PLL and vertical section)	Yes	
I^2C control for H-position	±10	%
XRAY protection	Yes	
I^2C horizontal duty cycle adjust	30 to 60	%
I^2C free running frequency adjustment	0.8 to 1.3FO	FH
Stand-by function	Yes	
Dual polarity H-drive outputs	No	
Supply voltage monitoring	Yes	
PLL1 inhibition possibility	No	
Blanking output	No	
Vertical frequency	35 to 200	Hz
Vertical Autosync (for 150nf on pin22 and 470nf on pin20)	50 to 185	Hz
Vertical S correction	Yes	
Vertical C correction	Yes	
Vertical amplitude adjustment	Yes	
DC breathing control on vertical amplitude	Yes	
Corner correction	Yes	
East/West parabola output (also known as pin cushion output)	Yes	
East/West correction amplitude adjustment	Yes	
Keystone adjustment	Yes	
Vertical position adjustment	Yes	
Internal dynamic horizontal phase control	Yes	
Side pin balance amplitude adjustment	Yes	
Parallelogram adjustment	Yes	
Tracking of geometric corrections with vertical amplitude and position	Yes	
Reference voltage (both on horizontal and vertical)	Yes	

Table 2. Reference Data (Continued)

Parameter	Value	Unit
Vertical dynamic focus	Yes	
I^2C horizontal dynamic focus amplitude adjustment	No	
I^2C horizontal dynamic focus symmetry adjustment	No	
I^2C vertical dynamic focus amplitude adjustment	Yes	
Deflection of input sync type	Yes	
Vertical moire output	Yes	
Horizontal moire output	Yes	
I^2C controlled moire amplitude	Yes	
Frequency generator for burn-in	Yes	
Fast I^2C read/write	400	kHz
B+ regulation adjustable by I^2C	Yes	
B+ soft start	Yes	

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

No	Item	Symbol	Value	Unit
1	Supply voltage (Pin 29)	V_{CC}	13.5	V
2	Supply voltage (Pin 32)	V_{DD}	5.7	V
3	Maximum voltage on Pin 4 Pin 5 Pin 6, 7, 8, 14, 15, 16, 20, 22 Pin 9, 10, 18, 23, 24, 25, 26, 28 Pin 1, 2, 3, 30, 31	V_{IN}	4.0 6.4 8.0 V_{CC} V_{DD}	V V V V V
4	ESD susceptibility Human body model, 100pF discharge through 1.5KΩ EIAJ norm, 200pF discharge through 0Ω	VESD	2 300	kV V
5	Storage temperature	Tstg	- 40, +150	°C
6	Operating temperature	Topr	0, +70	°C

THERMAL CHARACTERISTICS

Table 4. Thermal Characteristics

No	Item	Symbol	Value	Unit
1	Junction temperature	Tj	+150	°C
2	Junction-ambient thermal resistance	θja	65	°C/W

SYNC PROCESSOR

OPERATING CODNITIONS(V_{DD} = 5V, Tamb = 25 °C)

Table 5. Sync Processor Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal sync input voltage	HsVR	Pin 1	0		5	V
Minimum horizontal input pulse duration	MinD	Pin 1	0.7			µs
Maximum horizontal input signal duty cycle	Mduty	Pin 1			25	%
Vertical sync input voltage	VsVR	Pin 2	0		5	V
Minimum vertical sync pulse width	VSW	Pin 2	5			µs
Maximum vertical sync input duty cycle	VSmD	Pin 2			15	%
Maximum vertical sync width on TTL H/V composite	VextM	Pin 1			750	µs
Sink and source current	$I_{HLOCKOUT}$	Pin 3			250	µA

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, Tamb = 25 °C)

Table 6. Sync Processor Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal and vertical input threshold voltage (pin 1, 2)	VINTH	Low level High level	 2.2		0.8	V V
Horizontal and vertical pull-up resister	RIN	Pins 1,2		200		KΩ
Falling and rising output CMOS buffer	TfrOut	Pin 3, Cout = 20pF			200	ns
Horizontal 1st PLL lock output status (pin 3)	VHlock	Locked, $I_{LOCKOUT}$ = -250µA Unlocked, $I_{LOCKOUT}$ = +250µA	 4.4	0 5	0.5	V V
Extracted Vsync integration time (% of TH (see 9)) on H/V composite	VoutT	C0 = 820pF	26	35		%

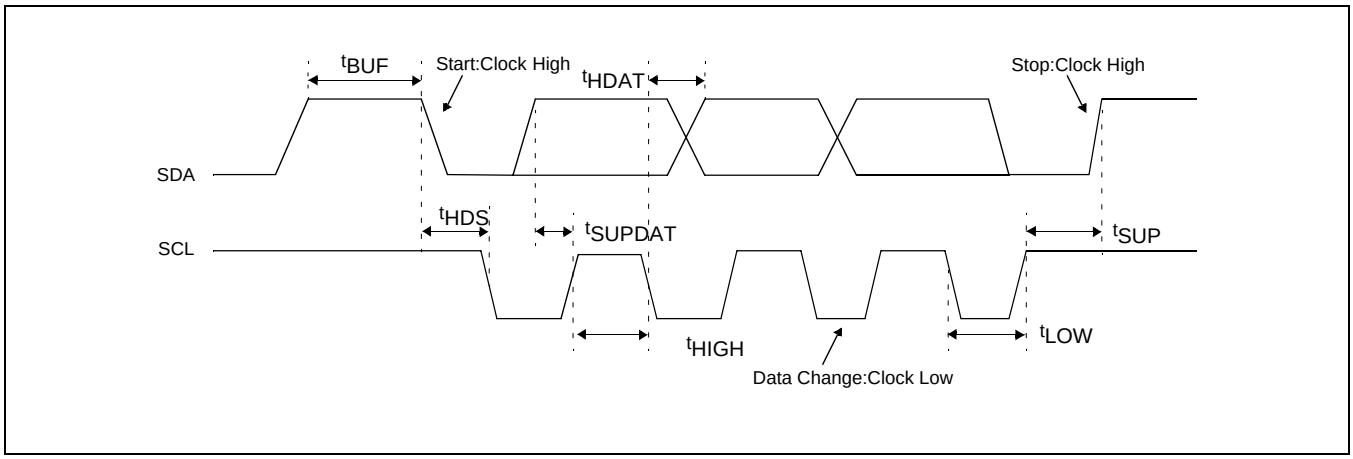
I^2C READ/WRITE (See also I^2C table control and I^2C sub address control)

OPERATING CONDITIONS (V_{DD} = 5V, Tamb = 25 °C)

Table 7. I^2C Read/Write Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input high level voltage	VinH		3.0	-	5.0	V
Input low level voltage	VinL		0	-	1.5	V
Hold time before a new transmission can start	tBUF		1.3	-	-	µs
Hold time for start conditions	tHDS		0.6	-	-	µs
Set-up time for stop conditions	tSUP		0.6	-	-	µs
Hold time data	tHDAT		0.3	-	-	µs
Set-up time data	tSUPDAT		0.25	-	-	µs
Rise time of SCL	tR		-	-	1.0	µs
Fall time of SCL	tF		-	-	3.0	µs
Maximum clock frequency	Fscl	Pin 30			400	kHz
Low period of the SCL clock	Tlow	Pin 30	1.3			µs
High period of the SCL clock	Thigh	Pin 30	0.6			µs
SDA and SCL input threshold	Vinth	Pin 30, 31		2.2		V
Acknowledge output voltage on SDA input with 3mA	VACK	Pin 31			0.4	V

I²C Bus Timing Requirement



HORIZONTAL SECTION

OPERATING CONDITIONS

Table 8. Horizontal Section Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCO						
Minimum oscillator resistor	$Ro_{(Min.)}$	Pin 6	6			KΩ
Minimum oscillator capacitor	$Co_{(Min.)}$	Pin 5	390			pF
Maximum oscillator frequency	$Fo_{(Max.)}$				150	kHz
OUTPUT SECTION						
Maximum input peak current	I12m	Pin 12			5	mA
Horizontal drive output maximum current	HOI	Pin 26, sunk current			30	mA

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Tamb = 25 °C)

Table 9. Horizontal Section Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY AND REFERENCE VOLTAGE						
Supply voltage	Vcc	Pin 29	10.8	12	13.2	V
Supply voltage	V_{DD}	Pin 32	4.5	5	5.5	V
Supply current	I_{CC}	Pin 29		50		mA
Supply current	I_{DD}	Pin 32		5		mA
Horizontal reference voltage	V_{REF-H}	Pin 13, I = -2mA	7.4	8	8.6	V
Vertical reference voltage	V_{REF-V}	Pin 21, I = -2mA	7.4	8	8.6	V

Table 9. Horizontal Section Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Max. sourced current on V_{REF-H}	I_{REF-H}	Pin 13			5	mA
Max. sourced current on V_{REF-V}	I_{REF-V}	Pin 21			5	mA
1st PLL SECTION						
Polarity integration delay	HpolT	Pin 1	0.75			ms
VCO control voltage (pin 7)	V_{VCO}	V_{REF-H} = 8V fo fH (Max.)		 1.3 6.2		 V V
VCO gain (pin 7)	V_{COG}	Ro = 6.49KΩ, Co = 820pF, dF/dV = 1/11RoCo		17		kHz/V
Horizontal phase adjustment (see 11)	Hph	% of horizontal period		±10		%
Horizontal phase setting value (Pin 8) (see 11) Minimum current value Typical value Maximum value	 Hphmin Hphtyp Hphmax	Sub-address 01 Byte x 1111111 Byte x 1000000 Byte x 0000000		 2.8 3.4 4.0		 V V V
PLL1 filter current charge	IPII1U IPII1L	PLL1 is unlocked PLL1 is locked		±140 ±1		µA mA
Free running frequency	fo	Ro = 6.49KΩ, Co = 820pF, fo = 0.97/8RoCo		22.8		kHz
Free running frequency thermal drift (no drift on external components) (see 7)	dF0/dT			-150		ppm/c
Free running frequency adjustment Minimum value Maximum value	 fo(Min.) fo(Max.)	Sub-address 02 Byte x x x 11111 Byte x x x 00000		 0.8 1.3		 Fo Fo
PLL1 capture range	CR	Ro = 6.49KΩ, Co = 820pF, from fo + 0.5kHz to 4.5Fo (fo:22.8kHz) fH (min.) fH (max.)	 100		 23.5	 kHz kHz
Safe forced frequency SF1 Byte 11 x x x x x x SF2 Byte 10 x x x x x x	SFF	Sub-address 02		 2F0 3F0		
2ND PLL SECTION HORIZONTAL OUTPUT SECTION						
Flyback input threshold voltage (pin12)	FBth		0.65	0.75		V
Horizontal jitter	Hjit	At 31.4kHz		70		ppm

Table 9. Horizontal Section Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal drive output duty-cycle (pin 26) (see 1) Low level High level	 HDmin HDmax	Sub-address 00 Byte xxx11111 Byte xxx00000 (see 2)		 30 60		 % %
X-RAY protection input threshold voltage	XRAYth	Pin 25 (see 12)		8		V
Internal clamping levels on 2nd PLL loop filter (pin 4)	Vphi2	Low level High level		1.6 4.0		V V
Threshold voltage to stop H-out, V-out, B-out and XRAY when V_{CC} < VSCinh	VSCinh	Pin 29		7.5		V
Threshold voltage to stop H-out, V-out, B-out and reset XRAY when V_{DD} < VSDinh	VSDinh	Pin 32		4.0		V
Horizontal drive output (low level)	HDvd	Pin 26 I_{OUT} = 30mA			0.4	V
VERTICAL DYNAMIC FOCUS FUNCTION (POSITIVE PARABOLA)						
Bottom DC output level	HDFDC	R_{LOAD} = 10KΩ, Pin 10		2		V
DC output voltage thermal drift (see 17)	TDHDF			200		ppm/C
Vertical dynamic focus parabola amplitude with VAMP and VPOS typical Min. Byte 000000 Typ. Byte 100000 Max. Byte 111111	AMPVDF	Sub-address 0F		 0 0.5 1		 Vpp Vpp Vpp
Parabola amplitude function of VAMP (tracking between VAMP and VDF) with VPOS typ. (Figure 1) (see 3)	VDFAMP	Sub-address 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.6 1 1.5		 Vpp Vpp Vpp
Parabola asymmetry function of VPOS control (tracking between VPOS and VDF) with VAMP Max.	VHDFKeyt	Sub-address 06 Byte x0000000 Byte x1111111		 0.52 0.52		 Vpp Vpp

VERTICAL SECTION

OPERATING CONDITIONS

Table 10. Vertical Section Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUTS SECTION						
Maximum EW output voltage	VEWM	Pin 24			6.5	V
Minimum EW output voltage	VEWm	Pin 24	1.8			V
Minimum load for less than 1% vertical amplitude drift	R_{LOAD}	Pin 20	65			MΩ

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, TAMB = 25 °C)

Table 11. Vertical Section Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VERTICAL RAMP SECTION						
Voltage at ramp bottom point	VRB	V_{REF-V} = 8V, Pin 22		2		V
Voltage at ramp top point (with sync)	VRT	V_{REF-V} = 8V, Pin 22		5		V
Voltage at ramp top point (without sync)	VRTF	Pin 22		VRT-0.1		V
Vertical sawtooth discharge time duration (pin 22)	VSTD	With 150nF cap		70		µs
Vertical free running frequency see (see 4)	VFRF	$C_{OSC\,(pin22)}$=150nF measured on pin 22		100		Hz
AUTO -SYNC frequency (see 13)	ASFR	C_{22}=150nF ± 5%	50		185	Hz
Ramp amplitude drift versus frequency at Maximum vertical amplitude	RAFD	C_{22} = 150nF 50Hz < f < 185Hz		200		ppm/ Hz
Ramp linearity on pin 22 (ΔI22/I22) (see 4)	RIin	2.5 < V_{22} < 4.5V		0.5		%
Vertical position adjustment voltage (pin 23 - V_{OUT} centering)	Vpos	Sub address 06 Byte x0000000 Byte x1000000 Byte x1111111	 3.65	 3.2 3.5 3.8	 3.3 	 V V V
Vertical output voltage (peak-to-peak on pin 23)	VOR	Sub address 05 Byte x0000000 Byte x1000000 Byte x1111111	 3.5	 2.25 3 3.75	 2.5 	 V V V
Vertical output maximum current (pin 23)	VOI			±5		mA

Table 11. Vertical Section Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Max vertical S-correction amplitude (see 14) XOXXXXXX inhibits S-CORR X1111111 gives max S-CORR	dVS	Sub address 07 ΔV/Vpp at TV/4 ΔV/Vpp at 3TV/4		 -4 +4		 % %
Vertical C-Corr amplitude XOXXXXXX inhibits C-corr	Ccorr	Sub address 08 ΔV/Vpp at TV/2 Byte X1000000 Byte X1100000 Byte X1111111		 -3 0 3		 % % %
EAST/WEST FUNCTION						
DC output voltage with typ. Vpos, keystone and corner inhibited	EW_{DC}	pin 24, see figure 2		2.5		V
DC output voltage thermal drift	$TDEW_{DC}$	see note 7		100		ppm/C
Parabola amplitude with max. Vamp, typ. V-Pos, keystone and corner inhibited	EWpara	Sub address 0A Byte 1111111 Byte 1100000 Byte 1000000		 1.7 0.85 0		 Vpp Vpp Vpp
Parabola amplitude function of V-AMP control (tracking between V-AMP and E/W) with typ. Vpos, typ. EW amplitude, keystone and corner inhibited (see 8)	EWtrack	Sub address 05 Byte 1000000 Byte 1100000 Byte 1111111		 0.30 0.55 0.85		 Vpp Vpp Vpp
Keystone adjustment capability with typ.Vpos, corner and E/W inhibited and max. vertical amplitude. (see 8)	KeyAdj	Sub address 09 Byte 1x000000 Byte 1x111111		 0.65 0.65		 Vpp Vpp
Intrinsic keystone function of V-POS control (tracking between V-pos and EW) max. E/W and max. vertical amplitude and corner inhibited. (see 7) A/B ratio B/A ratio	Key-Track	Sub address 06 Byte x0000000 Byte x1111111		 0.52 0.52		
Corner amplitude with max. VAMP, typ. VPOS, keystone and E/W inhibit	Corner	Sub address 0B Byte 11111111 Byte 11000000 Byte 10000000		 1.7 0 -1.7		 Vpp Vpp Vpp
INTERNAL HORIZONTAL DYNAMIC PHASE CONTROL FUNCTION						
Side pin balance parabola amplitude (Figure3) with max. Vamp, typ. V-POS and parallelogram inhibited (see 8, 9)	SPBpara	Sub address 0D Byte x1111111 Byte x1000000		 +1.4 -1.4		 $\%T_H$ $\%T_H$

Table 11. Vertical Section Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Side pin balance parabola amplitude function of Vamp control (tracking between Vamp and SPB) with max. SPB, typ. V-POS and parallelogram inhibited (see 8, 9)	SPBtrack	Sub address 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.5 0.9 1.4		 $\%T_H$ $\%T_H$ $\%T_H$
Parallelogram adjustment capability with max. Vamp, typ. V-POS and max. SPB (see8, 9)	ParAdj	Sub address 0E Byte x1111111 Byte x1000000		 +1.4 -1.4		 $\%T_H$ $\%T_H$
Intrinsic parallelogram function of Vpos control (tracking between V-pos and DHPC) with max. Vamp, max. SPB and parallelogram inhibited (see 8, 9) A/B ratio B/A ratio	Partrack	Sub address 06 Byte x0000000 Byte x1111111		 0.52 0.52		
VERTICAL MOIRE						
Vertical moire (measured on V_{OUT}) pin 23	VMOIRE	Sub address 0C Byte 01x11111		 6		 mV
BREATHING COMPENSATION						
DC breathing control range (see 15)	BRRANG	V18	1		12	V
Vertical output variation versus DC breathing control (Pin 23)	BRADj	V18 ≥ V_{REF-V} V18 = 4V		0 -10		% %

B+ SECTION

OPERATING CONDITIONS

Table 12. B+ Section Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum feedback resistor	FeedRes	Resistor between pins 15 and 14	5			KΩ

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, Tamb = 25 °C)

Table 13. B+ Section Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Error amplifier open loop gain	OLG	At low frequency (see 10)		85		dB
Sunk current on error amplifier output when BOUT is in safety condition	Icomp	Pin 14 (see 12)		0.5		mA
Unity gain band width	UGBW	(see 7)		6		MHz
Regulation input bias current	IRI	Current sourced by pin 15 (PNP base)		0.2		µA
Maximum guaranteed error amplifier output current	EAOI	Current sourced by pin 14 Current sunk by pin 14			0.5 2	mA mA
Current sense input voltage gain	CSG	Pin 16		3		
Max current sense input threshold voltage	MCEth	Pin 16		1.2		V
Current sense input bias current	ISI	Current sourced by pin 16 (PNP base)		1		µA
Maximum external power transistor on time	Tonmax	% of H-period @ fo = 27kHz (see 6)		100		%
B+ output saturation voltage	B+OSV	V_{28} with I_{28} = 10mA		0.25		V
Internal reference voltage	IV_{REF}	On error amp positive input for subaddress 0B Byte 1000000		4.8		V
Internal reference voltage adjustment range	V_{REFADJ}	Byte 111111 Byte 000000		+20 -20		% %
Falling time	t_{FB+}	Pin 28		100		ns

NOTES:

1. Duty cycle is the ratio of power transistor off time period. Power transistor is off when output transistor is off.
2. Initial condition for safe operation start up.
3. S and C correction are inhibited so the output sawtooth has a linear shape.
4. With register 07 at byte x0xxxxxx (s-correction is inhibited) then the S correction is inhibited, and with register 08 at byte x0xxxxxx (C-Correction is inhibited) consequently the sawtooth has a linear shape.
5. These parameters are not tested on each unit. They are measured during our internal qualification.
6. The external power transistor is OFF during 400ns.
7. These parameters are not tested on each unit. They are measured during out internal qualification.
8. Refers to notes 4.
9. TH is the Horizontal period.
10. These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches coming from corners of our processes and also temperature characterization.
11. See Figure 7 for explanation of reference phase.
12. See Figure 11.
13. This is the frequency range for which the vertical oscillator will automatically synchronize, using a single capacitor value on Pin 22 and with a constant ramp amplitude.
14. TV is the vertical period.
15. When not used the DC breathing control pin must be connected to 12V.

CAUTIONS:

The ICS near CDT can be latched up by EHT. Therefore, in order to minimize the impact of the EHT, it is necessary to place ICs far from CDT.

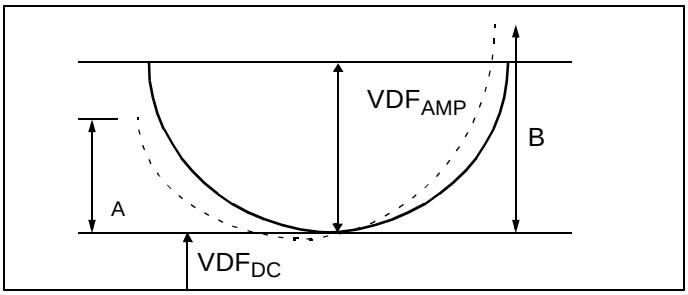


Figure 1. Vertical Dynamic Focus Function

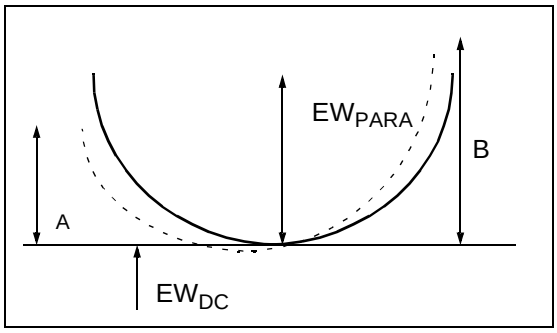


Figure 2. E/W Output

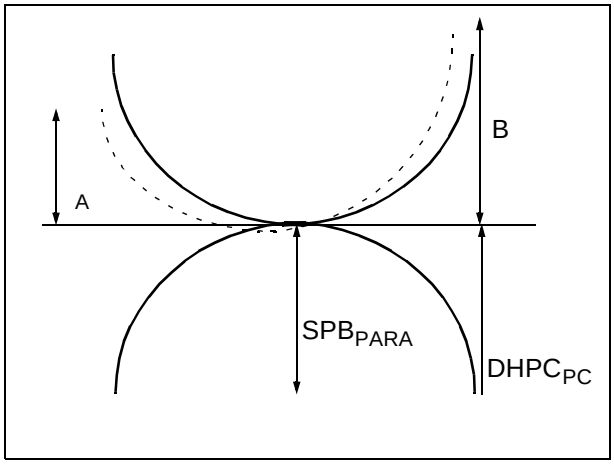


Figure 3. Dynamic Horizontal Phase Control Output

Table 14. Typical Vertical Output Wave forms

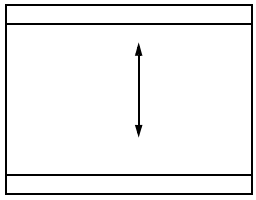
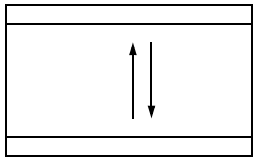
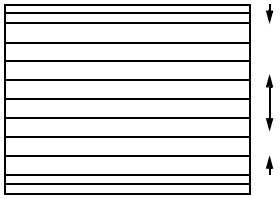
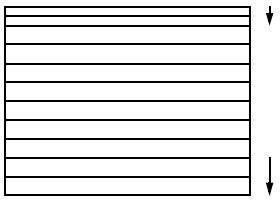
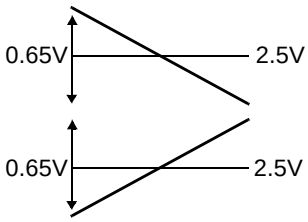
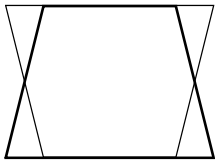
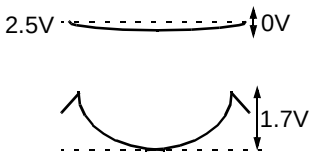
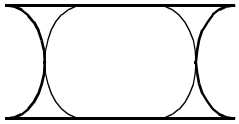
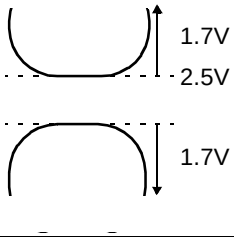
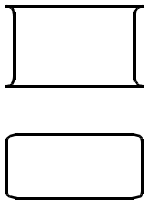
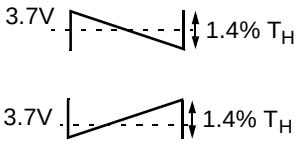
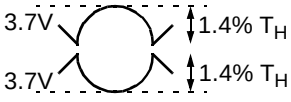
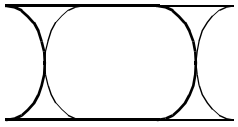
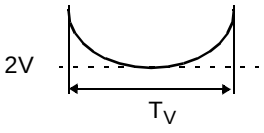
Function	Sub Address	Pin	Byte	Specification	Picture Image
Vertical Size	05	23	10000000 11111111	V_{OUTDC} 2.25V V_{OUTDC} 3.75V	
Vertical Position DC Control	06	23	x0000000 x1000000 x1111111	3.2V 3.5V 3.8V	
Vertical S Linearity	07	23	x0xxxxxx Inhibited x1111111	ΔV, Vpp, $\frac{\Delta V}{Vpp}$=4%	
Vertical C Linearity	08	23	x1000000 x1111111	ΔV, Vpp, $\frac{\Delta V}{Vpp}$=3% ΔV, Vpp, $\frac{\Delta V}{Vpp}$=3%	

Table 15. Geometry Output Wave forms

Function	Sub address	Pin	Byte	Specification	Picture Image
Key stone (trapezoid) control	09	24	E/W + corner inhibited 1x000000 1x111111		
E/W (pin cushion) control	0A	24	Keystone + corner Inhibited 10000000 1111111		
Corner control	0B	24	Keystone + E/W inhibited 11111111 10000000		
Parallelogram control	0E	Internal	SPB Inhibited 1x000000 1x111111		
Side pin balance control	0D	Internal	Parallelogram Inhibited 1x000000 1x111111		
Vertical dynamic focus	OF	10			

I²C BUS ADDRESS TABLE

Slave address (8C): Write mode

Sub address definition

Table 16. I²C Bus Address Table

	D8	D7	D6	D5	D4	D3	D2	D1	
0	0	0	0	0	0	0	0	0	Horizontal drive selection/horizontal duty cycle
1	0	0	0	0	0	0	0	1	Horizontal position
2	0	0	0	0	0	0	1	0	Forced Frequency/free running frequency
3	0	0	0	0	0	0	1	1	Synchro priority/horizontal moire amplitude
4	0	0	0	0	0	1	0	0	Refresh/B+ reference adjustment
5	0	0	0	0	0	1	0	1	Vertical ramp amplitude
6	0	0	0	0	0	1	1	0	Vertical position adjustment
7	0	0	0	0	0	1	1	1	S correction
8	0	0	0	0	1	0	0	0	C correction
9	0	0	0	0	1	0	0	1	E/W keystone
A	0	0	0	0	1	0	1	0	E/W amplitude
B	0	0	0	0	1	0	1	1	E/W corner adjustment
C	0	0	0	0	1	1	0	0	Vertical moire amplitude
D	0	0	0	0	1	1	0	1	Side pin balance
E	0	0	0	0	1	1	1	0	Parallelogram
F	0	0	0	0	1	1	1	1	Vertical dynamic focus amplitude

Slave address (8D): Read mode

No sub address needed

Table 17. I²C Bus Address Table (continued)

	D8	D7	D6	D5	D4	D3	D2	D1
WRITE MODE								
00		HDrive 0: off [1]: on		Horizontal duty cycle				
				[0]	[0]	[0]	[0]	[0]
01	Xray 1: reset [0]	Horizontal phase adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
02	Forced frequency			Free running frequency				
	1: on [0]: off	1: F0x2 [0]: F0x3		[0]	[0]	[0]	[0]	[0]
03	Sync 0: comp [1]: sep	HMoire 1: on [0]		Horizontal moire amplitude				
				[0]	[0]	[0]	[0]	[0]
04	Detect refresh [0]: off			B+ reference adjustment				
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
05	Vramp 0: off [1]: on	Vertical ramp amplitude adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
06		Vertical position adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
07	S Select 1: on [0]		S correction					
			[1]	[0]	[0]	[0]	[0]	[0]
08	C Select 1: on [0]		C correction					
			[1]	[0]	[0]	[0]	[0]	[0]
09	EW key 0: off [1]		East/west keystone					
			[1]	[0]	[0]	[0]	[0]	[0]
0A		East/west amplitude						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0B	E/W cor 0: off [1]	East/west corner adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0C	Test V 1: on [0]: off	Vmoire 1: on [0]		Vertical moire				
				[0]	[0]	[0]	[0]	[0]
0D	SPB sel 0: off [1]		Side pin balance					
			[1]	[0]	[0]	[0]	[0]	[0]
0E	Parallelogram 0: off [1]		Parallelogram					
			[1]	[0]	[0]	[0]	[0]	[0]
0F	Test H 1: on [0]: off		Vertical dynamic focus amplitude					
			[1]	[0]	[0]	[0]	[0]	[0]
READ MODE								
00	Hlock 0: on [1]: no	Vlock 0: on [1]: no	Xray 1: on [0]: off	Polarity detection		Synchro detection		
				H/V pol [1], negative	V pol [1], negative	Vext det [0], no det	H/V det [0], no det	V det [0], no det

[ ] initial value

Set the unspecified bit to [0] in order to assure the compatibility with future devices.

OPERATING DESCRIPTION

GENERAL CONSIDERATIONS

Power Supply

The typical values of the power supply voltages Vcc and V_{DD} are respectively 12V and 5V. Perfect operation is obtained if Vcc and V_{DD} are maintained in the limits: 10.8 to 13.2V and 4.5 to 5.5V.
In order to avoid erratic operation of the circuit during the transient phase of Vcc and V_{DD} switching on, or switching off, the value of Vcc and V_{DD} are monitored and the outputs of the circuit are inhibited if Vcc is less than 7.5V typically.
In the same manner, V_{DD} is monitored and internal set-up is made until V_{DD} reaches 4V (see I^2C control table for power on reset).

In order to have a very good power supply rejection, the circuit is internally powered by several internal voltage references (the typical value is 8V). Two of these voltage references are externally accessible, one for the vertical part and on one for the horizontal one. If needed, these voltage references can be used (until I_{load} is less than 5mA). Furthermore it is necessary to filter the a.m. voltage references by the use of external capacitor connected to ground, in order to minimize the noise and consequently the “jitter” on vertical and horizontal output signals.

I^2C Control

KB2512 belongs to the I^2C controlled device family, instead of being controlled by DC voltage on dedicated control pins, each adjustment can be realized through the I^2C interface. The I^2C bus is a serial bus with a clock and a data input. The general function and the bus protocol are specified in the Phillips-bus data sheets.

The interface (data and clock) is TTL-level compatible. The internal threshold levels of the input comparator are 2.2V on rising edge and 0.8V on falling edge (when V_{DD} is 5V). Spikes of up to 50ns are filtered by an integrator and maximum clock speed is limited to 400kHz.

The data line (SDA) can be used in a bidirectional way that means in read-mode the IC clocks out a reply information (1byte) to the micro-processor.
The bus protocol prescribes always a full-byte transmission. The first byte after the start condition is used to transmit the IC-address (hexa 8C for write, 8D for read).

Write Mode

In write mode the second byte sent contains the sub address of the selected function to adjust (or controls to affect) and the third byte the corresponding data byte. It is possible to send more than one data byte to the IC. If after the third byte no stop or start condition is detected, the circuit increments automatically the momentary sub address in the sub address counter by one (auto-increment mode). So it is possible to transmit immediately the next data bytes without sending the IC address or sub address. It can be useful so as to reinitialize the whole controls very quickly (flash manner). This procedure can be finished by a stop condition.

The circuit has 16 adjustment capabilities: 3 for horizontal part, 4 for vertical one, 2 for E/W correction, 2 for the dynamic horizontal phase control, 1 for moire option, 3 for horizontal and vertical dynamic focus and 1 for B+ reference adjustment.
17 bits are also dedicated to several controls (on/off, horizontal forced frequency, sync priority, detection refresh and XRAY reset).

Read Mode

During read mode the second byte transmits the reply information.
The reply byte contains horizontal and vertical lock/unlock status, the XRAY activated or not, the horizontal and vertical polarity detection. It also contains the Synchro detection status which is used by the MCU to assign sync priority.
A stop condition always stops all the activities of the bus decoder and switches to high impedance both the data and the clock line (SDA and SCL) .
See I^2C sub address and control tables.

Sync processor

The internal sync processor allows the KB2512 to accept any kind of input Synchro signals:

- Separated horizontal & vertical TTL-compatible sync signals,
- Composite horizontal & vertical TTL-compatible sync signals.

Sync identification Status

The MCU can read (address read mode: 8D) the status register via the I^2C bus, and then select the sync priority depending on this status.
Among other data this register indicates the presence of sync pulses on H/HVIN, VSYNCIN and (when 12V is supplied) whether a Vext has been extracted from H/HVIN. Both horizontal and vertical sync are detected even if only 5V is supplied.

In order to choose the right sync priority the MCU may proceed as follows (see I^2C address Table):

- Refresh the status register,
- Wait at least for 20ms(max. vertical period),
- Read this status register,

Sync priority choice should be:

Vext Det	H/V Det	V Det	Sync Priority Subaddress 03 (D8)	Comment Sync Type
No	Yes	Yes	1	Separated H & V
Yes	Yes	No	0	Composite TTL H & V

Of course, when choice is made, one can refresh the sync detections and verify that extracted Vsync is present and that no sync change occurred.
The Sync processor is also giving sync polarity information.

IC status

The IC can inform the MCU about the 1st horizontal PLL and vertical section status, and about the XARY protection (activated or not). Resetting the XRAY internal latch can be done either by decreasing the Vcc supply or directly resetting it via the I^2C interface.

Sync Inputs

Both H/HVin and Vsyncin inputs are TTL compatible trigger with Hysteresis to avoid erratic detection.
Both inputs include a pull up register connected to V_{DD}.

Sync Processor Output

The sync processor indicates on the HLOCKOUT Pin whether 1st PLL is locked to an incoming horizontal sync. HLOCKOUT is a TTL compatible CMOS output. Its level goes to high when locked. In the same time the D8 bit of the status register is set to 0. This information is mainly used to trigger safety procedures (like reducing B+ value) as soon as a change is detected on the incoming sync. Further to this, it may be used in an automatic procedure for free running frequency(fo) adjustment.

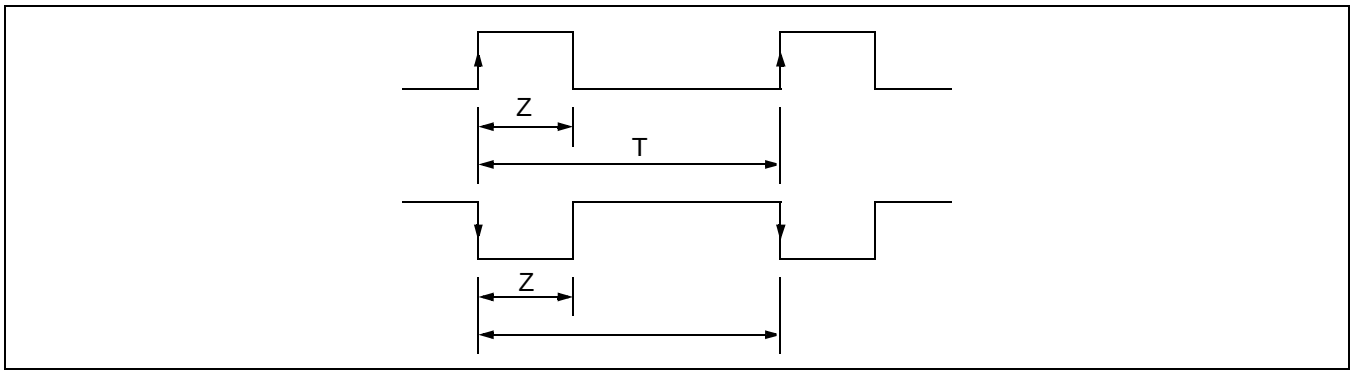
Sending the desired fo on the sync input and progressively decreasing the free running frequently I^2C register value (address 02), the HLOCKOUT Pin will go high as soon as the proper setting is reached. Setting the free running frequency this way allows to fully exploit the KB2512 horizontal frequency range.

HORIZONTAL PART

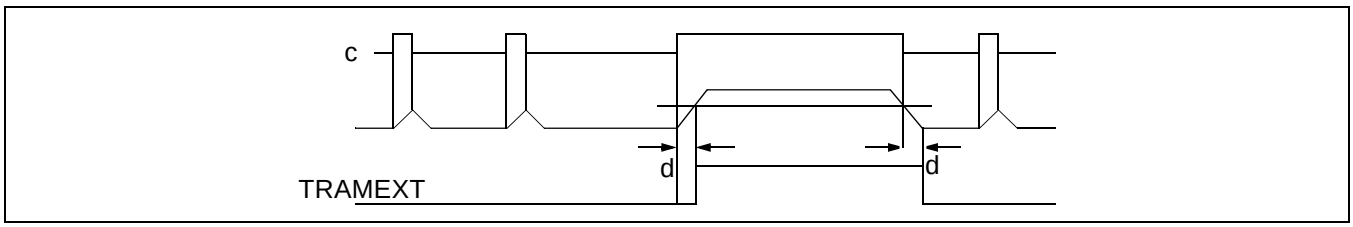
Internal input conditions

Horizontal part is internally fed by Synchro processor with a digital signal corresponding to horizontal Synchro pulses or to TTL composite input.
concerning the duty cycle of the input signal, the following signals (positive or negative) may be applied to the circuit.

Using internal integration, both signals are recognized on condition that Z/T < 25%, Synchronization occurs on the leading edge of the internal sync signal. The minimum value of Z is 0.7µs.



An other integration is able to extract vertical pulse of composite Synchro if duty cycle is more than 25% (typically d = 35%) (see 7)



The last feature performed is the equalizing pulses removing to avoid parasitic pulse on phase comparator input which is intolerant to wrong or missing pulse.

PLL1

The PLL1 is composed of a phase comparator, an external filter and a voltage control oscillator (VCO).
The phase comparator is a phase frequency type designed in CMOS technology. This kind of phase detector avoids locking on false frequencies. It is followed by a charge pump, composed of two current sources sunk and sourced (I = 1mA typ. when locked, I = 140µA when unlocked). This difference between lock/unlock permits a smooth catching of horizontal frequency by PLL1. This effect is reinforced by an internal original slow down system when PLL1 is locked avoiding horizontal too fast frequency change.

The dynamic behavior of the PLL is fixed by an external filter which integrates the current of the charge pump. A CRC filter is generally used (see Figure 4)

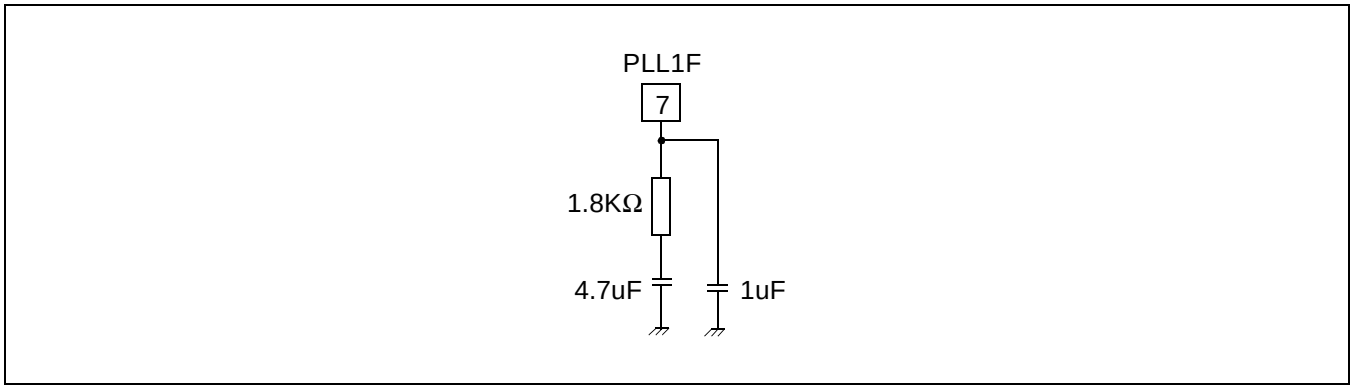


Figure 4. PLL1

PLL1 is internally inhibited during extracted vertical sync (if any) to avoid taking in account missing pulses or wrong pulse on phase comparator. The inhibition results from the opening of a switch located between the charge pump and the filter (see Figure 5).

The VCO uses an external RC network. It delivers a linear sawtooth obtained by charge and discharge of the capacitor, by a current proportional to the current in the resistor. Typical thresholds of sawtooth are 1.6V and 6.4V.

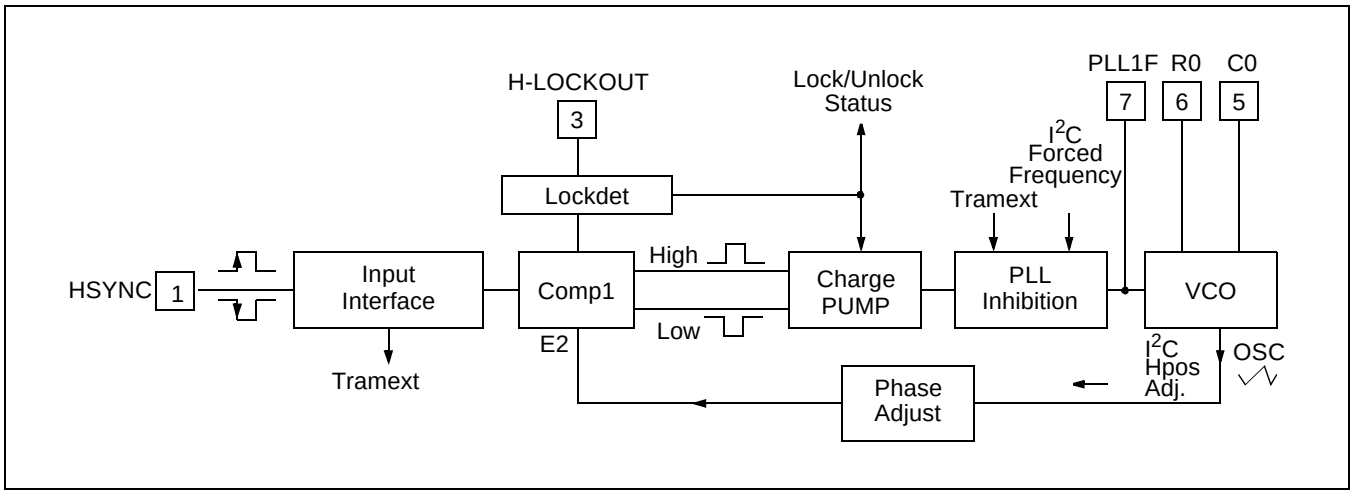


Figure 5. Block Diagram

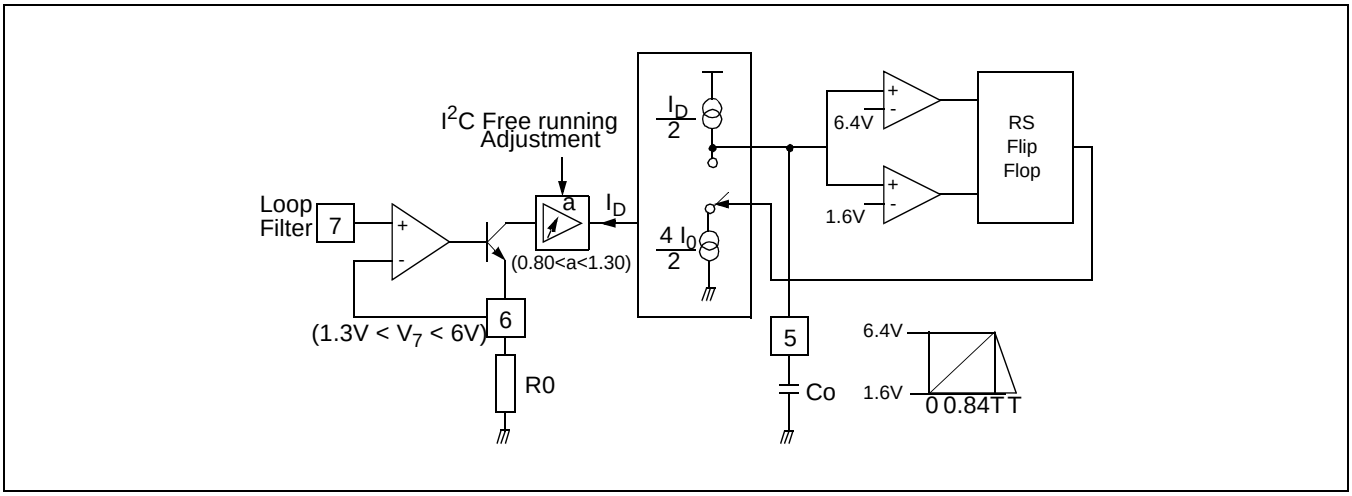
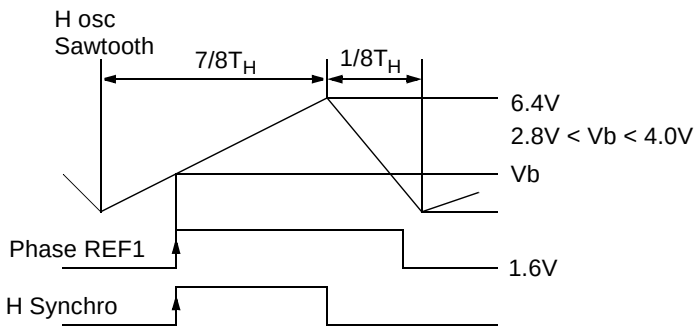


Figure 6. Details of VCO

The control voltage of the VCO is typically comprised between 1.33V and 6V (see figure 6). The theoretical frequency range of this VCO is in the ratio 1 to 4.5, the effective frequency range has to be smaller 1 to 4.2 due to clamp intervention on filter lowest value. To avoid spread of external components and the circuit itself, it is possible to adjust free running frequency through I^2C. This adjustment can be made automatically on the manufacturing line without manual operation by using lock/unlock information. The adjustment range is 0.8 to 1.3 F0 (where 1.3 F0 is the free running frequency at power on reset).

The sync frequency has to be always higher than the free running frequency. As an example for a Synchro range from 24kHz to 100kHz, the suggested free running frequency is 23kHz.
Another feature is the capability for MCU to force horizontal frequency throw I^2C to 2xF0 or 3xF0 (for burn in mode or safety requirement). In this case, inhibition switch is opened leaving PLL1 free but voltage on PLL1 filter is forced to 2.66V for 2xF0 or 4.0V for 3xF0.

The PLL1 ensures the coincidence between the leading edge of the Synchro signal and a phase reference obtained by comparison between the sawtooth of the VCO and an internal DC voltage I^2C adjustable between 2.8V and 4.0V (corresponding to ±10%) (see Figure 7)



Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.8V and 4.0V. The PLL1 ensures the exact coincidence between the signals phase REF and Hsyns. A $\pm T_H/10$ phase adjustment is possible

Figure 7. PLL1 Timing Diagram

The KB2512 also includes a lock/unlock identification block which senses in real time whether PLL1 is locked or not on the incoming horizontal sync signal. The resulting information is available on Hlockout (see sync processor). The block function is described in figure 5.
When PLL1 is unlocked, It forces Hlockout to leave high.
The lock/unlock information is also available throw I^2C read.

PLL2

The PLL2 ensures a constant position of the shaped Flyback signal in comparison with the sawtooth of the VCO (Figure 8). The phase comparator of PLL2 (phase type comparator) is followed by a charge pump (typical output current:0.5mA). The Flyback input is composed of an NPN transistor. This input must be current driven. The maximum recommended input current is 5mA (see Figure 9).

The duty cycle is adjustable through I^2C from 30% to 60%. For start up safe operation, initial duty cycle (after power on reset) is 60% in order to avoid having a too long conduction period of the horizontal scanning transistor. The maximum storage time (Ts max.) is ($0.44T_H$-T_{FLY}/2). Typically, T_{FLY}/TH is around 20% which means that Ts max is around 34% of T_H.

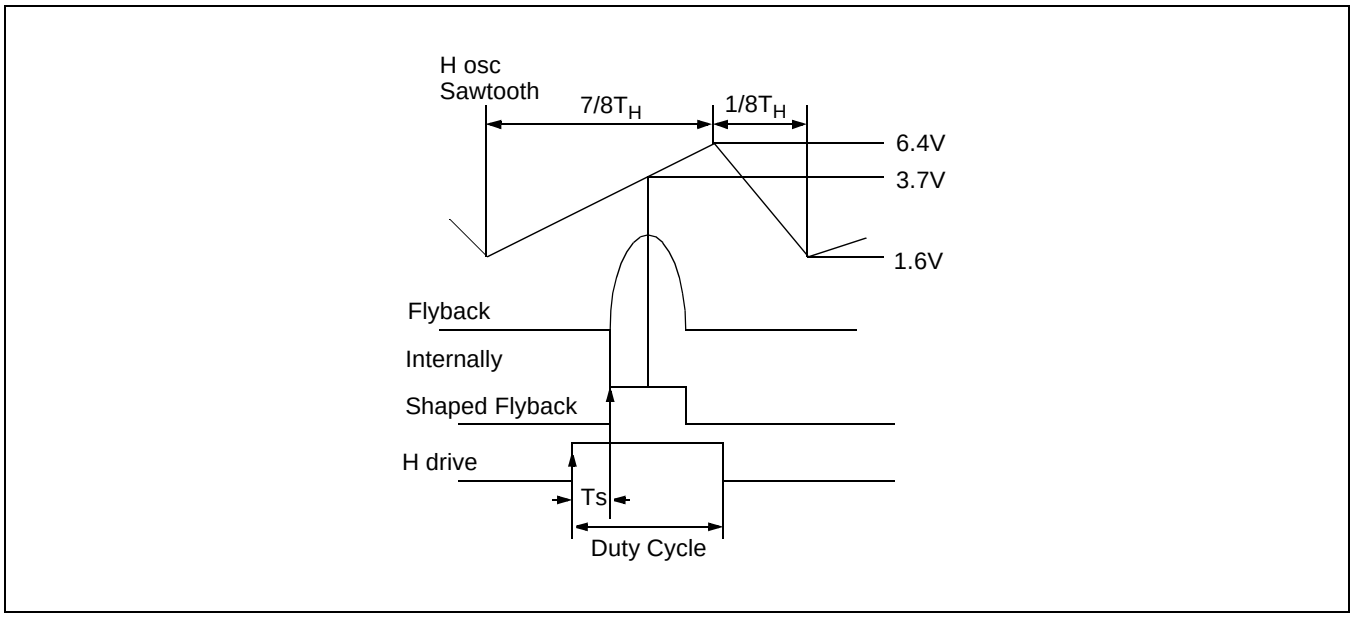


Figure 8. PLL2 Timing Diagram

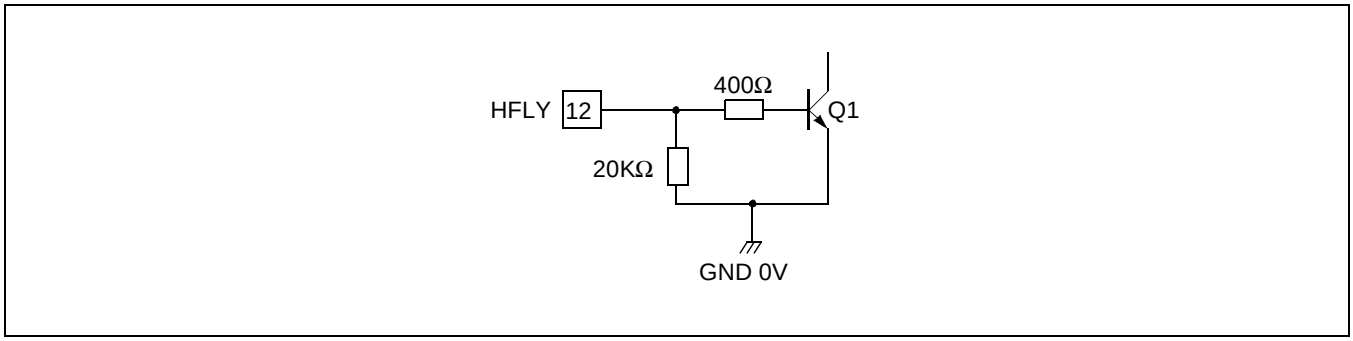


Figure 9. Flyback Input Electrical Diagram

Output Section

The H-drive signal is transmitted to the output through a shaping block ensuring TS and I^2C adjustable duty cycle. In order to secure scanning power part operation, the output is inhibited in the following circumstances:

- Vcc and V_{DD} too low
- XRAY protection activated
- During horizontal Flyback
- H Drive I^2C bit control is off.

The output stage is composed of a NPN bipolar transistor. Only the collector is accessible (see Figure 10).

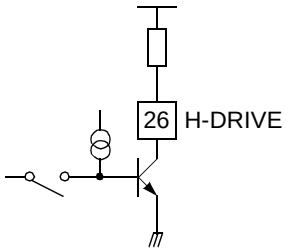


Figure 10. Output Section

The output NPN is in off-state when the power scanning transistor is also in off-state.
The maximum output current is 30mA, and the corresponding voltage drop of the output V_{CEsat} is 0.4V Max.
It is evident that the power scanning transistor cannot be directly driven by the integrated circuit. An interface has to be designed between the circuit and the power transistor which can be of bipolar or MOS type.

X-RAY Protection

The activation of the X-ray protection is obtained by application of a high level on the X-ray input (8V on pin 25). It inhibits the H-drive and B+ outputs.
This protection is latched; It may be reset either by Vcc or V_{DD} switch off or by I^2C (see Figure 11).

Vertical Dynamic Focus

The KB2512 delivers a vertical parabola wave from on pin 10. Vertical dynamic focus is tracked with VPOS and VAMP. Its amplitude can be adjusted. It is also affected by S and C corrections. This positive signal once amplified has to be connected to the CRT focusing grids.

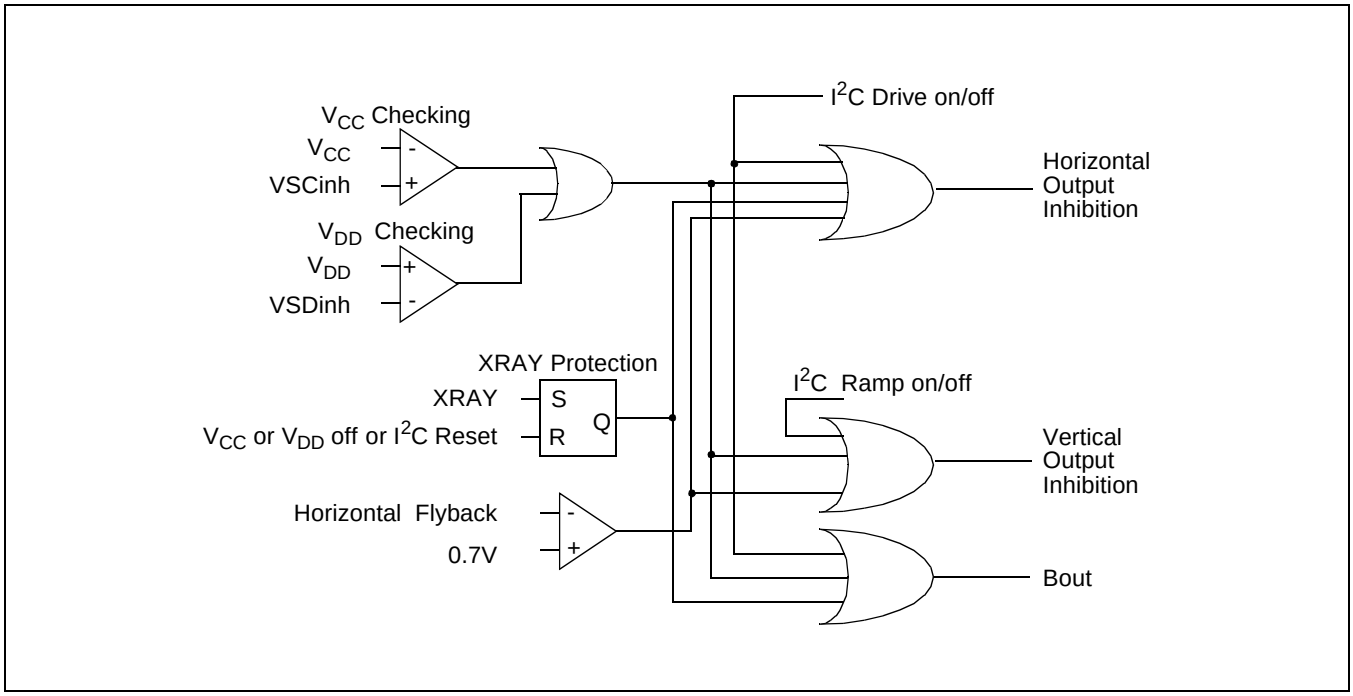


Figure 11. Safety Functions Block Diagram

VERTICAL PART

Geometric Corrections

The principle is represented in Figure 12.

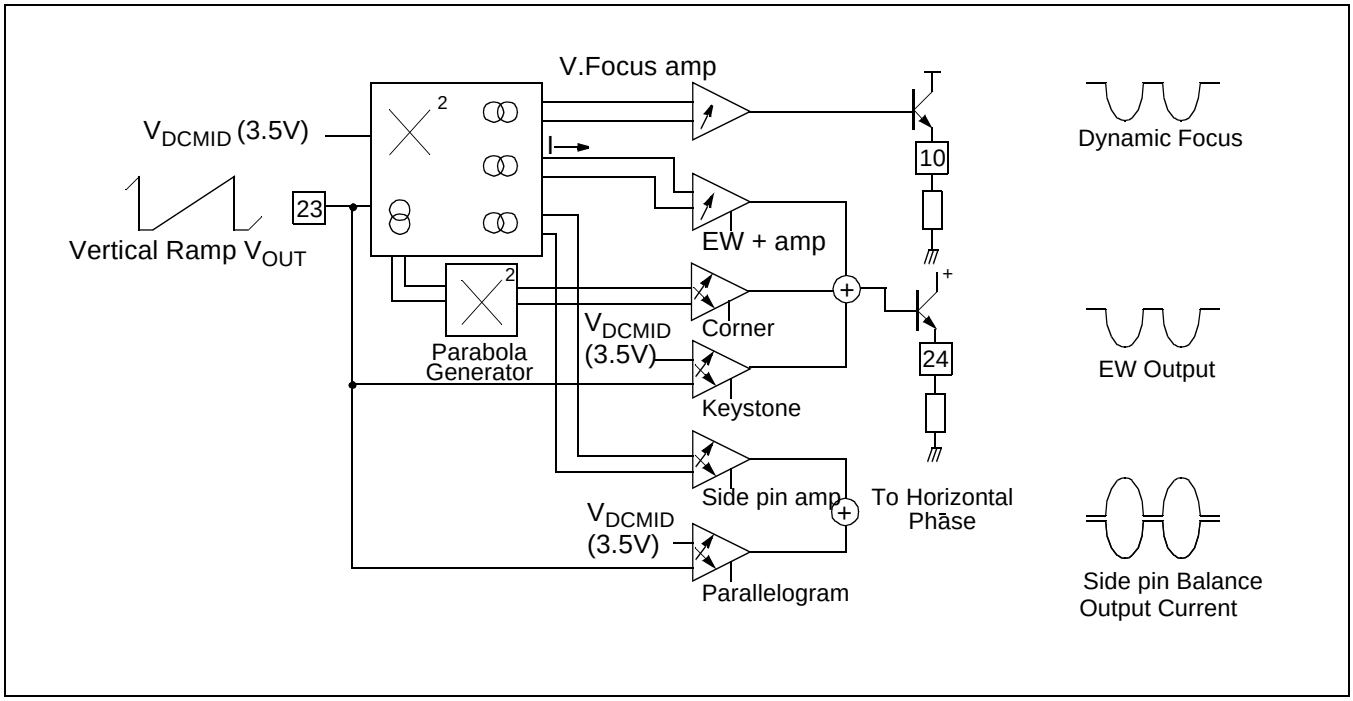


Figure 12. Geometric Corrections Principle

Starting from the vertical ramp, a parabola shaped current is generated for E/W correction, dynamic horizontal phase control correction, and vertical dynamic focus correction.
The base of the parabola generator is an analog multiplier, the output current of which is equal to:

$\Delta I = k \times (V_{OUT} - V_{DCMID})^2$

Where Vout is the vertical output ramp (typically between 2 and 5V) and V_{DCMID} is 3.5V (for V_{REF-V} = 8V). One more multiplier provides a current proportional to $(Vout - V_{DCMID})^4$ for corner correction The VOUT sawtooth is typically centered on 3.5V. By changing the vertical position, the sawtooth shifts by ±0.3V.
In order to keep a good screen geometry for any end user preference adjustment we implemented the geometry tracking.

Due to large output stages voltage range (E/W, keystone corner), the combination of tracking function with maximum vertical amplitude max or min vertical position and maximum gain on the DAC control may lead to the output stages saturation. This must be avoided by limiting the output voltage by appropriate I^2C registers values.
For E/W part and dynamic horizontal phase control part, a sawtooth shaped differential current in the following form is generated:

$\Delta I' = k' \times (V_{OUT} - V_{DCMID})^2$

Then ΔI and ΔI'are added together and converted into voltage for the E/W part.
Each of the three E/W components and the two dynamic horizontal phase control ones may be inhibited by their own I^2C select bit.
The E/W parabola is available on pin 24 by the way of an emitter follower which has to be biased by an external resistor (10KΩ). It can be DC coupled with external circuitry.

The vertical dynamic focus is available on output pin 10. Dynamic horizontal phase control current drives internally the H-position, moving the Hfly position on the horizontal sawtooth in the ± 1.4% The both on side pin balance and parallelogram.

EW

$EWOUT = 2.5V + K1 (V_{OUT} - V_{DCMID}) + K2 (V_{OUT} - V_{DCMID})^2 + K3 (Vout - V_{DCMID})^4$
K1 is adjustable by the keystone I^2C register
K2 is adjustable by the EW amplitude I^2C register
K3 is adjustable by the corner I^2C register

Dynamic Horizontal Phase Control

$IOUT = K4 (V_{OUT} - V_{DCMID})^2 + K5 (V_{OUT} - V_{DCMID})$
K4 is adjustable by side pin balance I^2C register
K5 is adjustable by parallelogram I^2C register.

Function

When the Synchronization pulse is not present, an internal current source sets the free running frequency. For an external capacitor, C_{OSC} = 150nF, the typical free running frequency is 100Hz.
Typical free running frequency can be calculated by:

$$fo(Hz) = 1.5 \cdot 10^{-5} \cdot \frac{1}{C_{OSC}}$$

A negative or positive TTL level pulse applied on pin 2 (VSYNC) as well as a TTL composite sync on pin 1 can Synchronize the ramp in the range [fmin, fmax]. This frequency range depends on the external capacitor connected on pin 22. A capacitor in the range [150nF, ± 5%] is recommended for application in the following range: 50Hz to 185Hz.
Typical maximum and minimum frequency, at 25°C and without any correction (S correction or C correction), can be calculated by:

$f_{(Max.)} = 3.5 \times fo$ and $f_{(Min.)} = 0.33 \times fo$

If S or C corrections are applied, these values are slightly affected.
If a Synchronization pulse is applied, the internal oscillator is Automatically caught but the amplitude is no more constant. An internal correction is activated to adjust it in less than a half a second: the highest voltage of the ramp pin 22 is sampled on the sampling capacitor connected on pin 20 at each clock pulse and a transconductance amplifier generates the charge current of the capacitor. The ramp amplitude becomes again constant.

The read status register enables to have the vertical lock-unlock and the vertical sync polarity informations.
It is recommended to use a AGC capacitor with low leakage current. A value lower than 100nA is mandatory.
A good stability of the internal closed loop is reached by a 470nF ± 5% capacitor value on pin 20 (VAGC)

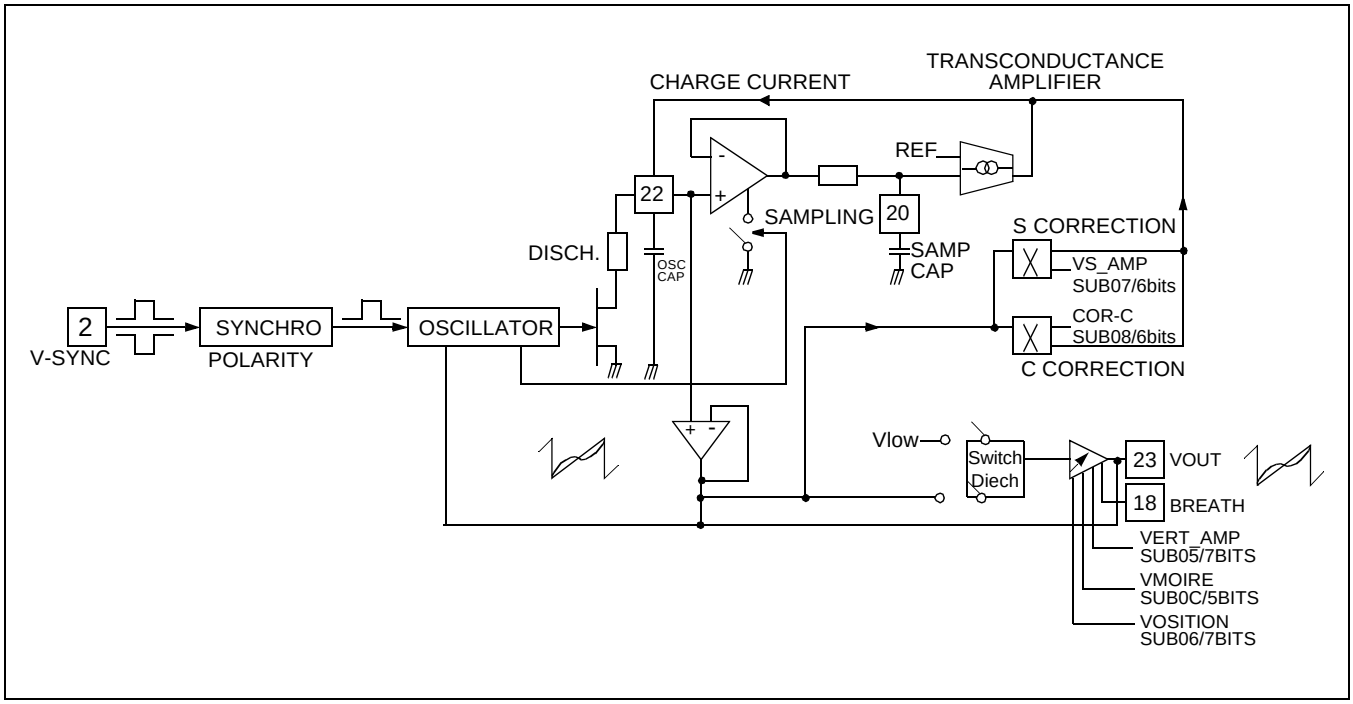


Figure 13. AGC Loop Block Diagram

I²C Control Adjustments

Then, S and C correction shapes can be added to this ramp. This frequency independent S and C corrections are generated internally. Their amplitude are adjustable by their respective I²C register. They can also be inhibited by their select bit. The amplitude of this S and C corrected ramp can be adjusted by the vertical ramp amplitude control register. The adjusted ramp is available on pin 23 (VOUT) to drive an external power stage. The gain of this stage is typically 25% depending on its register value. The mean value of this ramp is driven by its own I²C register (vertical position). Its value is VPOS = 7/16 • V_{REF} ± 300mV.
Usually VOUT is sent through a resistive divider to the inverting input of the booster. Since VPOS derives from V_{REF-V}, the bias voltage sent to the non-inverting input of booster should also derive from V_{REF-V} to optimize the accuracy (see application diagram).

Basic Equations

In first approximation, the amplitude of the ramp on pin 23 (Vout) is:
V_{OUT} - VPOS = (V_{OSC} - V_{DCMID}) • (1 + 0.25 (V_{AMP}))
with:

- V_{DCMID} = 7/16•V_{REF} (typically 3.5V, the middle value of the ramp on pin 22)
- V_{OSC} = V22 (ramp with fixed amplitude)
- VAMP = - 1 for minimum vertical amplitude register value and +1 for maximum
- VPOS is calculated by: VPOS = V_{DCMID} + 0.3Vp with Vp equals -1 for minimum vertical position register value and +1 for maximum

The current available on pin 22 is:

$$I_{OSC} = \frac{3}{8} \bullet V_{REF} \bullet C_{OSC} \bullet f$$

with C_{OSC}: capacitor connected on pin 22
f: synchronization frequency.

Vertical Moire

By using the vertical moire, VPOS can be modulated from frame to frame. This function is intended to cancel the fringes which appear when line to line interval is very close to the CRT vertical pitch. The amplitude of the modulation is controlled by register VMOIRE on address OC and can be switched - off via the control bit D7.

DC/DC CONVERTER PART

This unit controls the switch-mode DC/DC converter. It converts a DC constant voltage into the B+ voltage(roughly proportional to the horizontal frequency) necessary for the horizontal scanning. This DC/DC converter must be configured in step-up mode. It operates very similarly to the well known UC3842.

Step-up Mode

Operating description

- The power MOS is switched-on at the middle of the horizontal Flyback.
- The power MOS is switched-off when its current reaches predetermined value. For this purpose, a sense resistor is inserted in its source. The voltage on this resistor is sent to pin16 (I_{SENSE}).
- The feedback (coming either from the EHV or from the Flyback) is divided to a voltage close to 4.8V and compared to the internal 4.8V reference (I_{VREF}). The difference is amplified by an error amplifier, the output of which controls the power MOS switch-off current.

Main Features

- Switching synchronized on the horizontal frequency
- B+ voltage always higher than the DC source
- Current limited on a pulse-by-pulse basis
- The DC/DC converter is disabled:
  - When V_{CC} or V_{DD} are too low,
  - When X-Ray protection is latched,
  - Directly through I^2C bus.
- When disabled, BOUT is driven to GND by a 0.5mA current source. This feature allows to implement externally a soft start circuit.

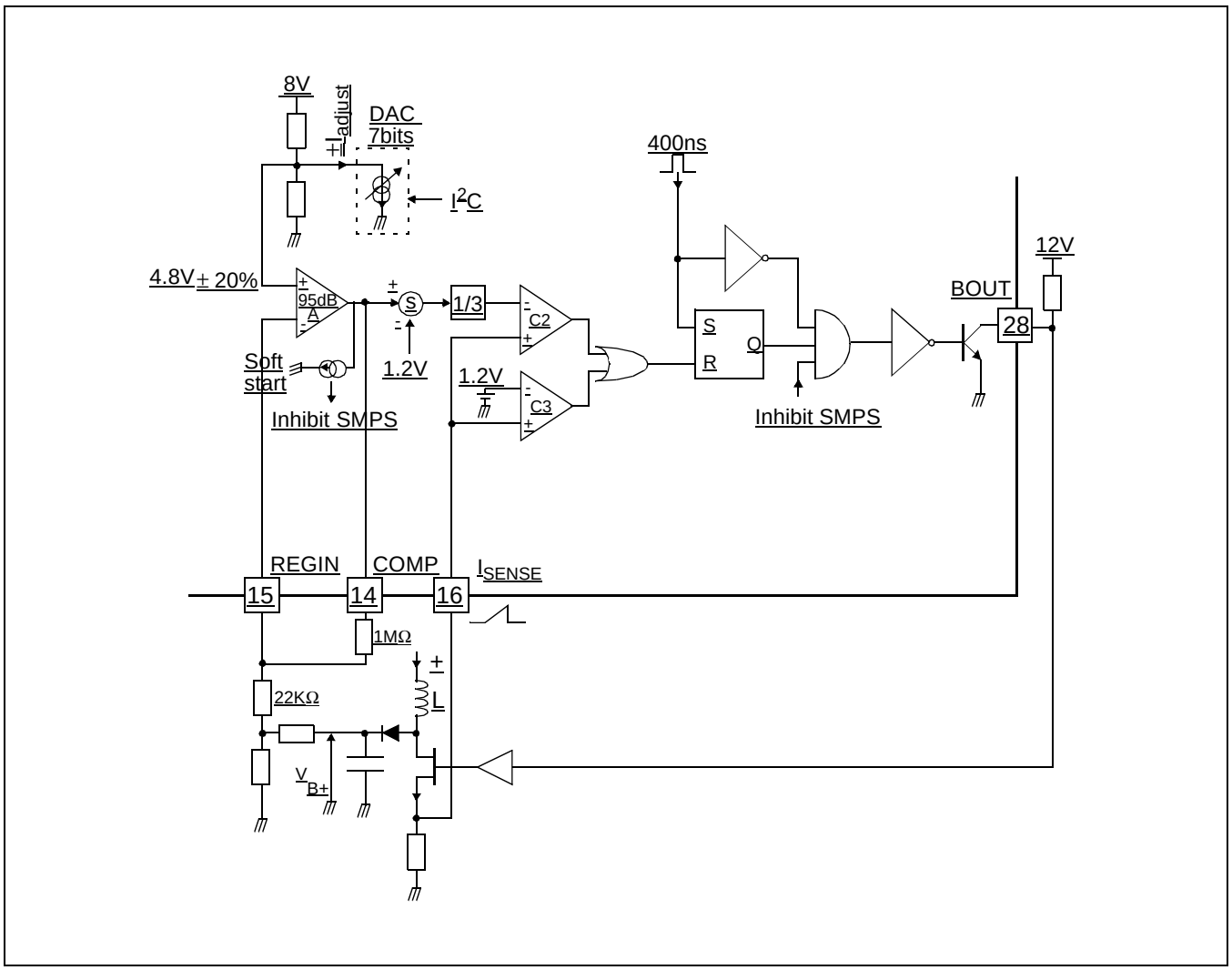


Figure 14. DC/DC Converter Part

SAMSUNG ELECTRONICS

APPLICATION BOARD CIRCUIT

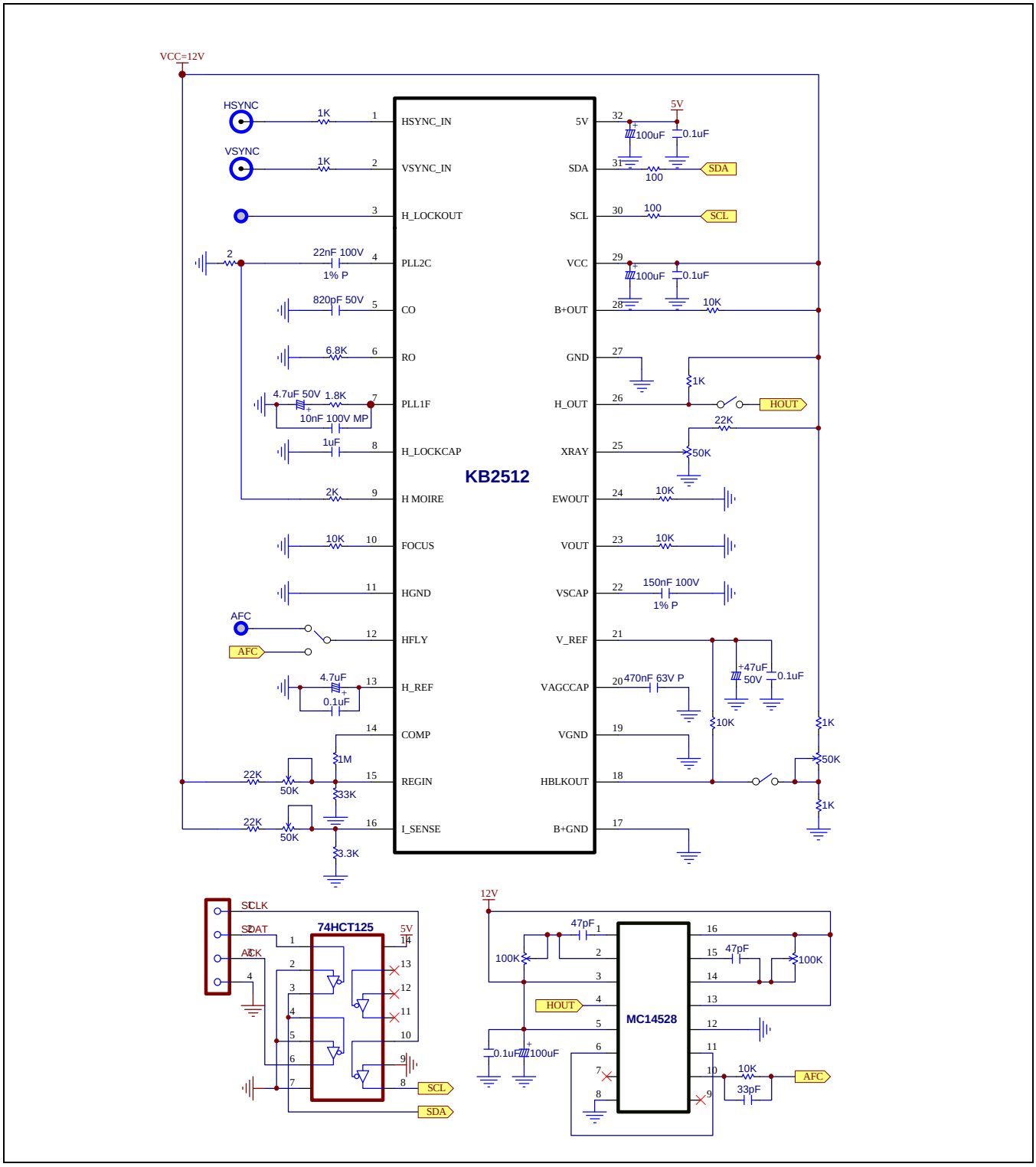


Figure 15. Application Circuit