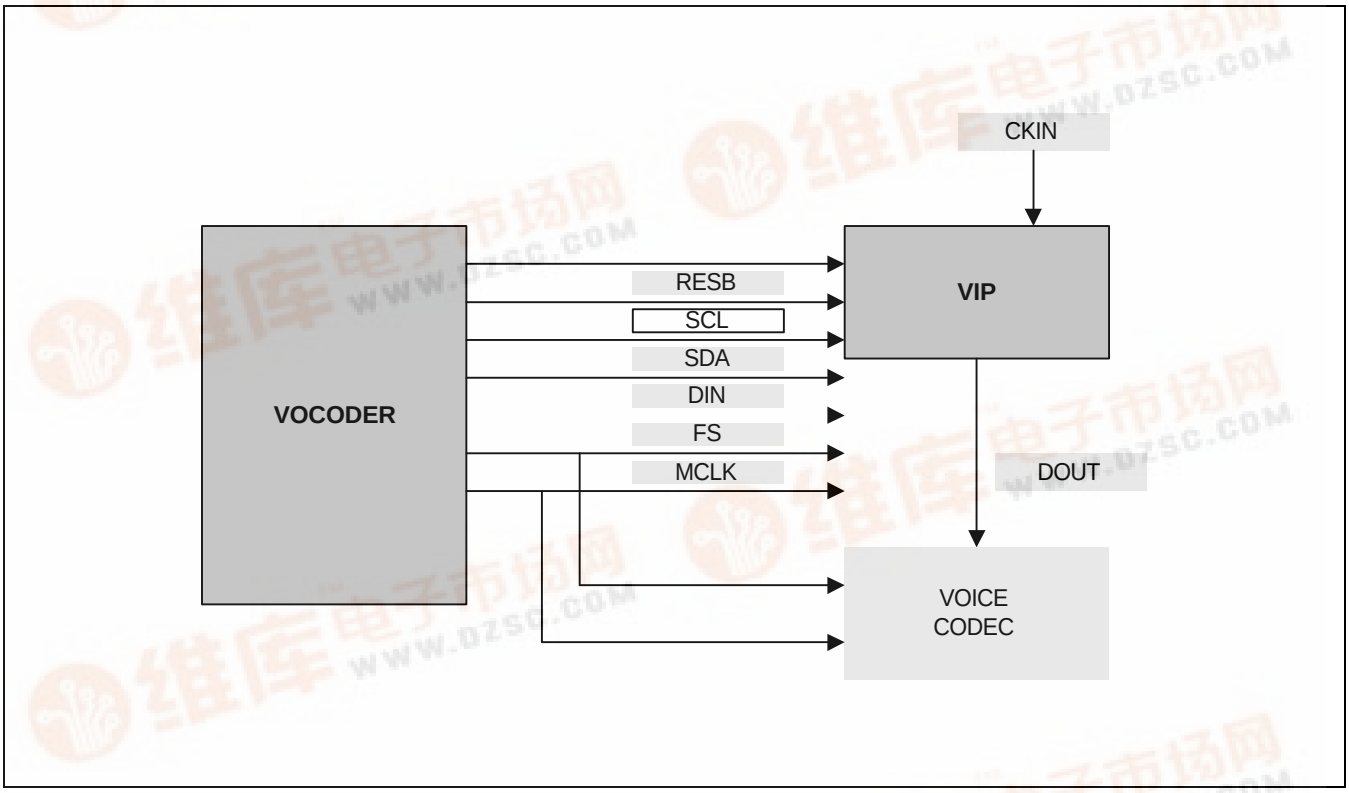
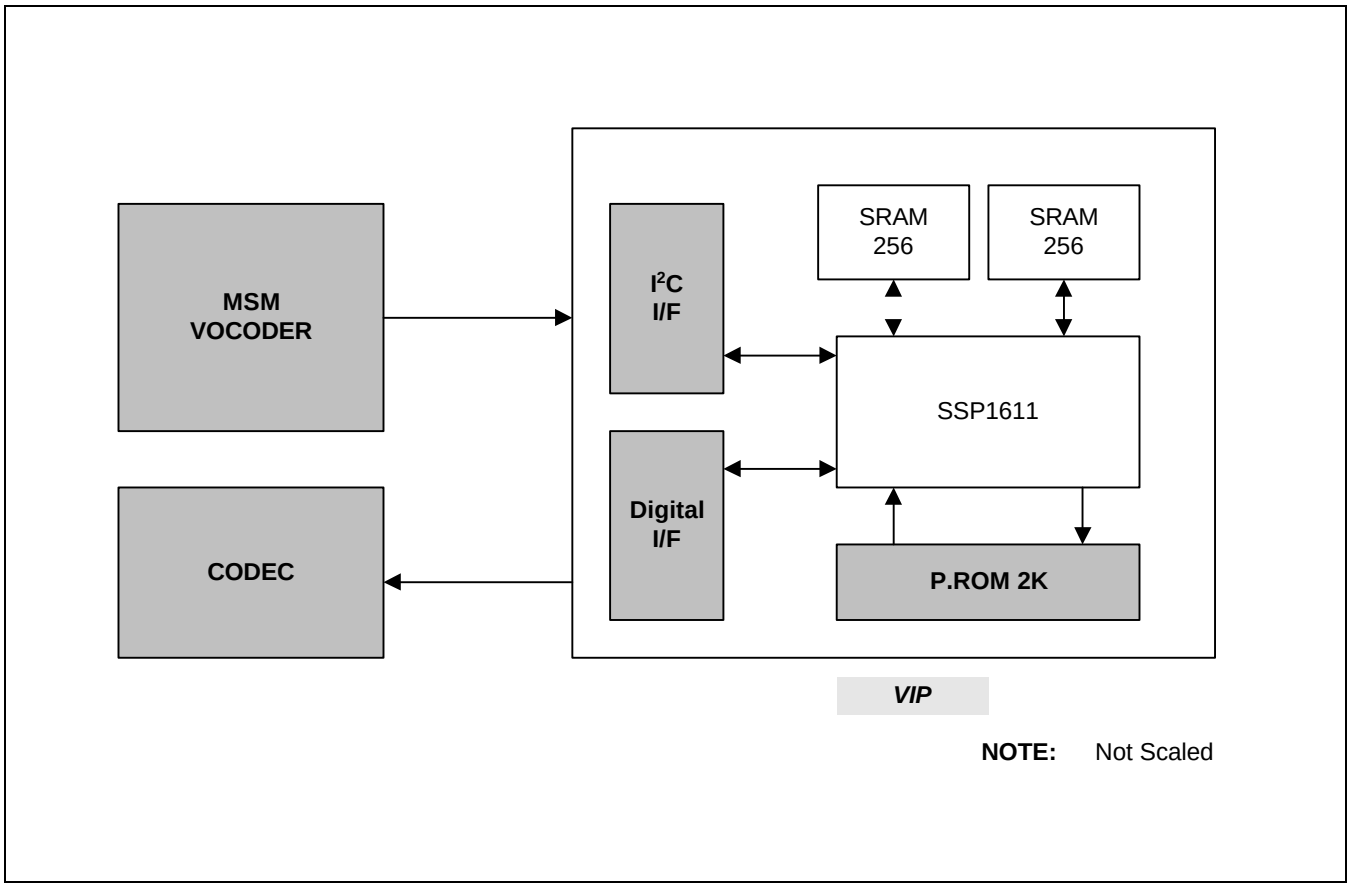
1. BLOCK DIAGRAM

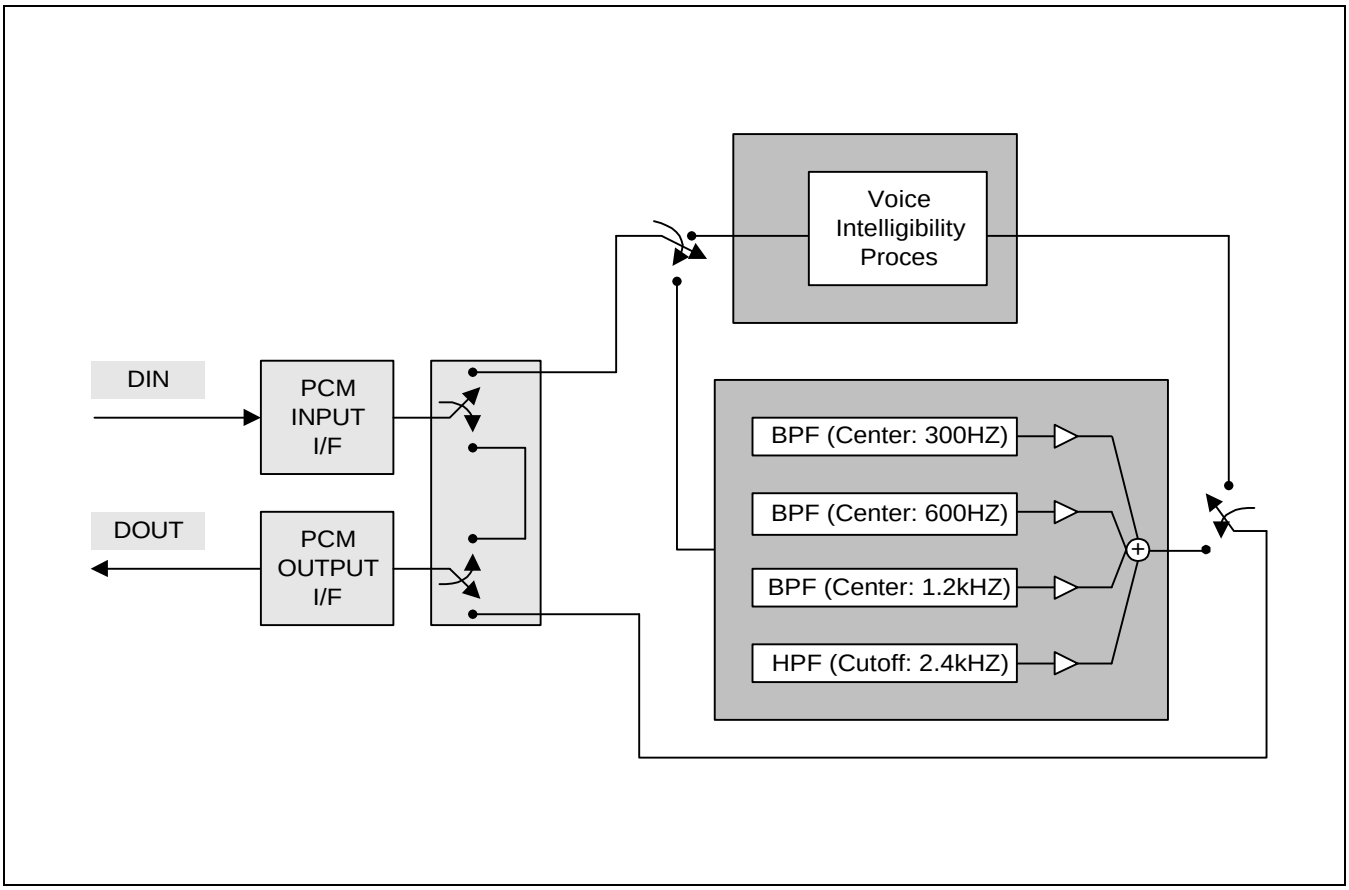
1.1 SYSTEM BLOCK DIAGRAM



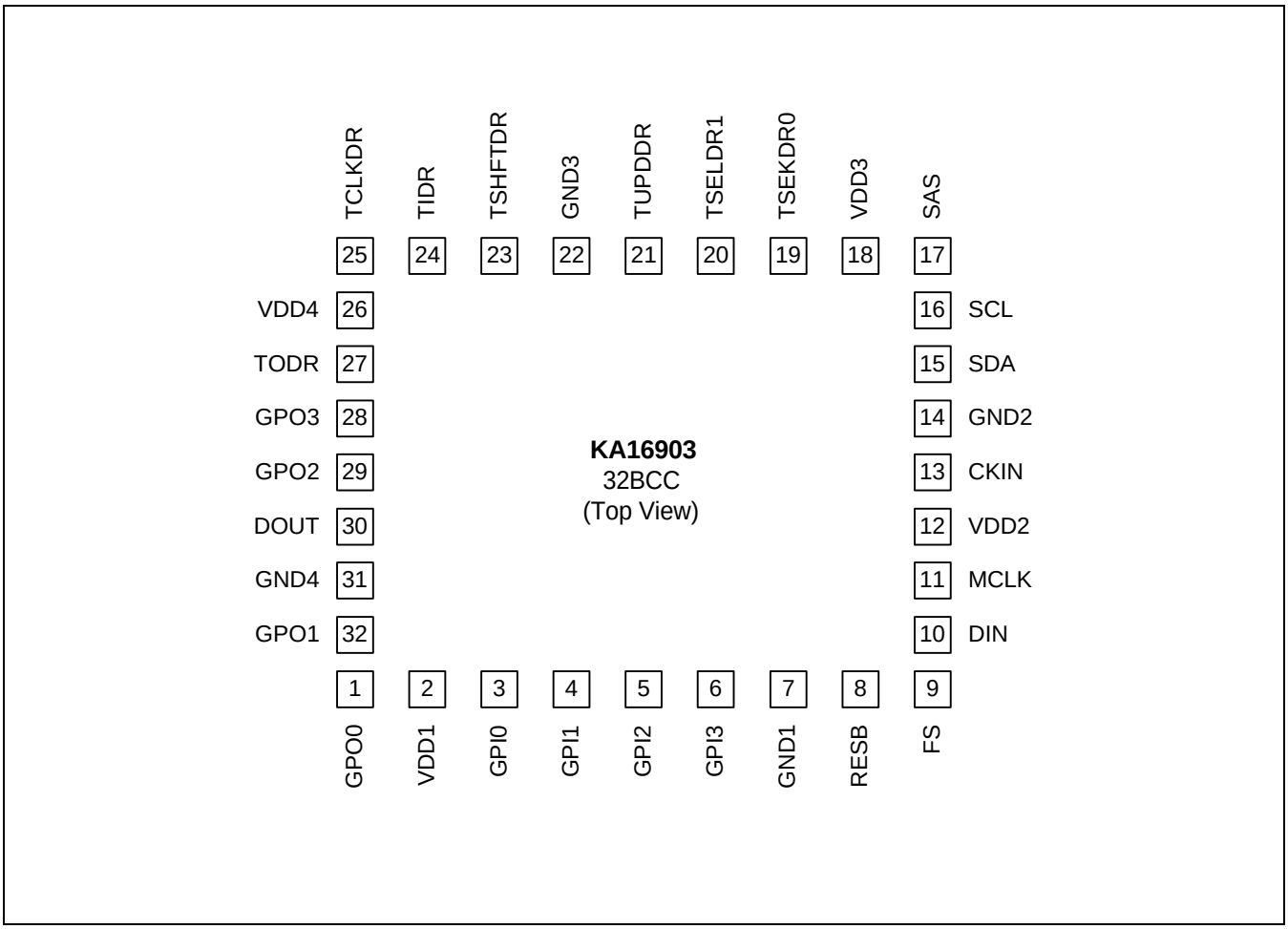
1.2 CHIP BLOCK DIAGRAM



1.3 FUNCTIONAL BLOCK DIAGRAM



2. PIN ASSIGNMENTS



3. PIN DESCRIPTION

Related Block	PIN NAME	PIN NO.	I/O	Description
HIU	RESB	8	I	Reset: Active Low with CKIN(Min 10 cycle)
	SDA	15	I/O	I^2C Serial Data
	SCL	16	I	I^2C Serial Clock
	SAS	17	I	I^2C Address Selection
CIU	DIN	10	I	16 Bit PCM Serial Data In
	DOUT	30	O	16 Bit PCM Serial Data Out
	FS	9	I	PCM Data Frame Sync.
	MCLK	11	I	PCM Data Bit Clock
System	CKIN	13	I	System Clock (9.84MHz)
TEST	GPI0	3	I	Test Pin0 (Host INT. Indicator)
	GPI1	4	I	Test Pin1(0:No Fade, 1:Fade)
	GPI2	5	I	Test Pin2 (0:RAM Test)
	GPI3	6	I	Test Pin3 (0:Codec Bypass)
	TSELDR0	19	I	Test Pin for JTAG
	TSELDR1	20	I	Test Pin for JTAG
	TUPDDR	21	I	Test Pin for JTAG
	TSHFTDR	23	I	Test Pin for JTAG
	TIDR	24	I	Test Pin for JTAG
	TCLKDR	25	I	Test Pin for JTAG
	TODR	27	O	Test Pin for JTAG
	GPO0	1	O	Host Ack. Pin
	GPO1	32	O	Host Test Output
	GPO2	29	O	Host Test Output
	GPO3	28	O	Host Test Output
Power	VDD1, VDD2 VDD3, VDD4	2, 12, 18, 26	P	Digital Power (+3.0V)
Ground	GND1, GND2 GND3, GND4	7, 14, 22, 31	G	Digital GND

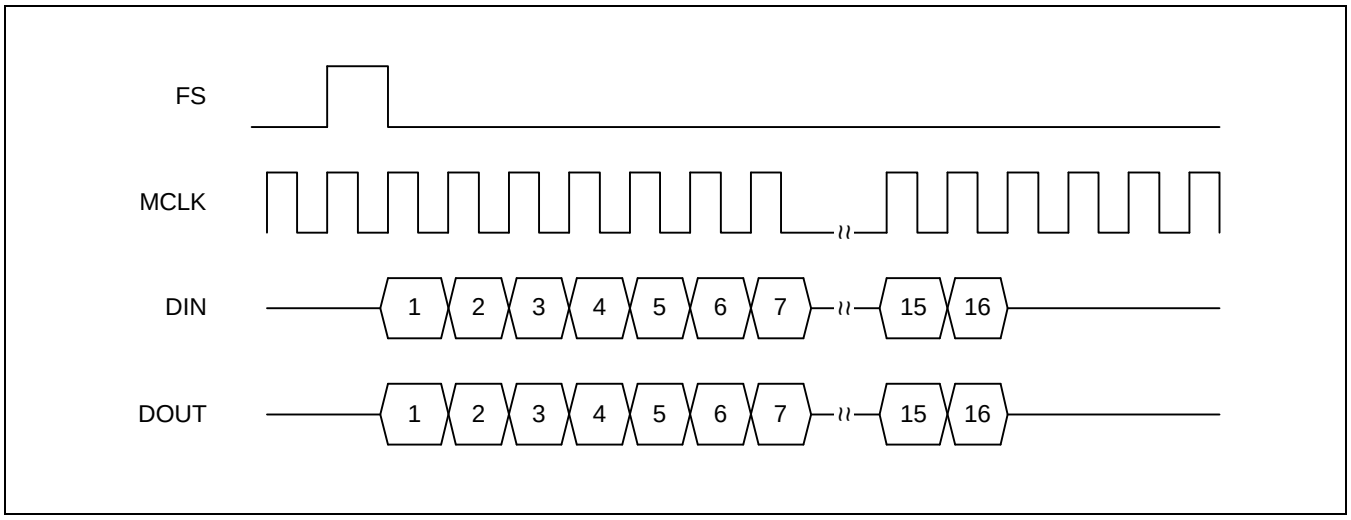
4. DSP PORT ASSIGNMENT FOR I/F WITH PERIPHERALS

I/F	Read/ Write	Port	Interrupt
HIU	Read	EXT1	INT1
	Write	EXT1	
CIU	Read	EXT0	INT0
	Write	EXT0	

5. HARDWARE SPECIFICATION

5.1 CODEC INTERFACE UNIT (CIU)

- Time Diagram



Important!:

During FS (Frame Sync. Clock) high, the falling edge of MCLK (PCM Bit Clock) should exist one time.

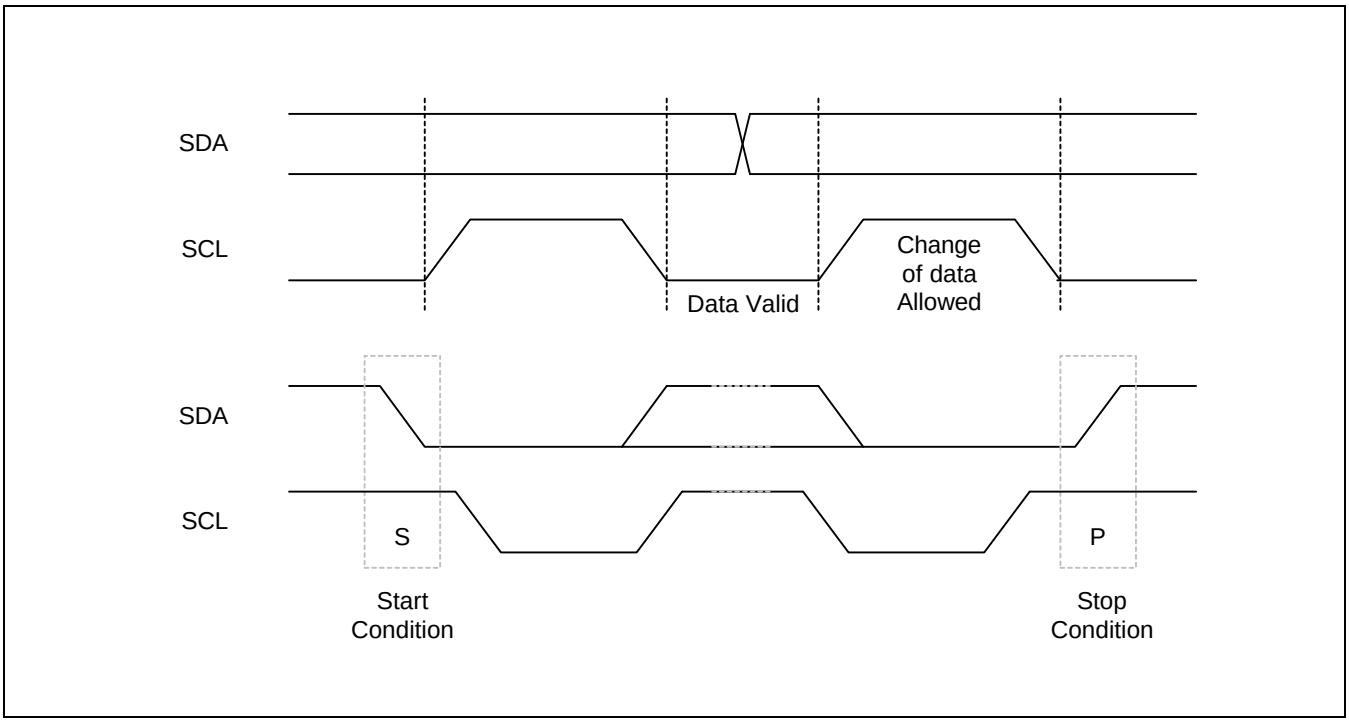
5.2 HOST INTERFACE UNIT (HIU)

- I²C Bus Interface

The VIP can be controlled by a microcontroller via the 2-line I2C bus, SDA (Serial Data Line) and SCL (Serial Clock Line). Both lines must be connected to a positive supply via pull-up resistor. Data transfer may be initiated only when the bus is not busy. When the bus is free, both lines are high. The data on the SDA line must be stable during the high period of clock, SCL. When the SCL is low, the SDA can change. Every byte transferred through the SDA line must contain 8 bits including programmable slave address and read/write direction control bit. Each byte must be followed by acknowledge bit which is sent back to the microcontroller by the VIP by pulling down the SDA line. The MSB is transferred first.

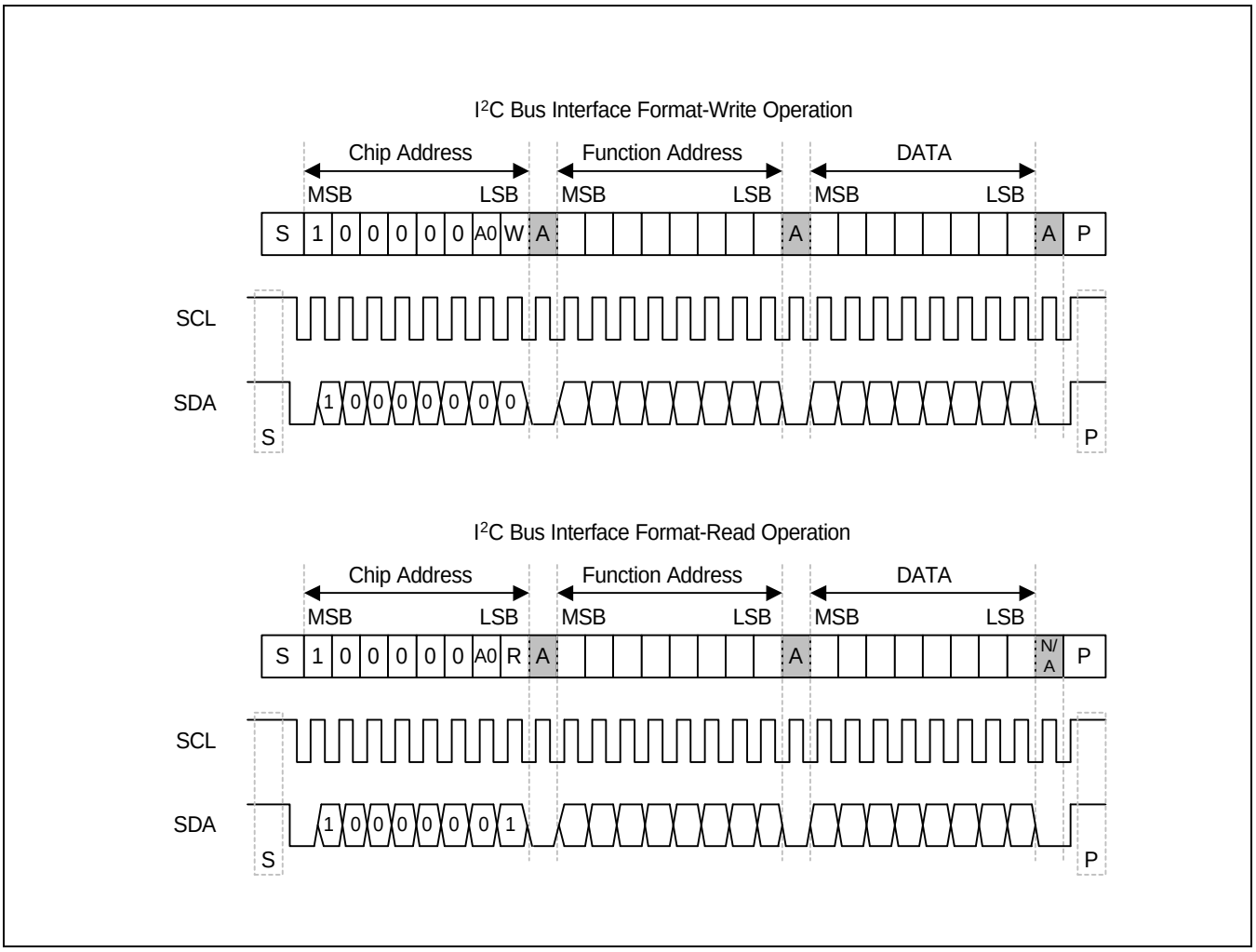
- I²C bus interface start and stop condition

The start condition is high to low transition of the SDA line while the SCL is high. The stop condition is low to high transition of the SDA line while SCL is high.



- I²C Bus Interface Acknowledge

The acknowledge related clock pulse is generated by a microcontroller.
The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. The slave-transmitter generates negative acknowledge when read operation processes. The negative acknowledge is generated by a master (microcontroller).



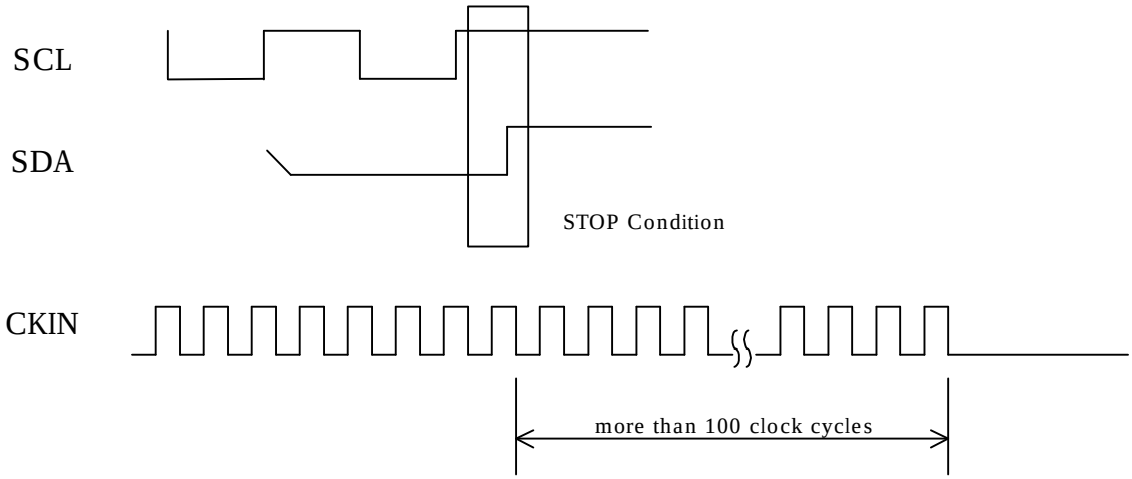
- Relationship between the I2C Bus Interface signal SCL/SDA and main clock of KD16903(CKIN)

Commands are sent from MSM to KD16903 via the I2C (SDA/SCL) bus, triggered by the input signal CKIN. To achieve immunity towards noise, the glitch protection circuitry must be put into operation, thereby meeting the I2C specification.

Thus CKIN should be input with the SDA/SCL.

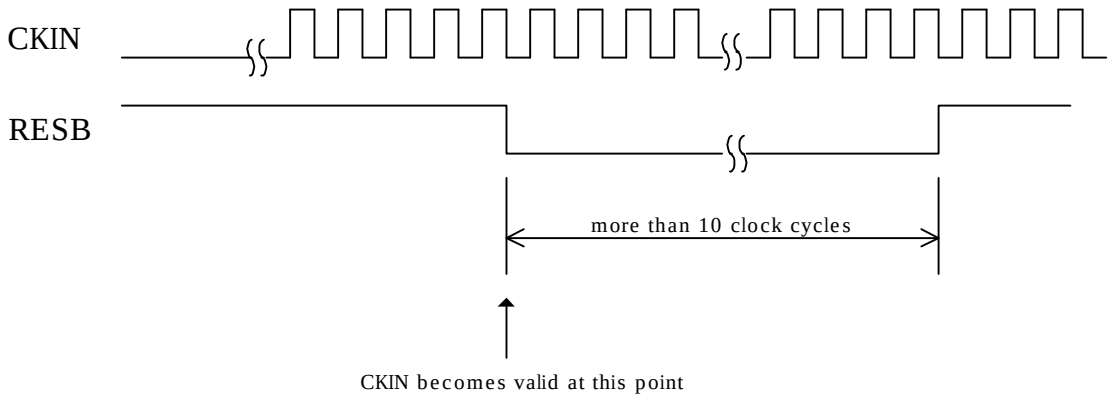
Another issue is, at least 100 clock(CKIN) cycles are needed to execute the command completely by the KD16903. Even as the end condition of the I2C interface is met, the MSM must supply KD16903 with CKIN, as

long as the command is being processed.



RESET Mechanism

RESB should be held "LOW" for more than 10 cycles.



Using RESB

The KD16903 consists of an DSP Unit, Host Interface, and a Codec Interface. And between these internal units, information is exchanged via the interrupt mechanism.
None of the internally exchanged informations are available outside the KD16903.

On the handphone, signals FS, MCLK, CKIN are controlable by the MSM. However, it is also likely that the KD16903 may fall into a state of deadlock, since none of these signals are monitorable externally.

Furthermore trying to escape from the deadlock state by resupplying the FSK, MCLK, CKIN may not guarantee nominal operation.

One way to escape from this deadlock state is to use the external reset mechanism. However, it is a good practice using the internal reset mechanism, supplied at a every new CKIN set, hence avoiding this deadlock state altogether.

To avoid deadlock, Rest must be used for following three cases.
1. Initialization to enter stable state of KD16903.
2. When changing CKIN(CHIPX8) from Hold to Running.
3. When start running Vocoder.

Please note that the corresponding commands for the functions (VIP/EQ) must be downloaded after the Reset.

- Hardware Recommendation for Reset

Separate GPIO port must be assigned for RESB.

6. COMMAND

6.1 SUMMARY

IC Address	Command	Data		Description
80H	01H	-		Bypass (Default, DSP OFF)
80H	02H	-		VIP
80H	03H	-		Equalizer
80H	04H	-		Equalizer Flat
80H	05H	-		Equalizer Mode1
80H	06H	-		Equalizer Mode2
80H	07H	-		Equalizer Mode3
80H	08H	-		Equalizer Mode4
80H	09H	00H		VIP Level 100%
		01H		VIP Level 80%
		02H		VIP Level 60%
80H	0AH	Bit[7:5]	Bit[4:0]	
		000B	00000H - 11000H	Band1 Gain Control
		001B		Band2 Gain Control
		010B		Band3 Gain Control
		011B		Band4 Gain Control
80H	0BH	* * H		Host Test Mode (Return **H). Read after IC Read Address 0x81
80H	0CH	Bit [7:4]	Bit [3:0]	
		0H	0H - CH	VIP Filter1 Gain Control
		...	0H - CH	Bit [3:0] = 0H: +12dB, Bit [3:0] = CH: 0dB, 1dB Step
		9H	0H - CH	VIP Filter10 Gain Control
80H	0DH	00H - FFH		Noise Level Selection
80H	0EH	01H		Return Current Status followed by IC Read Address 0x81, [7:4] = Unused, [3:2] = VIP Level, [1] = Working Mode(0:VIP, 1:EQ), [0] = Bypass Flag (0: DSP ON, 1: DSP OFF)
80H		01H		Return Band1 Tone Level Status followed by IC Read Address 0x81 (00H: -12dB - 18H: + 12dB)
80H		02H		Return Band2 Tone Level Status followed by IC Read Address 0x81
80H		03H		Return Band3 Tone Level Status followed by IC Read Address 0x81
80H		04H		Return Band4 Tone Level Status followed by IC Read Address 0x81

6.2 DESCRIPTION

- Bypass Mode

· Format

Command Code (Hex)	Command Name
01	Bypass

• Description

In bypass mode, DIN (PCM input data line) is directly connected to DOUT (PCM output data line) and the DSP is in stop mode.

- VIP Mode

· Format

Command Code (Hex)	Command Name
02	VIP

· Description

This one byte command selects VIP mode.

- Equalizer Mode

· Format

Command Code (Hex)	Command Name
03	EQ

· Description

This one byte command selects Equalizer mode. Default tone levels are dipicted in

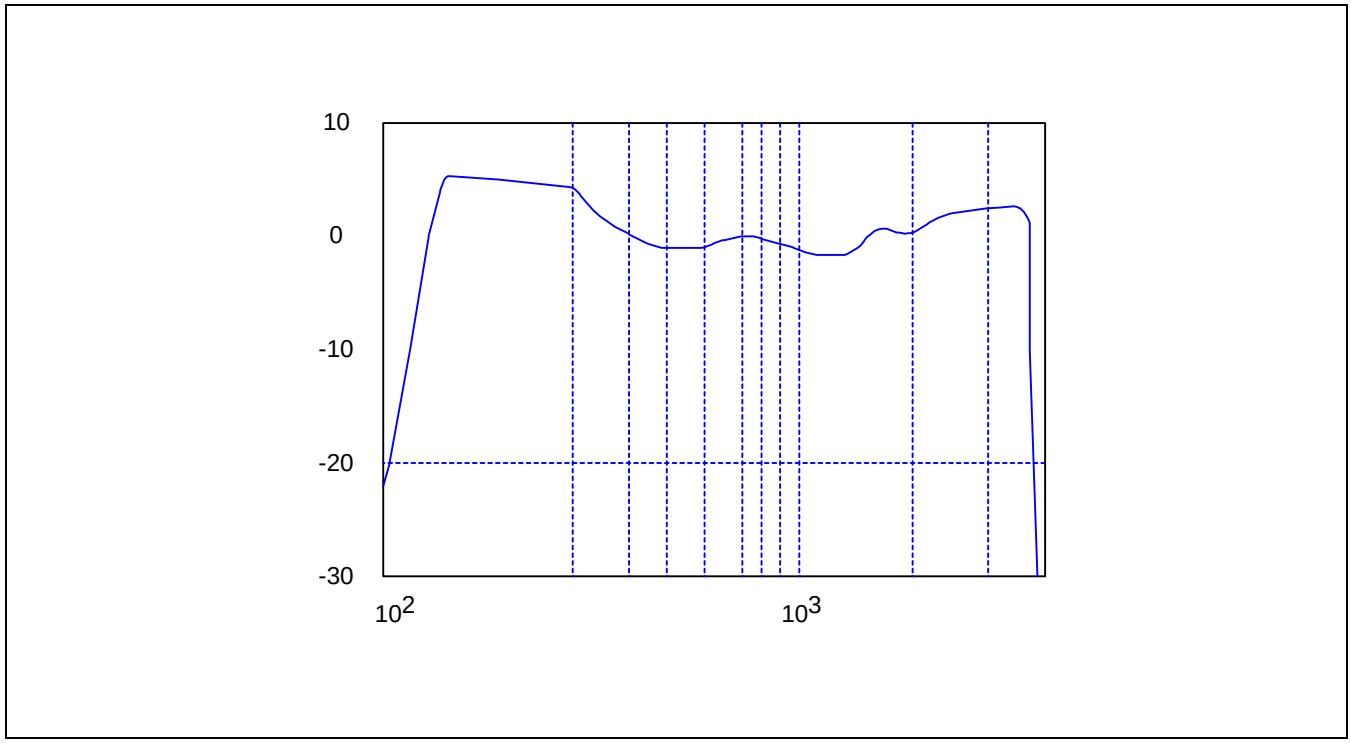


Figure 1: Default Tone Level (Band1: + 4dB, Band2: 0dB, Band3: 0dB, Band4: +1dB)

- VIP Level Select

- **Format**

Command Code (Hex)	Data (Hex)	Command Name	Description
09	00	VIP Level	100% (Max.)
	01		80% (Mid.)
	02		60% (Min.)

· **Description**

When the current mode is the VIP, its level can be changed using incoming data byte after the command. The default VIP level is 80%.

- EQ Mode Select

· **Format**

Command Code (Hex)	Command Name	Description
04	EQ Flat	All Bands are set to 0dB
05	EQ Mode1	Band1: +3dB, Band2: -1dB, Band3: -1dB, Band4: +1dB
06	EQ Mode2	Band1: +3dB, Band2: 0dB, Band3: 0dB, Band4: +3dB
07	EQ Mode3	Band1: +5dB, Band2: 0dB, Band3: 0dB, Band4: 0dB
08	EQ Mode4	Band1: +5dB, Band2: 0dB, Band3: 0dB, Band4: +1dB

· **Description**

Although equalizer can control all four bands, it assigns five preset tone level modes.

- EQ Tone Select

- Format

Command Code (Hex)	Data		Description	Command Name
0A	[7:5]	00	Band1 Select	Tone Control
		01	Band2 Select	
		10	Band3 Select	
		11	Band4 Select	
	[4:0]	00000	+12dB	
		00001	+11dB	
		…		
		01100	0dB	
		…		
		10111	-11dB	
		11000	-12dB	

· **Description**

The equalizer controls four different frequency bands. The gain for each frequency band can be controlled between -12dB and +12dB. The [7:5] in data byte after the command determines the frequency band to be controlled and [4:0] determines gain level.

- VIP Filter Gain Selection

· **Format**

Command Code (Hex)	Data (Hex)		Description	Command Name
0B	[7:4]	0	150Hz Filter Gain to Servo	VIP Filter Gain Control
		1	300Hz Filter Gain to Servo	
		2	150Hz & 300 Hz Sum Gain	
		3	600Hz Filter Gain to Servo	
		4	1.2kHz Filter Gain to Summer	
		5	1.2kHz Filter Gain to Servo	
		6	2.4kHz Filter Gain to Summer	
		7	2.4kHz Filter Gain to Servo	
		8	4.8kHz Filter Gain to Summer	
		9	4.8kHz Filter Gain to Servo	
	[3:0]	0	+ 12dB	
		1	+ 11dB	
			…	
		C	0dB	

· **Description**

These commands select the gains of filter outputs in the VIP mode. The detailed description of filter structure can be found in "VIP specification" published by SRS Labs.

- Noise Level Selection

· **Format**

Command Code (Hex)	Data (Hex)	Description	Command Name
0D	00 - FF	Assume the value in data as noise level	Noise Level Select

· **Description**

When the input from ADC has small noise, this noise can incresed in VIP or EQ mode since the specific frequency levels are increased. To avoid this problem in mute, the input data is tested for 25ms. If the absolute values of input data are less than noise level specified in Data and stay for 25ms, then the input is considered as zeros and are processed. Default noise level is set to 0x1F.

- Current Status

· **Format**

Command Code (Hex)	Data (Hex)	Description	Command Name
0E	01	Return current status register contents	Current Status

· **Description**

It returns the contents of the current status register as:
Status [7:4] = unused
Status [3:2] = VIP Level (00: 100%, 01: 80%, 10: 60%)
Status [1] = Working Mode (0: VIP, 1:EQ)
Status [0] = DSP On/Off (0: DSP On, 1: DSP Off)

- EQ Tone Level Status

· **Format**

Command Code (Hex)	Data (Hex)	Description	Command Name
0E	02	Return current band1 tone level	Current Tone Level Status
	03	Return current band2 tone level	
	04	Return current band3 tone level	
	05	Return current band4 tone level	

· **Description**

These commands return the current tone levels in EQ mode. Returned byte value is between 0x00 (-12dB) and 0x18 (+12dB).

7. MEMORY SIZE AND REQUIRED MIPS

7.1 MEMORY SIZE

Memory		Size (word*)
Data	Bank 0	256
	Bank 1	256
Program	VIP	800
	4band EQ	500
	Test	400
	Others	100
	Total	1860

* word = 16 bit

7.2 MIPS

Routines	No. of Cycles	MIPS	Remark
VIP	650	5.2	-
4band EQ	400	3.2	Working only when VIP is OFF
Others	80	0.64	-
Total (VIP ON) = 650 + 70 + 80 = 800 (6.4 MIPS)			

8. ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Vcc = 2.7V to 3.3V, TA = -30°C to 85°C ; typical characteristic are specified at Vcc = 3.0V, TA = 25°C; all signals are referenced to GND)

8.1 DIGITAL INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VIL	Input Low Voltage		0.8			V
VIH	Input High Voltage				1.9	V
VOL	Output Low Voltage	I_{OL} = 1uA			0.05	V
		I_{OL} = 4mA (see Note1)			0.4	V
		I_{OL} = 8mA (see Note 2)				
VOH	Output High Voltage	I_{OH} = -1uA	V_{DD}-0.05			V
		I_{OH} = -4mA (see Note1)	2.4			V
		I_{OH} = -8mA (see Note2)				
IIL	Input Low Current	V_{IN} = Vss	-10		10	uA
		V_{IN} = V_{SS} (see Note3)	-60	-30	-10	uA
IIH	Input High Current	V_{IN} = V_{DD}	-10		10	uA
		V_{IN} = V_{DD} (see Note4)	60	30	10	uA
IOZ	Output Current in High impedance (Tri-state)	V_{OUT} = V_{SS} or V_{DD}	-5		5	uA

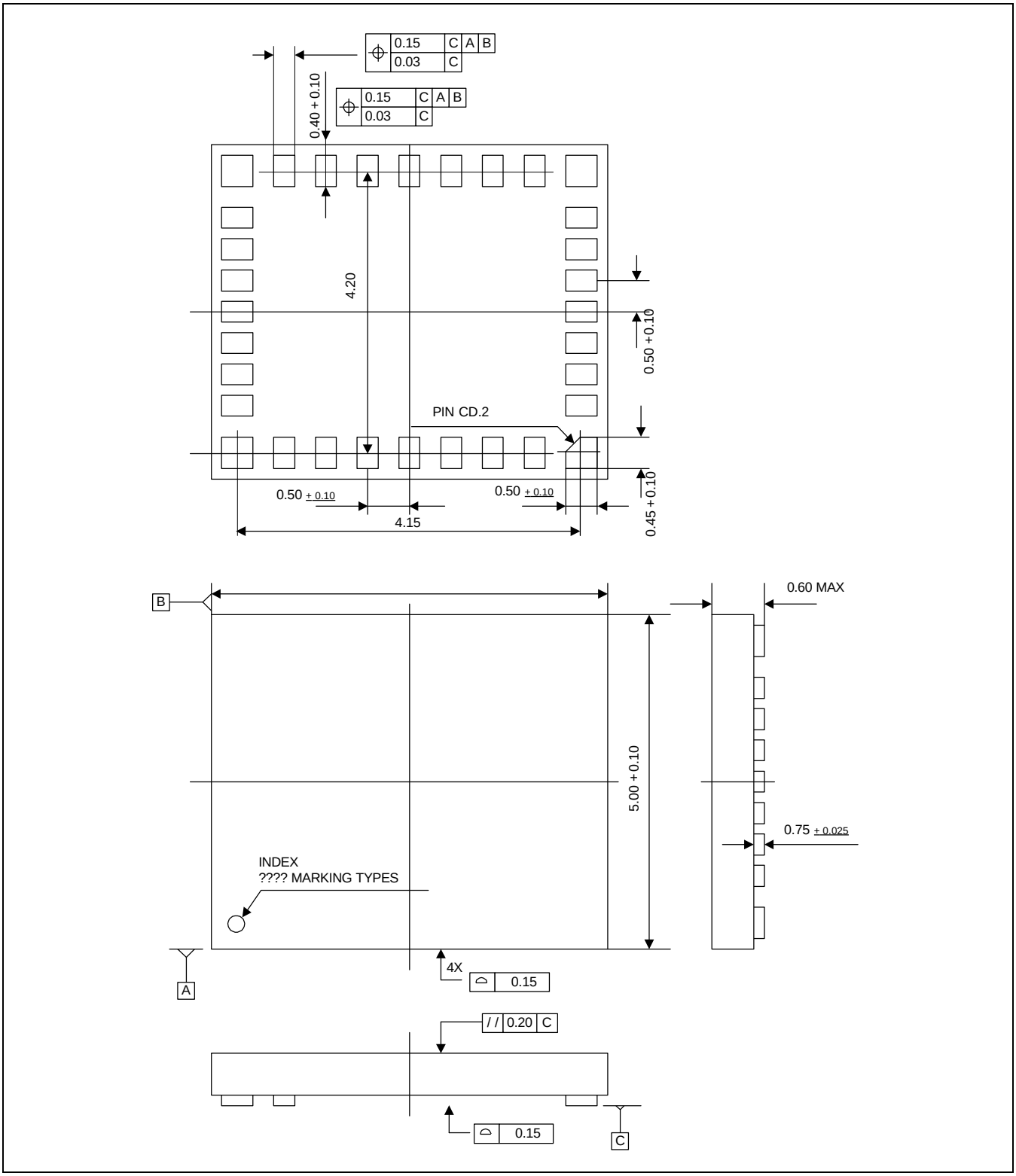
NOTES:
1. Normal Output Pin
2. SDA ,SCL Output Pin
3. Input Buffer with pull -up (3, 4, 5, 6, 8 Pin)
4. Input Buffer with pull -down (17, 19, 20, 21, 23, 24, 25 Pin)

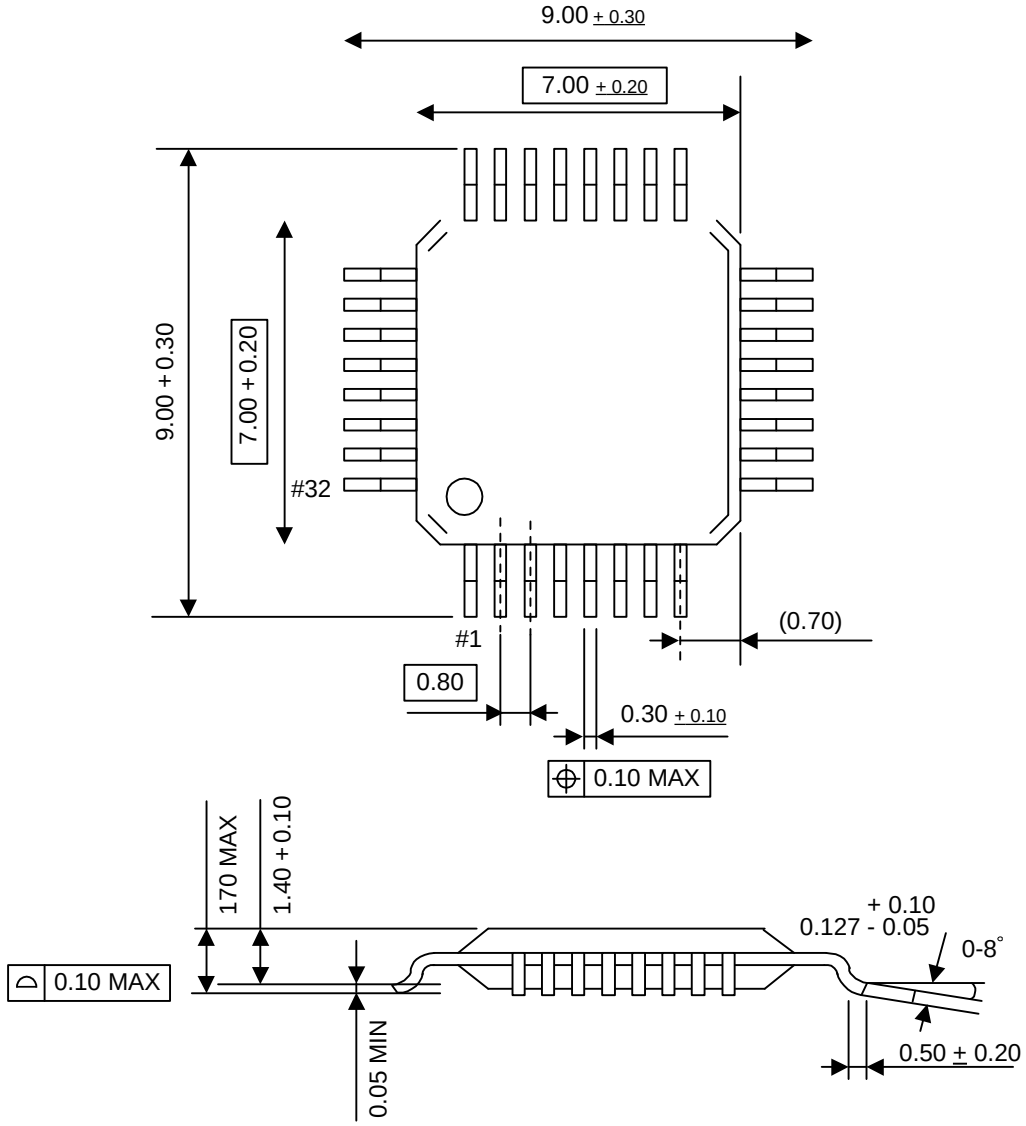
8.2 POWER DISSIPATION (@3.3V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ICC0	Operation Current	VIP or EQ Operation Mode	-	3	4	mA
ICC1	Bypass Current	Bypass Operation Mode	-	100	150	uA
ICC2	Static Current	No Operation (Sleep Mode)	-	10		uA

9. PACKAGE DIMENSION

9.1 32 BCC TYPE




9.00 + 0.30
7.00 + 0.20
9.00 + 0.30
7.00 + 0.20
#32
#1
(0.70)
0.80
0.30 + 0.10
0.10 MAX
170 MAX
1.40 + 0.10
+ 0.10
0.127 - 0.05
0-8°
0.10 MAX
0.05 MIN
0.50 + 0.20