

## Dual LDO with Low Noise, Very High PSRR, and Low I<sub>Q</sub>

ISL9000 is a high performance dual LDO capable of sourcing 300mA current from each output. It has a low standby current and very high PSRR and is stable with output capacitance of 1 $\mu$ F to 10 $\mu$ F with ESR of up to 200m $\Omega$ .

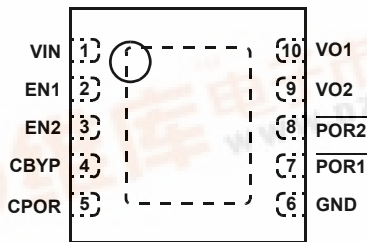
The device integrates an individual Power-On-Reset (POR) function for each output. The POR delay for VO2 can be externally programmed by connecting a timing capacitor to the CPOR pin. The POR delay for VO1 is internally fixed at approximately 2ms. A reference bypass pin is also provided for connecting a noise filtering capacitor for low noise and high-PSRR applications.

The quiescent current is typically only 42 $\mu$ A with both LDO's enabled and active. Separate enable pins control each individual LDO output. When both enable pins are low, the device is in shutdown, typically drawing less than 0.1 $\mu$ A.

Several combinations of voltage outputs are standard. Others are available on request. Output voltage options for each LDO range from 1.2V to 3.6V.

### Pinout

ISL9000  
10 LD 3X3 DFN  
TOP VIEW



### Features

- Integrates two 300mA high performance LDO's
- Excellent transient response to large current steps
- $\pm 1.8\%$  accuracy over all operating conditions
- Excellent load regulation:  
< 0.1% voltage change across full range of load current
- Low output noise: typically 30 $\mu$ Vrms @ 100 $\mu$ A (1.5V)
- Very high PSRR: 90dB @ 1kHz
- Extremely low quiescent current: 42 $\mu$ A (both LDOs active)
- Wide input voltage capability: 2.3V - 6.5V
- Low dropout voltage: typically 200mV @ 300mA
- Stable with 1-10 $\mu$ F ceramic capacitors
- Separate enable and POR pins for each LDO
- Soft-start and staged turn-on to limit input current surge during enable
- Current limit and overheat protection
- Tiny 10 Ld 3x3mm DFN package
- -40°C to +85°C operating temperature range
- Pb-free plus anneal available (RoHS compliant)

### Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices including Medical Handhelds

## ISL9000

### Ordering Information

| PART NUMBER<br>(Notes 1, 2, 3) | PART MARKING | VO1 VOLTAGE | VO2 VOLTAGE | TEMP RANGE (°C) | PACKAGE<br>(Pb-Free) | PKG DWG. # |
|--------------------------------|--------------|-------------|-------------|-----------------|----------------------|------------|
| ISL9000IRNJZ                   | DAAA         | 3.3V        | 2.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRNFZ                   | DBAA         | 3.3V        | 2.5V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRMMZ                   | DSAA         | 3.0V        | 3.0V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRLLZ                   | DRAA         | 2.9V        | 2.9V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRKKZ                   | DCAA         | 2.85V       | 2.85V       | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRKJZ                   | DDAA         | 2.85V       | 2.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRKFZ                   | DEAA         | 2.85V       | 2.5V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRKCZ                   | DHAA         | 2.85V       | 1.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRJMZ                   | DPAA         | 2.8V        | 3.0V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRJRZ                   | DNAA         | 2.8V        | 2.6V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRJCZ                   | DMAA         | 2.8V        | 1.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRJBZ                   | DFAA         | 2.8V        | 1.5V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRGCZ                   | DLAA         | 2.7V        | 1.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRFJZ                   | DGAA         | 2.5V        | 2.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRPLZ                   | DKAA         | 1.85V       | 2.9V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |
| ISL9000IRBJZ                   | DJAA         | 1.5V        | 2.8V        | -40 to +85      | 10 Ld 3x3 DFN        | L10.3x3C   |

#### NOTES:

1. Add -T to part number for tape and reel.
2. For other output voltages, contact Intersil Marketing.
3. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# ISL9000

## Absolute Maximum Ratings

|                                |                    |
|--------------------------------|--------------------|
| Supply Voltage (VIN) . . . . . | +7.1V              |
| All Other Pins . . . . .       | -0.3 to (VIN+0.3)V |

## Recommended Operating Conditions

|  |               |
|--|---------------|
| Ambient Temperature Range (TA) . . . . . | -40°C to 85°C |
| Supply Voltage (VIN) . . . . .           | 2.3 to 6.5V   |

## Thermal Information

|  |                      |                      |
|--|----------------------|----------------------|
| Thermal Resistance (Notes 1, 2)                    | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
| 3x3 DFN Package . . . . .                          | 50                   | 10                   |
| Junction Temperature Range . . . . .               | -40°C to +125°C      |                      |
| Operating Temperature Range . . . . .              | -40°C to +85°C       |                      |
| Storage Temperature Range . . . . .                | -65°C to +150°C      |                      |
| Maximum Lead Temperature (Soldering 10s) . . . . . | +300°C               |                      |

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- $\theta_{JC}$ , "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

## Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:  
 $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{IN} = (V_O + 0.5\text{V})$  to 6.5V with a minimum  $V_{IN}$  of 2.3V;  $C_{IN} = 1\mu\text{F}$ ;  $C_O = 1\mu\text{F}$ ;  
 $C_{BYP} = 0.01\mu\text{F}$ ;  $C_{POR} = 0.01\mu\text{F}$

| PARAMETER                              | SYMBOL    | TEST CONDITIONS   | MIN  | TYP | MAX  | UNITS            |
|--|-----------|---|------|-----|------|------------------|
| <b>DC CHARACTERISTICS</b>              |           |   |      |     |      |                  |
| Supply Voltage                         | $V_{IN}$  |   | 2.3  |     | 6.5  | V                |
| Ground Current                         |           | Quiescent condition: $I_{O1} = 0\mu\text{A}$ ; $I_{O2} = 0\mu\text{A}$  |      |     |      |                  |
|  | $I_{DD1}$ | One LDO active  |      | 25  | 32   | $\mu\text{A}$    |
|  | $I_{DD2}$ | Both LDO active   |      | 42  | 52   | $\mu\text{A}$    |
| Shutdown Current                       | $I_{DDS}$ | @25°C   |      | 0.1 | 1.0  | $\mu\text{A}$    |
| UVLO Threshold                         | $V_{UV+}$ |   | 1.9  | 2.1 | 2.3  | V                |
|  | $V_{UV-}$ |   | 1.6  | 1.8 | 2.0  | V                |
| Regulation Voltage Accuracy            |           | Initial accuracy at $V_{IN} = V_O + 0.5\text{V}$ , $I_O = 10\text{mA}$ , $T_J = 25^\circ\text{C}$                           | -0.7 |     | +0.7 | %                |
|  |           | $V_{IN} = V_O + 0.5\text{V}$ to 5.5V, $I_O = 10\mu\text{A}$ to 300mA, $T_J = 25^\circ\text{C}$                              | -0.8 |     | +0.8 | %                |
|  |           | $V_{IN} = V_O + 0.5\text{V}$ to 5.5V, $I_O = 10\mu\text{A}$ to 300mA, $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$      | -1.8 |     | +1.8 | %                |
| Maximum Output Current                 | $I_{MAX}$ | Continuous  | 300  |     |      | mA               |
| Internal Current Limit                 | $I_{LIM}$ |   | 350  | 475 | 600  | mA               |
| Dropout Voltage (Note 4)               | $V_{DO1}$ | $I_O = 300\text{mA}$ ; $V_O < 2.5\text{V}$  |      | 300 | 500  | mV               |
|  | $V_{DO2}$ | $I_O = 300\text{mA}$ ; $2.5\text{V} \leq V_O \leq 2.8\text{V}$  |      | 250 | 400  | mV               |
|  | $V_{DO3}$ | $I_O = 300\text{mA}$ ; $V_O > 2.8\text{V}$  |      | 200 | 325  | mV               |
| Thermal Shutdown Temperature           | $T_{SD+}$ |   |      | 145 |      | °C               |
|  | $T_{SD-}$ |   |      | 110 |      | °C               |
| <b>AC CHARACTERISTICS</b>              |           |   |      |     |      |                  |
| Ripple Rejection (Note 3)              |           | $I_O = 10\text{mA}$ , $V_{IN} = 2.8\text{V}(\text{min})$ , $V_O = 1.8\text{V}$ , $C_{BYP} = 0.1\mu\text{F}$                 |      |     |      |                  |
|  |           | @ 1kHz  |      | 90  |      | dB               |
|  |           | @ 10kHz   |      | 70  |      | dB               |
|  |           | @ 100kHz  |      | 50  |      | dB               |
| Output Noise Voltage (Note 3)          |           | $I_O = 100\mu\text{A}$ , $V_O = 1.5\text{V}$ , $T_A = 25^\circ\text{C}$ , $C_{BYP} = 0.1\mu\text{F}$<br>BW = 10Hz to 100kHz |      | 30  |      | $\mu\text{Vrms}$ |
| <b>DEVICE START-UP CHARACTERISTICS</b> |           |   |      |     |      |                  |
| Device Enable Time                     | $T_{EN}$  | Time from assertion of the ENx pin to when the output voltage reaches 95% of the $V_O(\text{nom})$                          |      | 250 | 500  | $\mu\text{s}$    |

# ISL9000

## Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{IN} = (V_O + 0.5\text{V})$  to  $6.5\text{V}$  with a minimum  $V_{IN}$  of  $2.3\text{V}$ ;  $C_{IN} = 1\mu\text{F}$ ;  $C_O = 1\mu\text{F}$ ;  $C_{BYP} = 0.01\mu\text{F}$ ;  $C_{POR} = 0.01\mu\text{F}$  **(Continued)**

| PARAMETER                                  | SYMBOL           | TEST CONDITIONS  | MIN  | TYP | MAX            | UNITS                  |
|--|------------------|--|------|-----|----------------|------------------------|
| LDO Soft-start Ramp Rate                   | $T_{SSR}$        | Slope of linear portion of LDO output voltage ramp during start-up |      | 30  | 60             | $\mu\text{s}/\text{V}$ |
| <b>EN1, EN2 PIN CHARACTERISTICS</b>        |                  |  |      |     |                |                        |
| Input Low Voltage                          | $V_{IL}$         |  | -0.3 |     | 0.5            | V                      |
| Input High Voltage                         | $V_{IH}$         |  | 1.4  |     | $V_{IN} + 0.3$ | V                      |
| Input Leakage Current                      | $I_{IL}, I_{IH}$ |  |      |     | 0.1            | $\mu\text{A}$          |
| Pin Capacitance                            | $C_{PIN}$        | Informative  |      | 5   |                | pF                     |
| <b>POR1, POR2 PIN CHARACTERISTICS</b>      |                  |  |      |     |                |                        |
| POR1, POR2 Thresholds                      | $V_{POR+}$       | As a percentage of nominal output voltage                          | 91   | 94  | 97             | %                      |
|  | $V_{POR-}$       |  | 87   | 90  | 93             | %                      |
| POR1 Delay                                 | $T_{P1LH}$       |  | 1.0  | 2.0 | 3.0            | ms                     |
|  | $T_{P1HL}$       |  |      | 25  |                | $\mu\text{s}$          |
| POR2 Delay                                 | $T_{P2LH}$       | $C_{POR} = 0.01\mu\text{F}$  | 100  | 200 | 300            | ms                     |
|  | $T_{P2HL}$       |  |      | 25  |                | $\mu\text{s}$          |
| POR1, POR2 Pin Output Low Voltage          | $V_{OL}$         | @ $I_{OL} = 1.0\text{mA}$  |      |     | 0.2            | V                      |
| POR1, POR2 Pin Internal Pull-up Resistance | $R_{POR}$        |  | 78   | 100 | 130            | $\text{k}\Omega$       |

### NOTES:

- Guaranteed by design and characterization.
- $V_{OX} = 0.98 * V_{OX}(\text{NOM})$ ; Valid for  $V_{OX}$  greater than 1.85V.

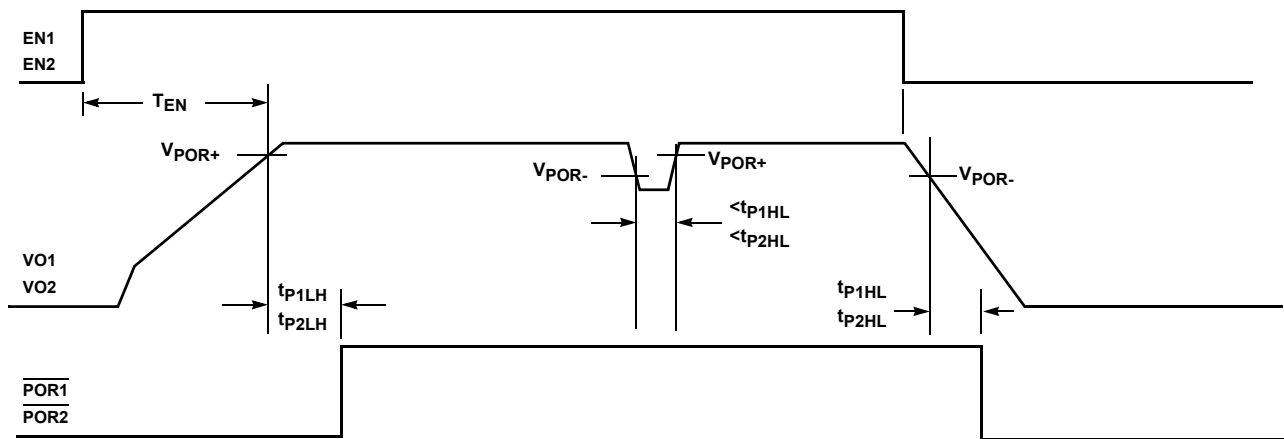


FIGURE 1. TIMING PARAMETER DEFINITION

Typical Performance Curves

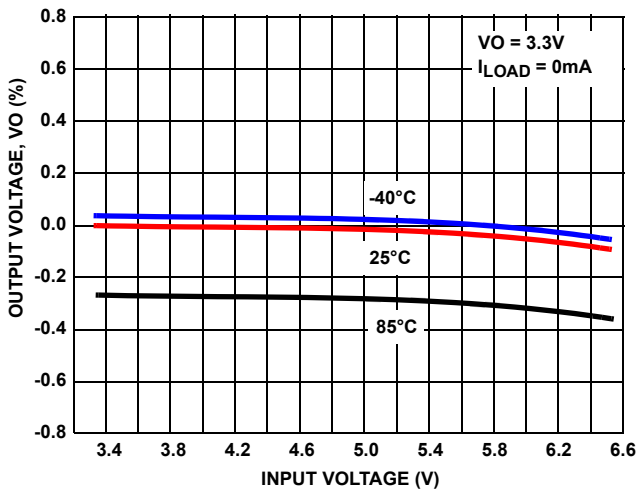


FIGURE 2. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

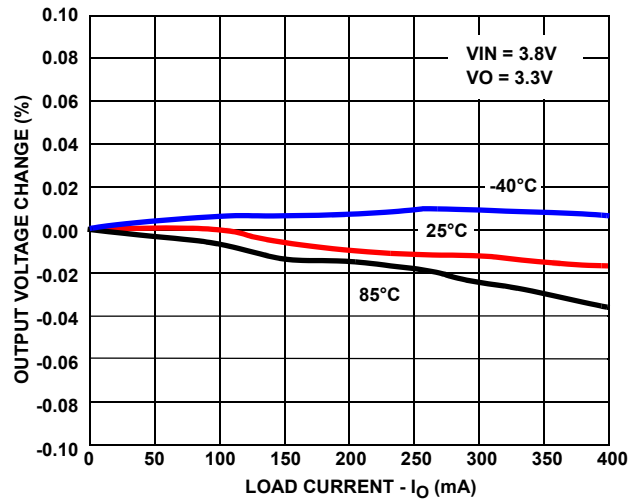


FIGURE 3. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

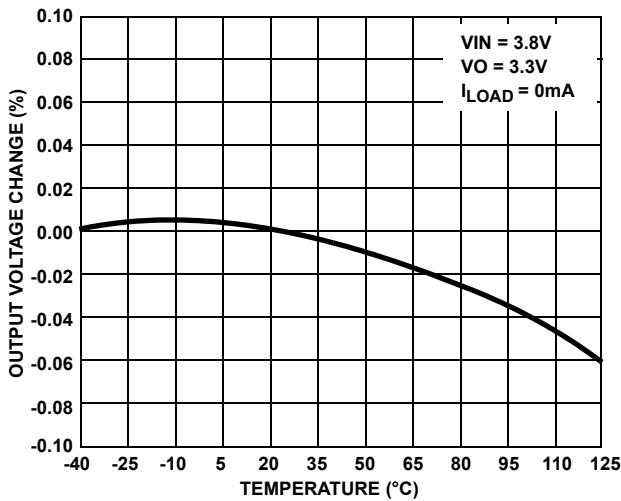


FIGURE 4. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

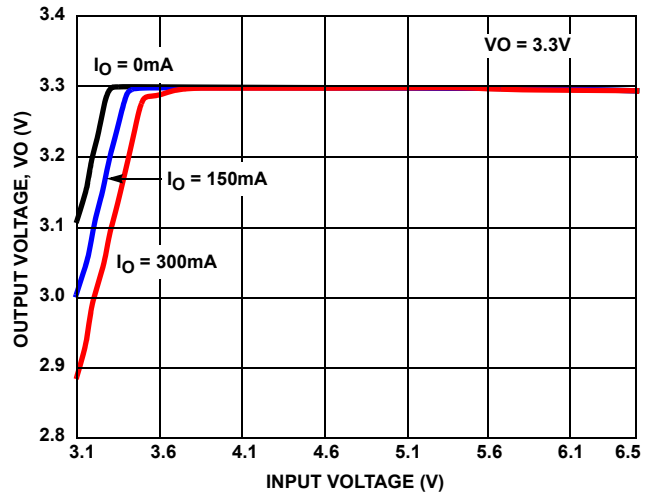


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

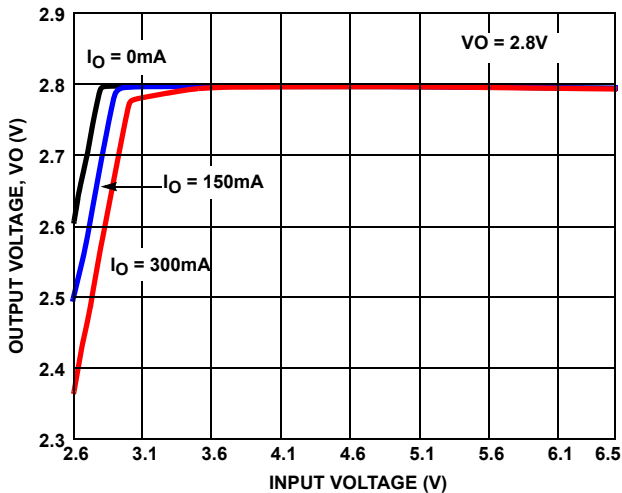


FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

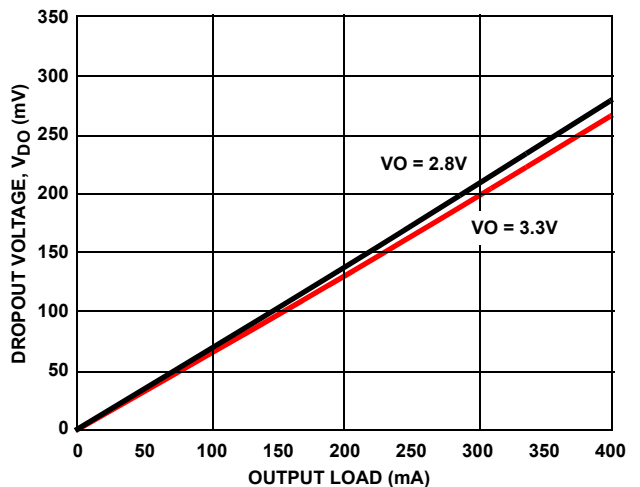


FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

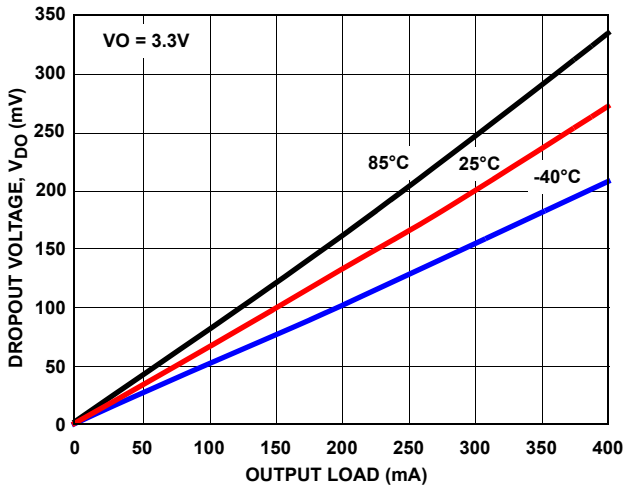


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

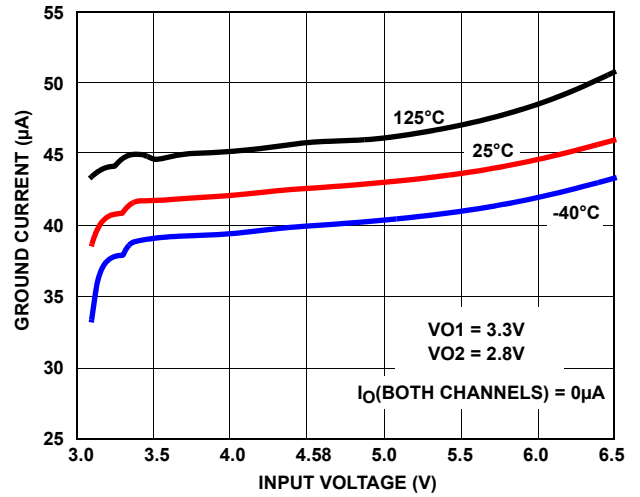


FIGURE 9. GROUND CURRENT vs INPUT VOLTAGE

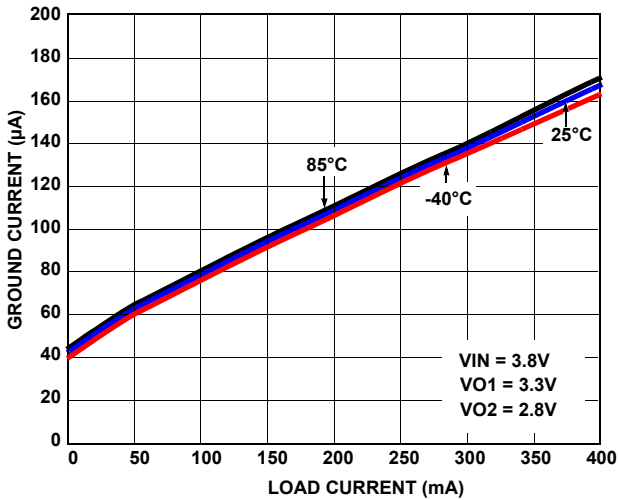


FIGURE 10. GROUND CURRENT vs LOAD

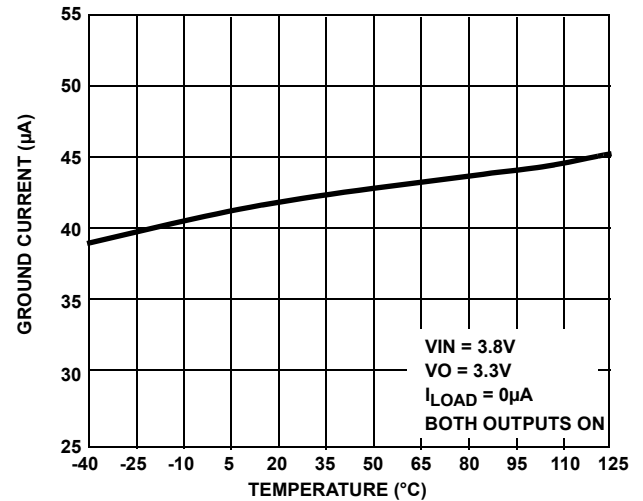


FIGURE 11. GROUND CURRENT vs TEMPERATURE

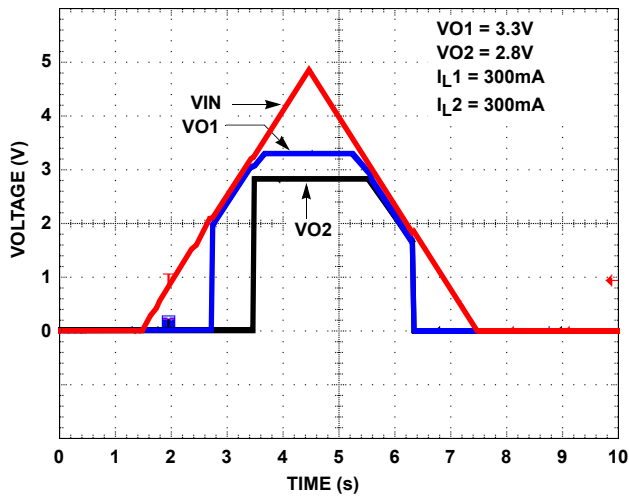


FIGURE 12. POWER-UP/POWER-DOWN

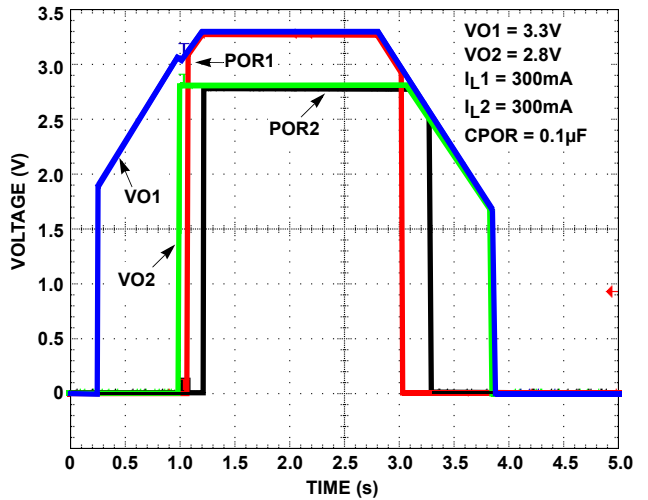


FIGURE 13. POWER-UP/POWER-DOWN WITH POR SIGNALS

Typical Performance Curves (Continued)

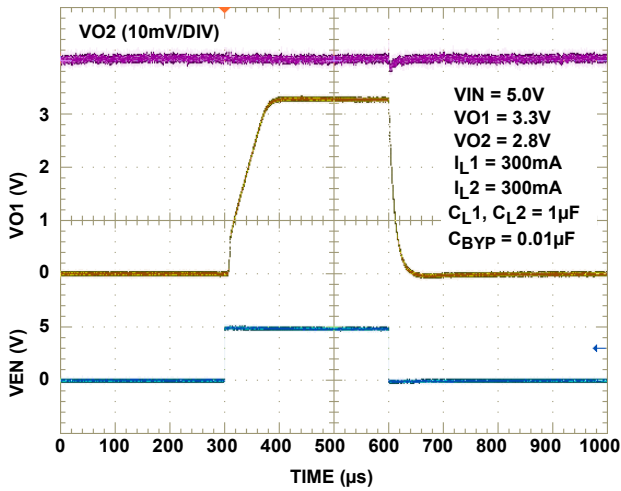


FIGURE 14. TURN ON/TURN OFF RESPONSE

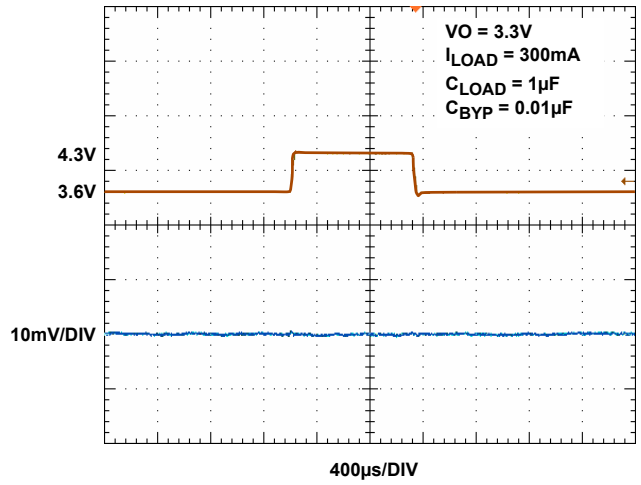


FIGURE 15. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

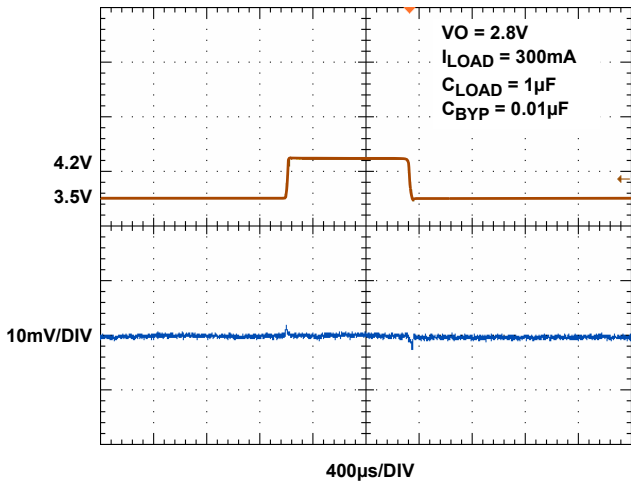


FIGURE 16. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

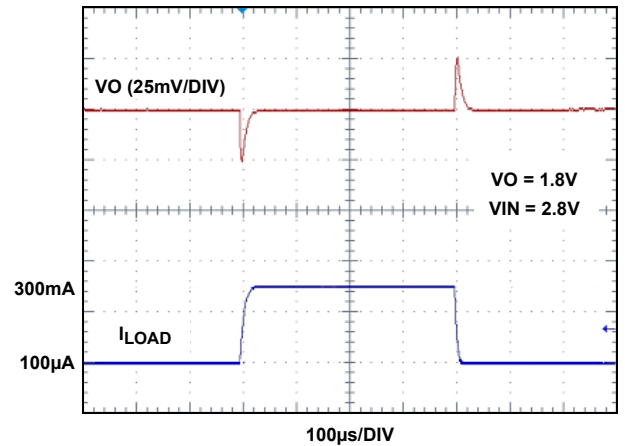


FIGURE 17. LOAD TRANSIENT RESPONSE

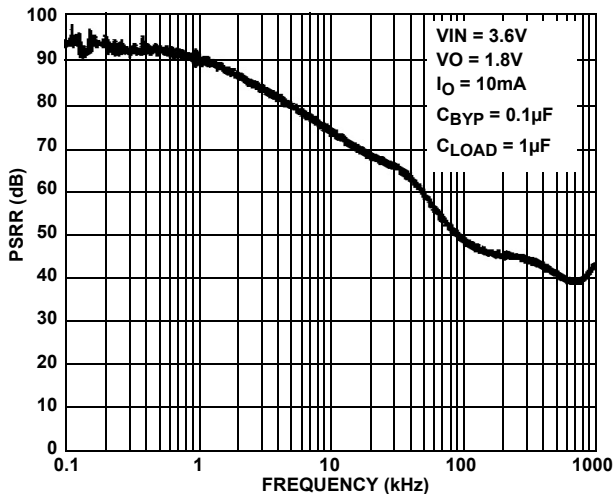


FIGURE 18. PSRR vs FREQUENCY

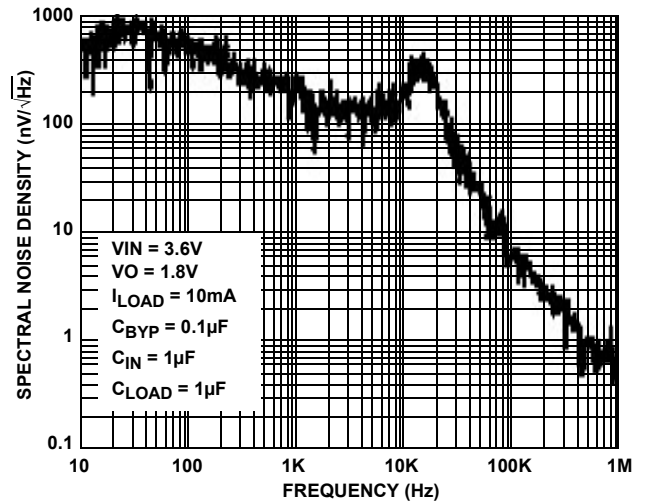


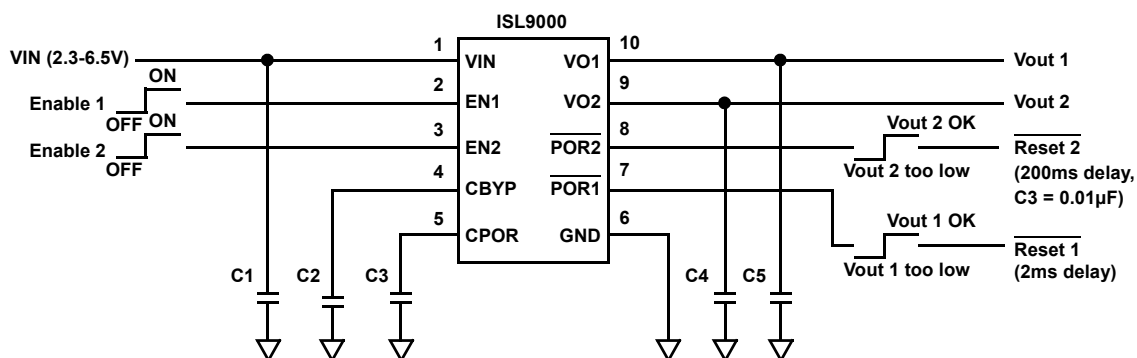
FIGURE 19. SPECTRAL NOISE DENSITY vs FREQUENCY

## ISL9000

### Pin Description

| PIN # | PIN NAME                 | TYPE                              | DESCRIPTION   |
|-------|--------------------------|-----------------------------------|---|
| 1     | VIN                      | Analog I/O                        | Supply Voltage / LDO Input:<br>Connect a 1 $\mu$ F capacitor to GND.  |
| 2     | EN1                      | Low Voltage Compatible CMOS Input | LDO-1 Enable.   |
| 3     | EN2                      | Low Voltage Compatible CMOS Input | LDO-2 Enable.   |
| 4     | CBYP                     | Analog I/O                        | Reference Bypass Capacitor Pin:<br>Optionally connect capacitor of value 0.01 $\mu$ F to 1 $\mu$ F between this pin and GND to tune in the desired noise and PSRR performance.  |
| 5     | CPOR                     | Analog I/O                        | POR2 Delay Setting Capacitor Pin:<br>Connect a capacitor between this pin and GND to delay the $\overline{\text{POR2}}$ output release after LDO-2 output reaches 94% of its specified voltage level. (200ms delay per 0.01 $\mu$ F). |
| 6     | GND                      | Ground                            | GND is the connection to system ground. Connect to PCB Ground plane.  |
| 7     | $\overline{\text{POR1}}$ | Open Drain Output (1mA)           | Open-drain POR Output for LDO-1 (active-low):<br>Internally connected to VO1 through 100k $\Omega$ resistor.  |
| 8     | $\overline{\text{POR2}}$ | Open Drain Output (1mA)           | Open-drain POR Output for LDO-2 (active-low):<br>Internally connected to VO2 through 100k $\Omega$ resistor.  |
| 9     | VO2                      | Analog I/O                        | LDO-2 Output:<br>Connect capacitor of value 1 $\mu$ F to 10 $\mu$ F to GND (1 $\mu$ F recommended).   |
| 10    | VO1                      | Analog I/O                        | LDO-1 Output:<br>Connect capacitor of value 1 $\mu$ F to 10 $\mu$ F to GND (1 $\mu$ F recommended).   |

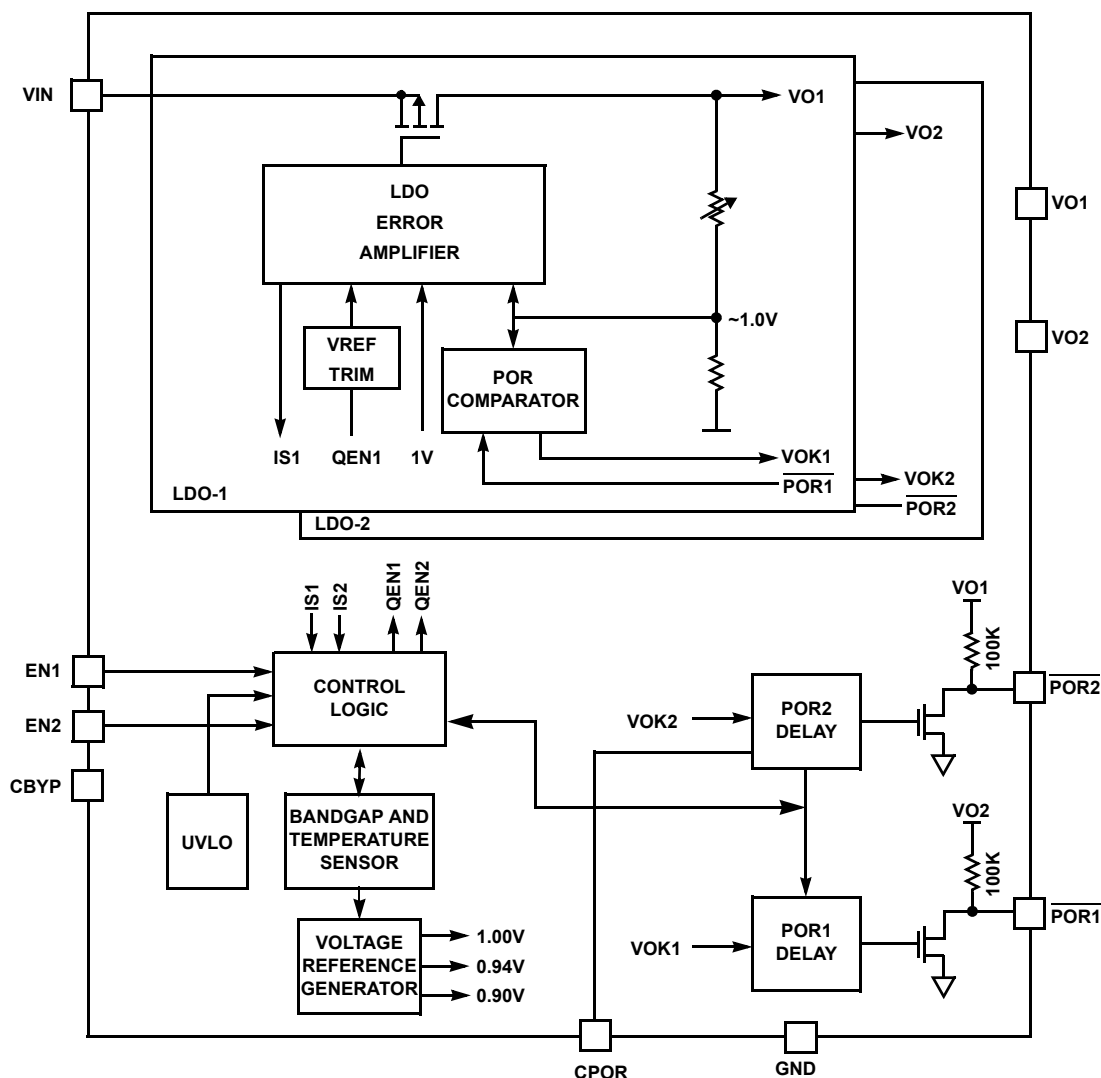
### Typical Application



- C1, C4, C5: 1 $\mu$ F X5R ceramic capacitor
- C2: 0.1 $\mu$ F X7R ceramic capacitor
- C3: 0.01 $\mu$ F X7R ceramic capacitor



## Block Diagram



## Functional Description

The ISL9000 contains two high performance LDO's. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9000 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, staged turn-on and soft-start. Smart Thermal shutdown protects the device against overheating. Staged turn-on and soft-start minimize start-up input current surges without causing excessive device turn-on time.

### Power Control

The ISL9000 has two separate enable pins, EN1 and EN2, to individually control power to each of the LDO outputs. When both EN1 and EN2 are low, the device is in shutdown

mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1 $\mu$ A.

When one or both of the enable pins are asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power up. Once the references are stable, a fast-start circuit quickly charges the external reference bypass capacitor (connected to the CBYP pin) to the proper operating voltage. After the bypass capacitor has been charged, the LDO's power up in their specified sequence.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30 $\mu$ s/V to minimize current surge.

If EN1 is brought high, and EN2 goes high before the VO1 output stabilizes, the ISL9000 delays the VO2 turn-on until the VO1 output reaches its target level. This minimizes input current surge due to concurrent turn-on.

If EN2 is brought high, and EN1 goes high before the VO2 output stabilizes, the ISL9000 delays the VO1 turn-on until the VO2 output reaches its target level.

If both EN1 and EN2 are brought high at the same time, the VO1 output has priority, and is always powered up first.

During operation, whenever the VIN voltage drops below about 1.8V, the ISL9000 immediately disables both LDO outputs. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

## Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01 $\mu$ F capacitor connected CBYP implements a 100Hz lowpass filter, and is recommended for most high performance applications. For the lowest noise application, a 0.1 $\mu$ F or greater CBYP capacitor should be used. This filters the reference noise to below the 10Hz – 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference, POR detection thresholds, and other voltage references required for current generation and over-temperature detection.

The current generator provides the references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

## LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9000 provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1 $\mu$ F to 10 $\mu$ F output capacitor that has a tolerance better than 20% and ESR less than 200m $\Omega$ . The design is performance-optimized for a 1 $\mu$ F capacitor. Unless limited by the application, use of an output capacitor value above 4.7 $\mu$ F is not normally needed as LDO performance improvement is minimal.

Each LDO uses an independently trimmed 1V reference. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory to one of the following output voltages: 1.5V, 1.8V, 1.85, 2.5V, 2.6, 2.7, 2.8V, 2.85V, 2.9, 3.0, and 3.3V.

## Power On Reset Generation

Each LDO has a separate Power-on Reset signal generation circuit which outputs to the respective  $\overline{\text{POR}}$  pins. The POR signal is generated as follows:

A POR comparator continuously monitors the output of each LDO. The LDO enters a power-good state when the output voltage is above 94% of the expected output voltage for a period exceeding the LDO PGOOD entry delay time (see below). In the power-good state, the open-drain  $\overline{\text{PORx}}$  output is in a high-impedance state. An internal 100k $\Omega$  pull-up resistor pulls the pin up to the respective LDO output voltage. An external resistor can be added between the  $\overline{\text{PORx}}$  output and the LDO output for a faster rise time, however, the  $\overline{\text{PORx}}$  output should not connect through an external resistor to a supply greater than the associated LDO voltage.

The power-good state is exited when the LDO output falls below 90% of the expected output voltage for a period longer than the PGOOD exit delay time. While power-good is false, the ISL9000 pulls the respective  $\overline{\text{POR}}$  pin low.

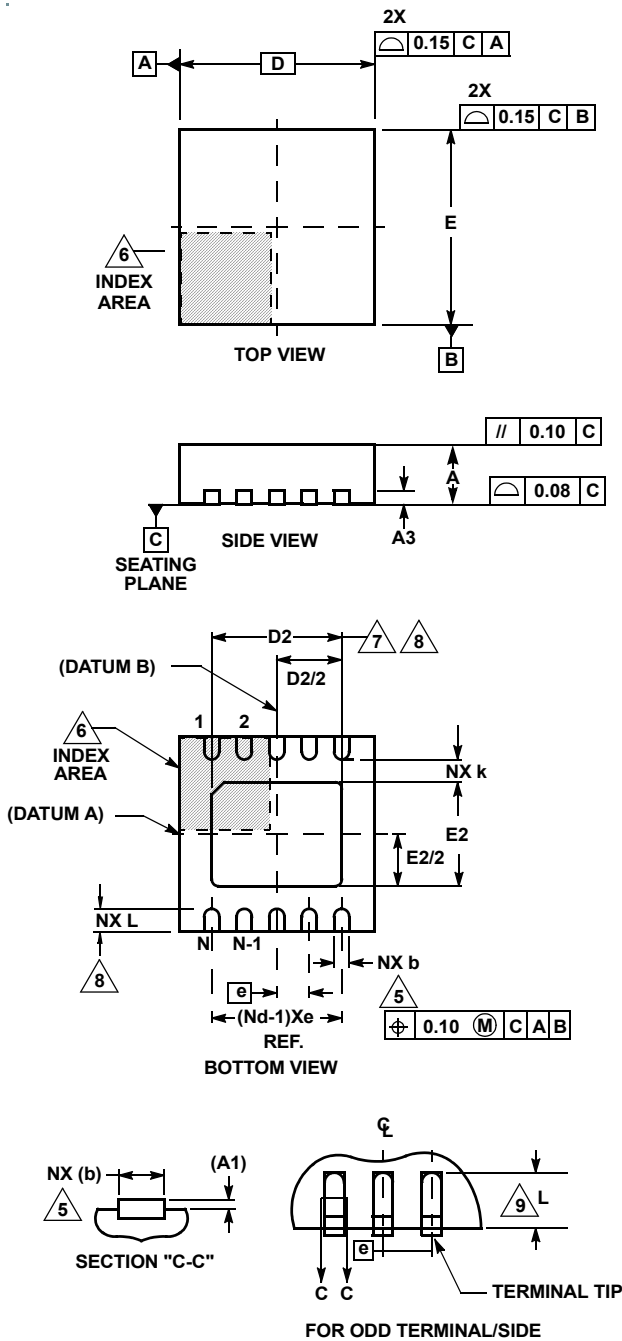
For LDO-1, the PGOOD entry delay time is fixed at about 2ms while the PGOOD exit delay is about 25 $\mu$ s. For LDO-2, the PGOOD entry and exit delays are determined by the value of the external capacitor connected to the CPOR pin. For a 0.01 $\mu$ F capacitor, the entry and exit delays are 200ms and 25 $\mu$ s respectively. Larger or smaller capacitor values will yield proportionately longer or shorter delay times. The POR exit delay should never be allowed to be less than 10 $\mu$ s to ensure sufficient immunity against transient induced false POR triggering.

## Overheat Detection

The bandgap provides a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about 145°C, one or both of the LDO's momentarily shut down until the die cools sufficiently. In the overheat condition, only the LDO sourcing more than 50mA will be shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs are disabled. Once the die temperature falls back below about 110°C, the disabled LDO(s) are re-enabled and soft-start automatically takes place.

The ISL9000 provides short-circuit protection by limiting the output current to about 475mA. If short circuited, an output current of 475mA will cause die heating. If the short circuit lasts long enough, the overheat detection circuit will turn off the output.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

| SYMBOL | MILLIMETERS |         |      | NOTES |
|--------|-------------|---------|------|-------|
|        | MIN         | NOMINAL | MAX  |       |
| A      | 0.80        | 0.90    | 1.00 | -     |
| A1     | -           | -       | 0.05 | -     |
| A3     | 0.20 REF    |         |      | -     |
| b      | 0.18        | 0.25    | 0.30 | 5, 8  |
| D      | 3.00 BSC    |         |      | -     |
| D2     | 2.23        | 2.38    | 2.48 | 7, 8  |
| E      | 3.00 BSC    |         |      | -     |
| E2     | 1.49        | 1.64    | 1.74 | 7, 8  |
| e      | 0.50 BSC    |         |      | -     |
| k      | 0.20        | -       | -    | -     |
| L      | 0.30        | 0.40    | 0.50 | 8     |
| N      | 10          |         |      | 2     |
| Nd     | 5           |         |      | 3     |

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

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