

**KS0065B**

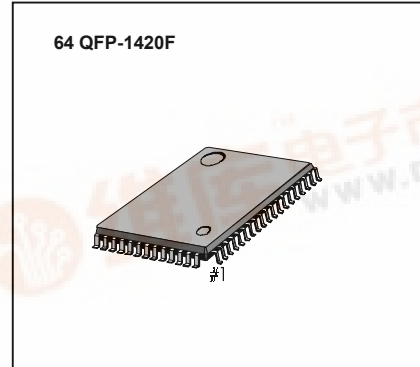
**40CH SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD**

**INTRODUCTION**

The KS0065B is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 20 x 2bit bi-directional shift register, 20 x 2bit data latch and 20 x 2bit driver. (refer to Fig 1) This LSI can be used as common or segment driver.

**FUNCTION**

- Dot matrix LCD driver with 40 channel output.
- Selects function to use common/segment drivers simultaneously.
- Input / Output signal
  - output : 20 x 2 channel waveform for LCD driving
  - input : - Serial display data and control signal from the controller LSI.
    - Bias voltage (V<sub>1</sub>~V<sub>6</sub>)



**FEATURES**

- Display driving bias : static~1/5
- Power supply voltage : 2.7 ~ 5.5V
- Supply voltage for display : 3.0 ~ 13.0V (V<sub>LCD</sub>=V<sub>DD</sub>-V<sub>EE</sub>)
- Interface

Driver (cascade connection)	Controller
Other KS0065B, KS0063B	KS0066U KS0070B KS0073

- CMOS Process
- 64QFP and bare chip available



BLOCK DIAGRAM

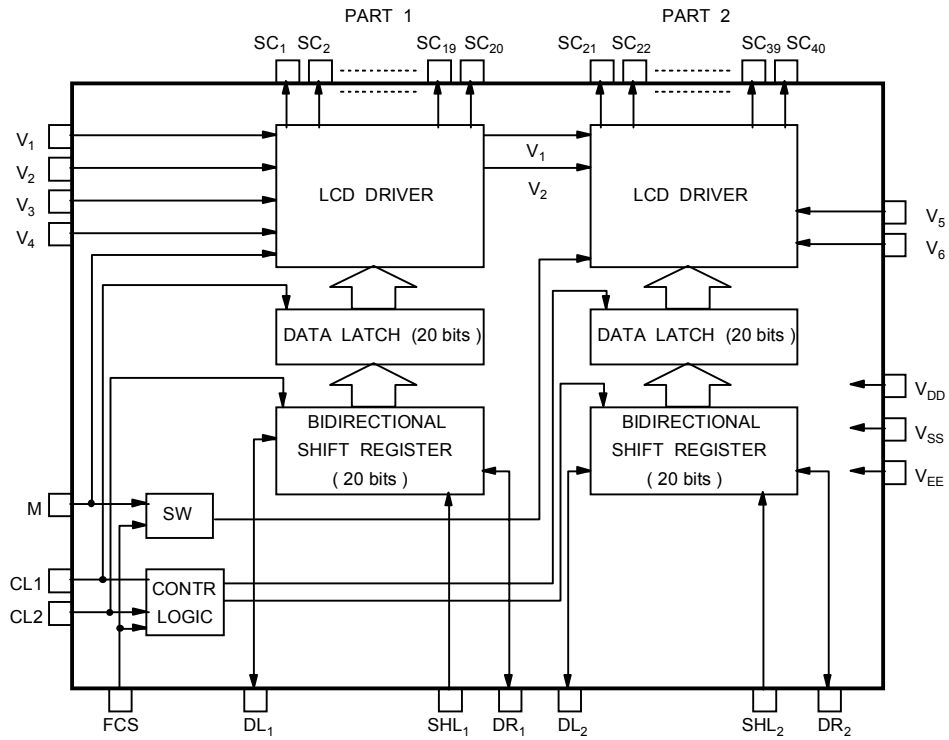


Fig 1. KS0065B functional block diagram

PIN CONFIGURATION

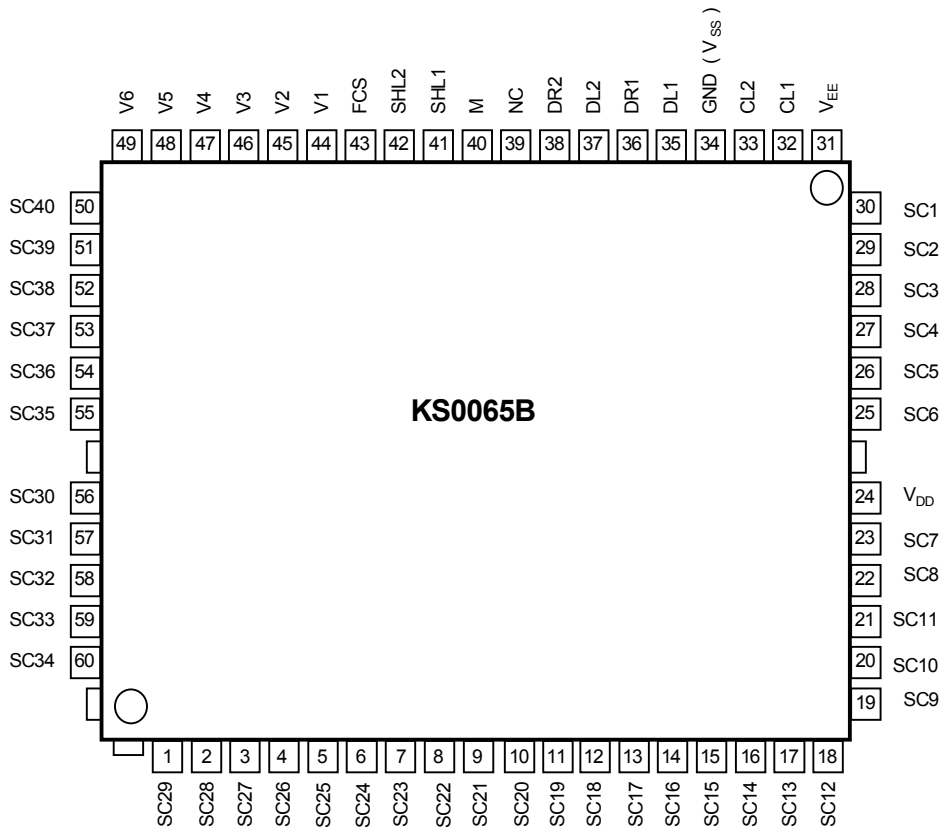
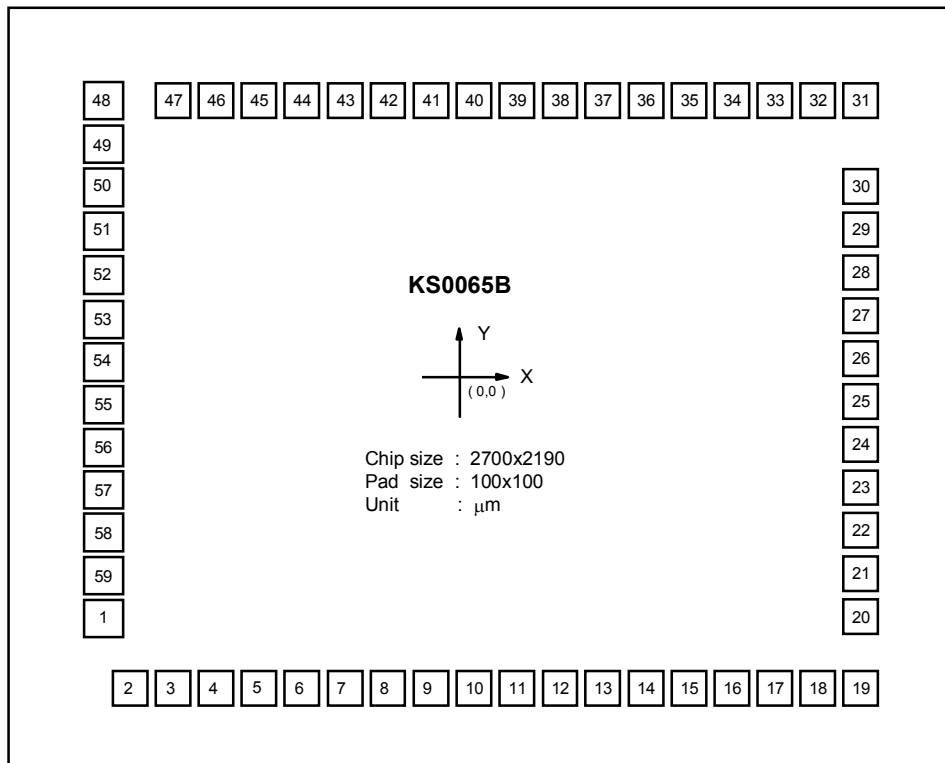


Fig 2. 60 QFP Top View

PAD DIAGRAM



Note : (0,0) is center in the chip

## PAD LOCATION

UNIT ( $\mu\text{m}$ )

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
1	VEE	-1120.2	-642.5	31	SC28	1117.5	865.2
2	CL1	-1062.5	-865.2	32	SC27	992.5	865.2
3	CL2	-937.5	-865.2	33	SC26	867.5	865.2
4	VSS	-812.5	-865.2	34	SC25	742.5	865.2
5	DL1	-687.5	-865.2	35	SC24	617.5	865.2
6	DR1	-562.5	-865.2	36	SC23	492.5	865.2
7	DL2	-437.5	-865.2	37	SC22	367.5	865.2
8	DR2	-312.5	-865.2	38	SC21	242.5	865.2
9	M	-187.5	-865.2	39	SC20	117.5	865.2
10	SHL1	-62.5	-865.2	40	SC19	-7.5	865.2
11	SHL2	62.5	-865.2	41	SC18	-132.5	865.2
12	FCS	187.5	-865.2	42	SC17	-257.5	865.2
13	V1	332.5	-865.2	43	SC16	-382.5	865.2
14	V2	457.5	-865.2	44	SC15	-507.5	865.2
15	V3	582.5	-865.2	45	SC14	-632.5	865.2
16	V4	707.5	-865.2	46	SC13	-757.5	865.2
17	V5	832.5	-865.2	47	SC12	-882.5	865.2
18	V6	957.5	-865.2	48	SC9	-1120.2	857.2
19	SC40	1082.5	-865.2	49	SC10	-1120.2	732.5
20	SC39	1120.2	-627.5	50	SC11	-1120.2	607.5
21	SC38	1120.2	-502.5	51	SC8	-1120.2	482.5
22	SC37	1120.2	-377.5	52	SC7	-1120.2	357.5
23	SC36	1120.2	-252.5	53	VDD	-1120.2	232.5
24	SC35	1120.2	-127.5	54	SC6	-1120.2	107.5
25	SC30	1120.2	-2.5	55	SC5	-1120.2	-17.5
26	SC31	1120.2	122.5	56	SC4	-1120.2	-142.5
27	SC32	1120.2	247.5	57	SC3	-1120.2	-267.5
28	SC33	1120.2	372.5	58	SC2	-1120.2	-392.5
29	SC34	1120.2	497.5	59	SC1	-1120.2	-517.5
30	SC29	1120.2	622.5				

## PIN DESCRIPTION

PIN(NO.)	INPUT/ OUTPUT	NAME	DESCRIPTION	INTERFACE																					
V <sub>DD</sub> (24)	Power	Operating Voltage	For logical circuit (2.7 ~ 5.5V)	Power Supply																					
GND(34)			0V (GND)																						
V <sub>EE</sub> (31)		Negative Supply Voltage	For LCD driver circuit																						
V <sub>1</sub> , V <sub>2</sub> (44,45)	Input	Bias Voltage	Bias voltage level for LCD drive (select level)	Power																					
SC <sub>1</sub> ~SC <sub>20</sub>	Output	Part 1	LCD driver	LCD driver output	LCD																				
V <sub>3</sub> , V <sub>4</sub> (46, 47)	Input		Bias Voltage	Bias voltage level for LCD drive (non-select level)	Power																				
SHL1 (41)	Input		Data interface	Selection of the shift direction of Part 1 shift register <table border="1" style="margin: 5px auto;"> <tr> <td>SHL1</td> <td>DL1</td> <td>DR1</td> </tr> <tr> <td>V<sub>DD</sub></td> <td>out</td> <td>in</td> </tr> <tr> <td>V<sub>SS</sub></td> <td>in</td> <td>out</td> </tr> </table>	SHL1	DL1	DR1	V <sub>DD</sub>	out	in	V <sub>SS</sub>	in	out	V <sub>DD</sub> or V <sub>SS</sub>											
SHL1	DL1		DR1																						
V <sub>DD</sub>	out	in																							
V <sub>SS</sub>	in	out																							
DL1, DR1 (35, 36)	Input Output		Data input/output of Part 1 shift register	Controller or KS0065B																					
SC <sub>21</sub> ~SC <sub>40</sub>	Output	Part 2	LCD driver	LCD driver output																					
V <sub>5</sub> , V <sub>6</sub> (48, 49)	Input		Bias Voltage	Bias voltage level for LCD drive (non-select level)	Power																				
SHL2 (42)	Input		Data interface	Selection of the shift direction of Part 2 shift register <table border="1" style="margin: 5px auto;"> <tr> <td>SHL2</td> <td>DL2</td> <td>DR2</td> </tr> <tr> <td>V<sub>DD</sub></td> <td>out</td> <td>in</td> </tr> <tr> <td>V<sub>SS</sub></td> <td>in</td> <td>out</td> </tr> </table>	SHL2	DL2	DR2	V <sub>DD</sub>	out	in	V <sub>SS</sub>	in	out	V <sub>DD</sub> or V <sub>SS</sub>											
SHL2	DL2		DR2																						
V <sub>DD</sub>	out	in																							
V <sub>SS</sub>	in	out																							
DL2, DR2 (37, 38)	Input Output		Data input/output of Part 2 shift register	Controller or KS0065B																					
M (40)	Input	Alternated signal for LCD driver output	<table border="1" style="margin: 5px auto;"> <thead> <tr> <th>PART</th> <th>FCS</th> <th>CL1</th> <th>CL2</th> <th>M polarity</th> </tr> </thead> <tbody> <tr> <td rowspan="2">1</td> <td>V<sub>SS</sub></td> <td>latch clock (  )</td> <td>shift clock (  )</td> <td rowspan="2">M</td> </tr> <tr> <td>V<sub>DD</sub></td> <td></td> <td></td> </tr> <tr> <td rowspan="2">2</td> <td>V<sub>SS</sub></td> <td></td> <td>shift clock (  )</td> <td rowspan="2"><math>\bar{M}</math></td> </tr> <tr> <td>V<sub>DD</sub></td> <td>shift clock (  )</td> <td>latch clock (  )</td> </tr> </tbody> </table>	PART	FCS	CL1	CL2	M polarity	1	V <sub>SS</sub>	latch clock (  )	shift clock (  )	M	V <sub>DD</sub>			2	V <sub>SS</sub>		shift clock (  )	$\bar{M}$	V <sub>DD</sub>	shift clock (  )	latch clock (  )	Controller
PART	FCS	CL1		CL2	M polarity																				
1	V <sub>SS</sub>	latch clock (  )		shift clock (  )	M																				
	V <sub>DD</sub>																								
2	V <sub>SS</sub>		shift clock (  )	$\bar{M}$																					
	V <sub>DD</sub>	shift clock (  )	latch clock (  )																						
CL1, CL2 (32,33)	Input	Data shift /latch clock																							
FCS(43)	Input	Mode selection	Shift/latch clock of display data and polarity of M signal are changed by FCS signal. By setting FCS to V <sub>DD</sub> level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.																						
NC(39)			No connection pin	N.C																					

**MAXIMUM ABSOLUTE LIMIT** ( $T_a=25^\circ\text{C}$ )

Characteristic	Symbol	Value	Unit
Operating Voltage	$V_{DD}$	-0.3 ~ +7.0	V
Driver Supply Voltage	$V_{LCD}$	$V_{DD}-15.0 \sim V_{DD}+0.3$	V
Input Voltage 1	$V_{IN1}$	-0.3 ~ $V_{DD}+0.3$	V
Input Voltage 2 ( $V_1-V_6$ )	$V_{IN2}$	$V_{DD}+0.3 \sim V_{EE}-0.3$	V
Operating Temperature	$T_{OPR}$	-30 ~ +85	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +125	$^\circ\text{C}$

\* Voltage greater than above may damage the circuit

\*  $V_{EE}$ : connect a protection resistor ( $220\Omega \pm 5\%$ )

**ELECTRICAL CHARACTERISTICS****DC CHARACTERISTICS** ( $V_{DD}=2.7 \sim 5.5\text{V}$ ,  $V_{DD}-V_{EE}=3 \sim 13\text{V}$ ,  $V_{SS}=0\text{V}$ ,  $T_a=-30 \sim +85^\circ\text{C}$ )

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	$I_{DD}$	$f_{CL2}=400\text{KHz}$	-	1	mA	-
Supply Current *	$I_{EE}$	$f_{CL1}=1\text{KHz}$	-	10	$\mu\text{A}$	
Input High Voltage	$V_{IH}$	-	$0.7 V_{DD}$	$V_{DD}$	V	CL1, CL2, DL1, DL2 DR1, DR2, SHL1, SHL2
Input Low Voltage	$V_{IL}$		0	$0.3 V_{DD}$		
Input Leakage Current	$I_{LKG}$	$V_{IN}=0-V_{DD}$	-5	5	$\mu\text{A}$	M, FCS
Output High Voltage	$V_{OH}$	$I_{OH}=-0.4\text{mA}$	$V_{DD}-0.4$	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	$V_{OL}$	$I_{OL}=+0.4\text{mA}$	-	0.4		
Voltage Descending	$V_{D1}$	$I_{ON}=0.1\text{mA}$ for one of SC1-SC40	-	1.1		
	$V_{D2}$	$I_{ON}=0.05\text{mA}$ for each SC1-SC40	-	1.5		
Leakage Current	$I_V$	$V_{IN}=V_{DD} \sim V_{EE}$ (Output SC1-SC40 : floating)	-10	10	$\mu\text{A}$	V1-V6

**AC CHARACTERISTICS** ( $V_{DD}=2.7 \sim 5.5\text{V}$ ,  $V_{DD}-V_{EE}=3 \sim 13\text{V}$ ,  $V_{SS}=0\text{V}$ ,  $T_a=-30 \sim +85^\circ\text{C}$ )

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	$f_{CL}$	-	-	400	KHz	CL2
Clock High Level Width	$t_{WCKH}$	-	800	-	ns	CL1, CL2
Clock Low Level Width	$t_{WCKL}$	-	800	-		CL2
Clock Set-up Time	$t_{SL}$	from CL2 to CL1	500	-		CL1, CL2
	$t_{LS}$	from CL1 to CL2	500	-		
Clock Rise/Fall Time	$t_R/t_F$	-	-	200		DL1, DL2, DR1, DR2, FLM
Data Set-up Time	$t_{SU}$	-	300	-		
Data Hold Time	$t_{DH}$	-	300	-		
Data Delay Time	$t_D$	CL=15pF	-	500	DL1, DL2, DR1, DR2	

\* Input/Output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at "H" or "L".



**TIMING CHARACTERISTICS**

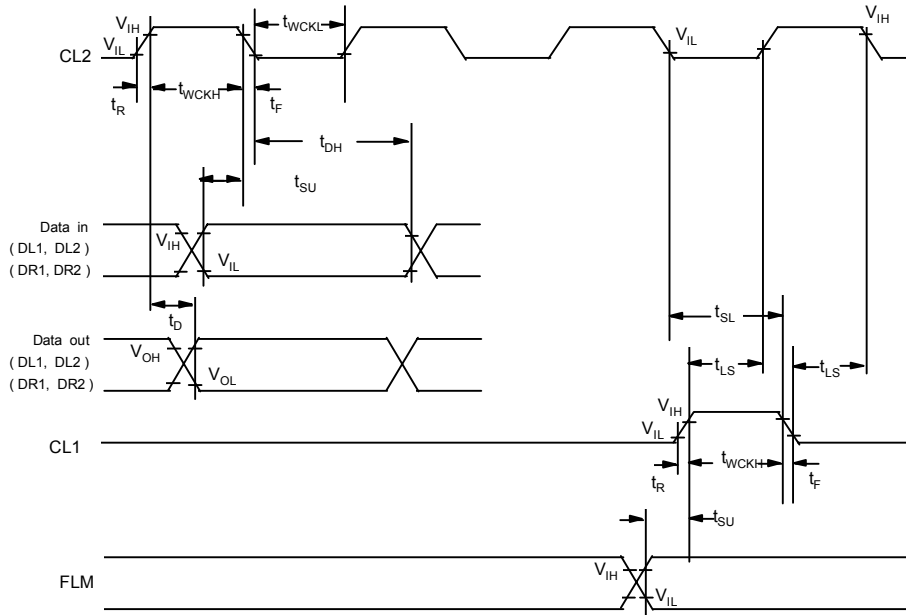


Fig 3. AC characteristics

**FUNCTIONAL DESCRIPTION**

1) To drive segment type

When the FCS is connected to Vss, KS0065B(SC1-SC40)is operated as segment driver.(refer to Fig 4)

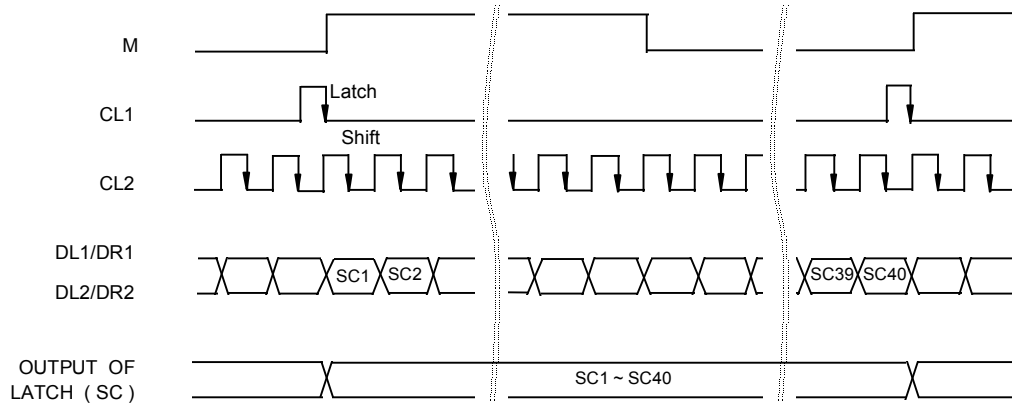


Fig 4. Segment Data Waveforms



2) To drive common type

When the FCS is connected to  $V_{DD}$ , only part2(SC21-SC40)of KS0065B is operated as common driver.(refer to Fig 5).

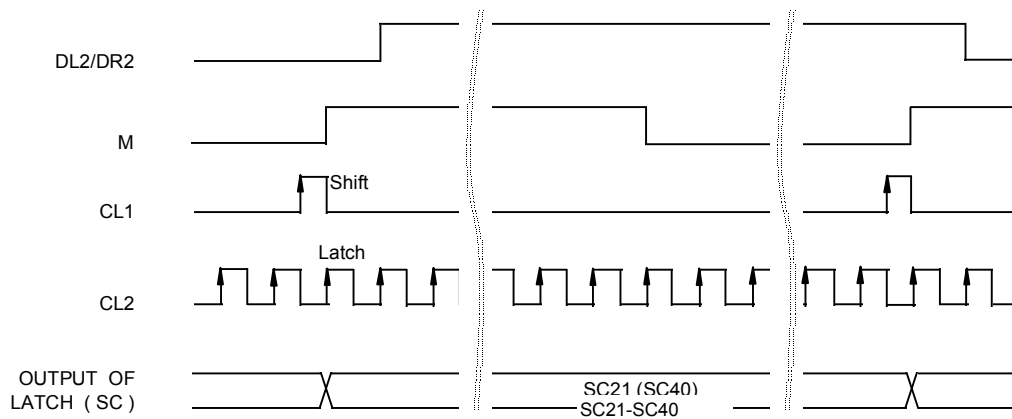


Fig 5. Common Data waveforms

LCD OUTPUT WAVEFORMS

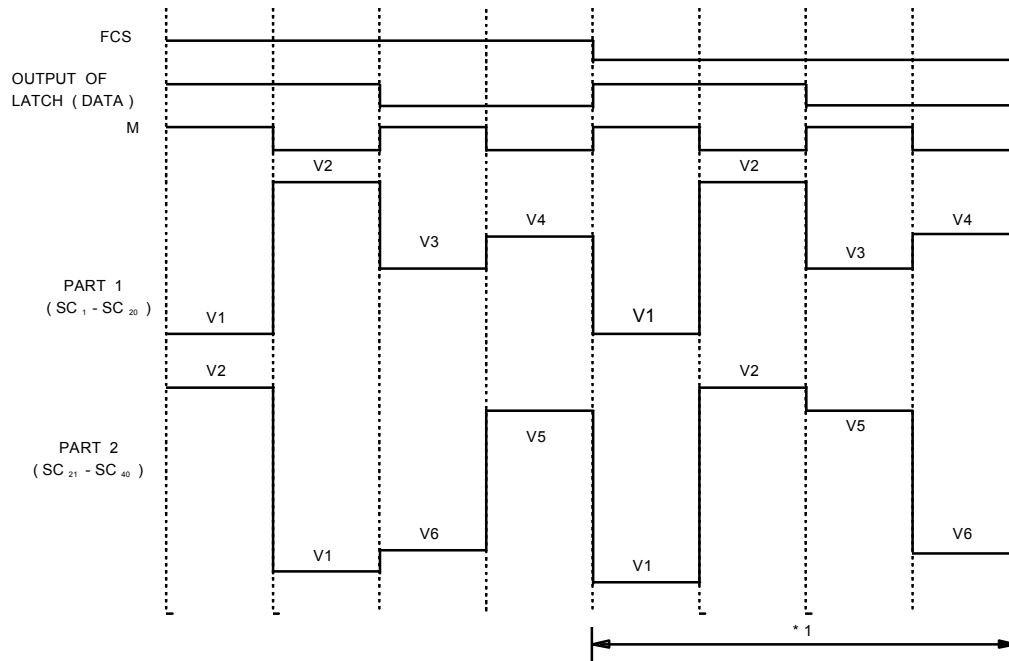
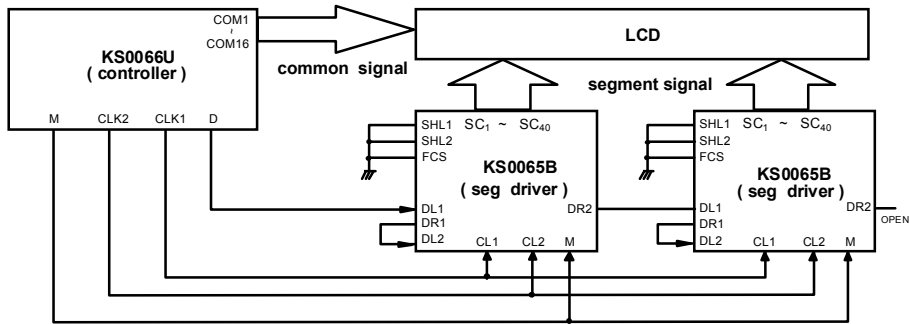


Fig. 6. Output waveform

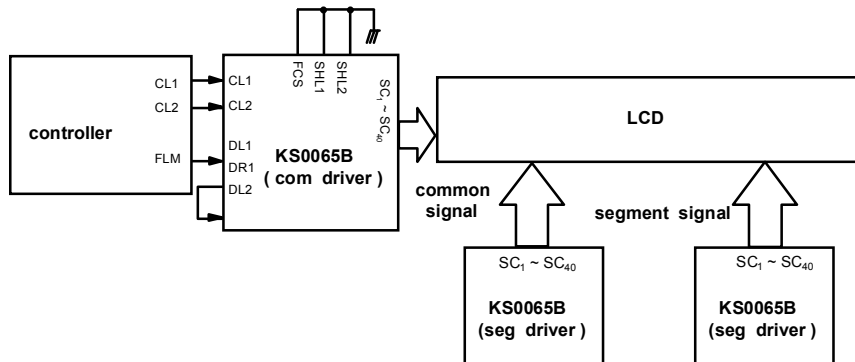
\*1: To use for same function of part 1 and part 2, V3 and V5 only for LCD drive are short circuited respectively.

APPLICATION CIRCUIT

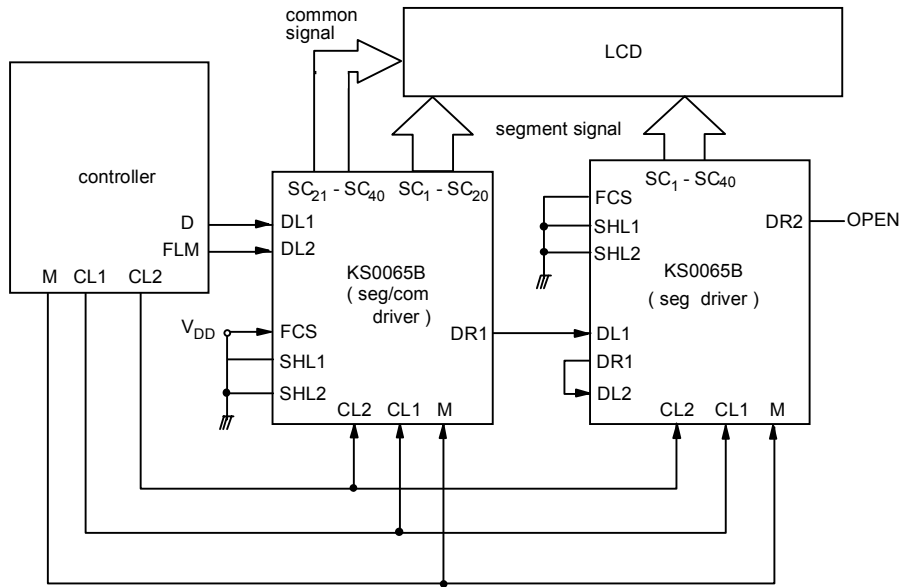
1) Segment driver



2) Common driver



3) Segment/common driver



# 64-QFP-1420F

Dimensions in Millimeters

