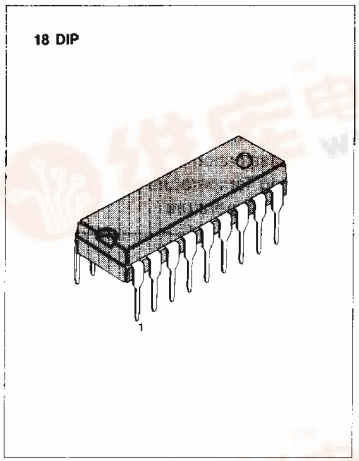
KS5805A/KS5805B CMOS INTEGRATED CIRCUIT

TELEPHONE PULSE DIALER WITH REDIAL

The KS5805A/B is a monolithic CMOS integrated circuit and provides all the features required for implementing a pulse dialer with redial.



FUNCTIONS

- $\overline{\text{Mute}}$ output logic "0"
- $\overline{\text{Pulse}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation
- Power up clear circuitry
- KS5805A pin 2: V_{REF}
- KS5805B pin 2: Tone out

FEATURES

- **Uses either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Tone signal output or on-chip reference Voltage by bonding option on chip**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS5805AN	18 DIP	Pin 2 = V_{ref}	−30 ~ +60°C
KS5805BN	18 DIP	Pin 2 = Tone Out	

TEST CIRCUIT

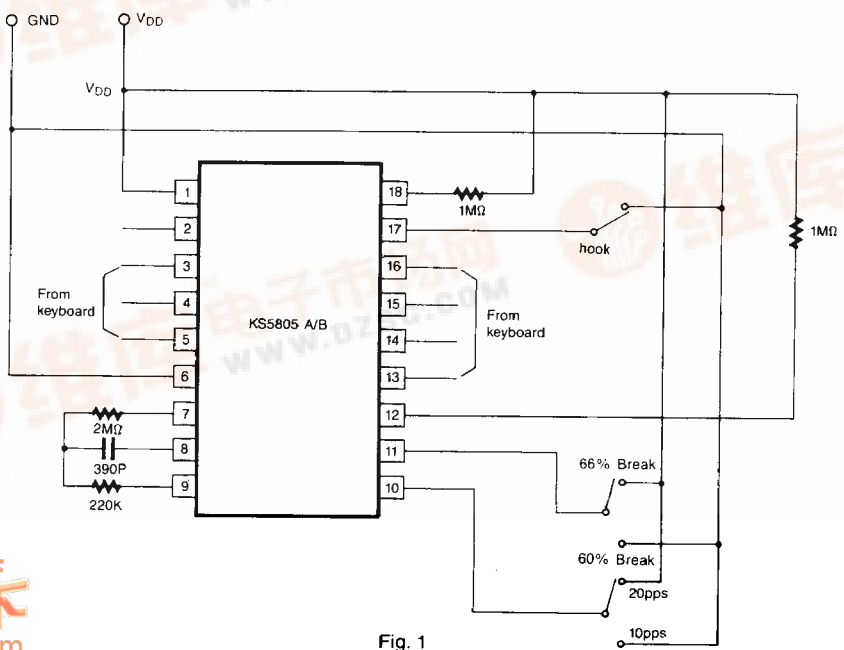


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	6.2	V
Voltage on Any Pin	V_{IN}	V_{DD} +0.3, Gnd−0.3	V
Power Dissipation	P_D	500.0	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

DC ELECTRICAL CHARACTERISTICS

(T_a=25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}		2.5		6.0	V	
Key Contract Resistance	R_{KI}				1	KΩ	1
Keyboard Capacitance	C_{KI}				30	pF	
Key Input Voltage	K_{IH}	2 of 7 input mode	0.8V_{DD}		V_{DD}	V	1
	K_{IL}		Gnd		0.2V_{DD}		
Key Pull-Up Resistance	K_{IRU}	V_{DD} = 6.0V		100		KΩ	
Key Pull-Down Resistance	K_{IRD}	V_{IN} = 4.8V		4.0		KΩ	
Mute Sink Current	I_M	V_{DD} = 2.5V V_O = 0.5V	500			μA	2
Pulse Output Sink Current	I_P	V_{DD} = 2.5V V_O = 0.5V	1.0			mA	3
Tone Output Sink Current	I_{TL}	V_{DD} = 2.5V V_O = 0.5V	250			μA	4
Tone Output Source Current	I_{TH}	V_{DD} = 2.5V V_O = 0.5V	250			μA	4
Memory Retention Current	I_{MR}	All outputs under no load		0.7		μA	6
Operating Current	I_{OP}	All outputs under no load		100	150	μA	
Mute or Pulse Off Leakage	I_{LKG}	V_{DD} = 6.0V V_O = 6.0V		0.001	1.0	μA	2.3
V_{REF} Output Source Current	I_{REF}	$V_{DD} - V_{REF}$ = 6.0V	1.0	7.0		mA	5

Note 1) Applies to key input pin. (R_1-R_4, C_1-C_3)
2) Applies to MUTE output in.
3) Applies to PULSE output pin.
4) Applies to TONE pin (KS5805B)
5) Applies to V_{REF} pin (KS5805A)
6) Current necessary for memory to be maintained. All outputs unloaded.

* Typical values are to be used as a design aid are not subject to production testing.

AC ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Charactistic	Symbol	Min	Typ	Max	Unit	Notes
Oscilator Frequency	F_{OSC}		4		KHz	1
Key Input Debounce Time	T_{DB}		10		ms	3,4
Key Down Time for Valid Entry	T_{KD}	40			ms	4,5
Key Down Time During Two-Key Roll Over	t_{KR}	5			ms	4
Oscillator Stat-Up Time (V_{DD} = 2.5V)	t_{os}		1		ms	
Mute Valid After Last Outpulse	t_{MO}		5		ms	3,4
Pulse Output Pulse Rate	P_R		10		PPS	2
On-Hook Time Required to Clear Memory	t_{OH}	300			ms	4
Pre-Digital Pause	T_{PDP}		800		ms	3,4
Inter-Digital Pause	T_{IDP}		800		ms	3,4
Frequency Stability V_{DD} = 2.5 ~ 3.5V	Δf		±4		%	
Frequency Stability V_{DD} = 3.5 ~ 6.0V	Δf		±4		%	
Tone Output Frequency	F_{TONE}		1		KHz	4,6

Note: 1) R_S = 2MΩ, R=220KΩ, C=390pF.
2) If pin 10 is tied to V_{CC}, the output pulse rate will be 20pps.
3) If the 20pps option is selected, the time will be 1/2 these shown.
4) These times are directly proportional to the oscillator frequency.
5) Debounce plus oscillator start-up time ≤ 40ms.
6) If the 20pps option is selected, the tone output frequency will be 2KHz. (KS5805B ONLY)

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS5805A)/Pacifier tone (KS5805B)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute Output}}$
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: $\overline{\text{On-Hook/Test}}$
Pin 18: $\overline{\text{Pulse Output}}$

TIMING CHARACTERISTICS

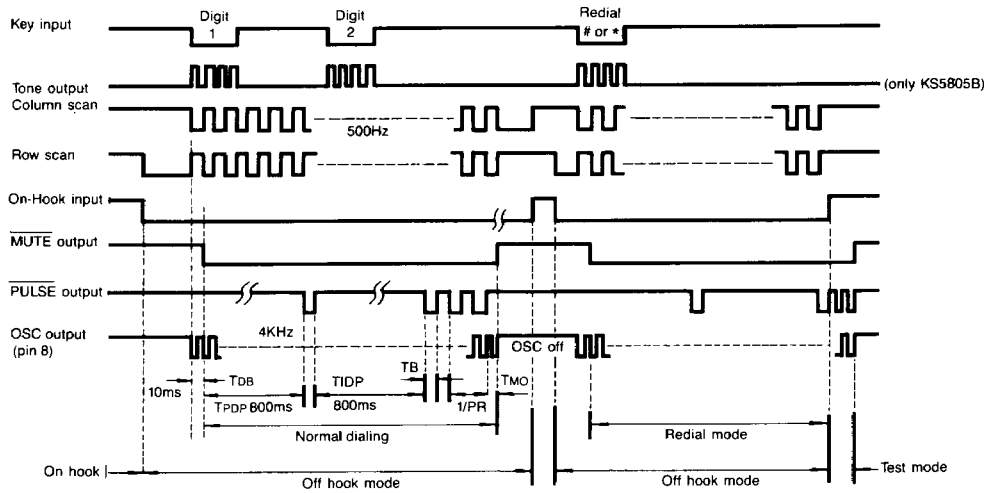


Fig. 2

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS comperementaly output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. Tone signal frequency is 1KHz when 10pps pulse rate is selected. (the frequency is 2KHz when 20pps pulse rate is selected). Only the pin 2 of KS5805A is V_{REF} (on-chip reference voltage).

TYPICAL I-V CHARACTERISTICS

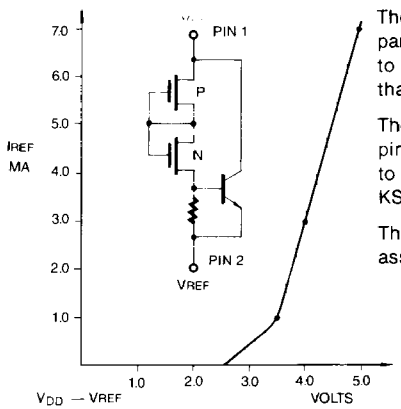


Fig. 3

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS5805A. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volt higher than the minimum operating voltage of each particular KS5805A.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS5805A is guaranteed.

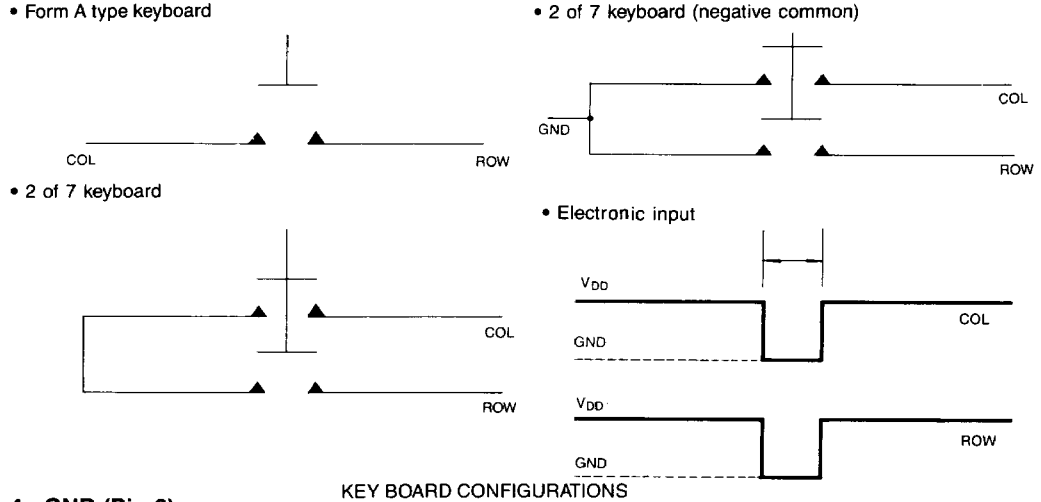
The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5805A/B incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valied key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 10msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

5. OSCILLATOR (Pins 7, 8, 9)

The KS5805A/B contains on-chip inverters to provide oscillator which will operate with a minimum external components.

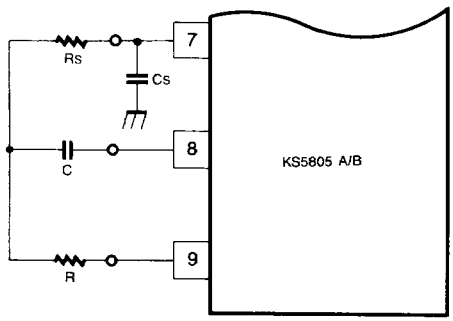
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$T=RC\,(1.386+(3.5KC_S)/C-(\pm K/(K+1))\,\ln\,(K/(1.5K+0.5))$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	34%	66%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{mute}}$ output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to $\overline{\text{mute}}$ the receiver during outpulsing. As shown in Fig. 2 the KS5805 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

The "ON-HOOK" or "Test" input of the KS5805A/B has a 100KΩ pull-up to the positive supply. A V_{CC} input or allowing the pin to float sets the circuit in its on-hook or test mode while a V_{GND} input sets it in the off-hook or normal mode. When off-hook the KS5805A/B will accept key inputs and outputs the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.
Switching the KS5805A/B to on-hook while it is outpulsing causes the remaining digits to be outpulsed at 100x the normal rate (M/B ratio is then 50/50).
This feature provides a means of rapidly testing the device and is also on efficient method by which the circuitry is reset. When the outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuity (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is eithr a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to $\overline{\text{pulse}}$ the telephone line by disconnecting and connecting the network. The KS58A/B05 pulse output is an open circuit during make and pulls to the GND supply during break.