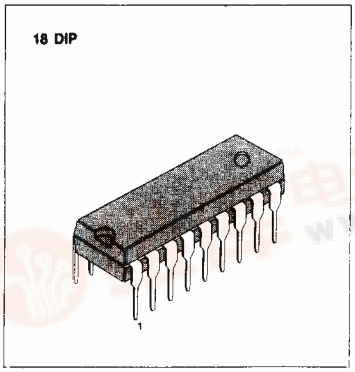
KS5851/2 CMOS INTEGRATED CIRCUIT

PULSE DIALER WITH REDIAL

The KS5851/2 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- $\overline{\text{MUTE}}$ output logic "0"
- $\overline{\text{PULSE}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

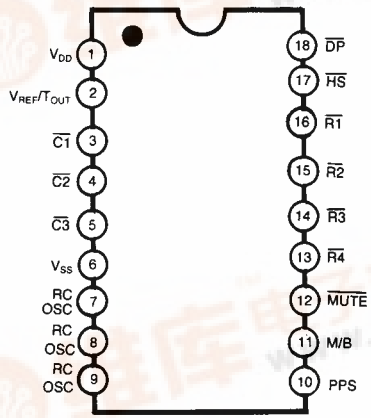
FEATURES

- **Wide operating voltage range (2.0 ~ 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Power up clear circuitry on chip**
- **KS5851 pin 2: V_{ref}, KS5852 pin 2: Tone output**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS5851	18 DIP	Pin 2 = V_{ref}	− 20 ~ + 70°C
KS5852	18 DIP	Pin 2 = Tone Out	

PIN CONFIGURATION



ARRANGEMENT OF KEYBOARD

1	2	3
4	5	6
7	8	9
*	0	#

(*, #: Redial)

Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_I	Gnd – 0.3, V_{DD} + 0.3	V
Output Voltage	V_O	Gnd – 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	– 20 ~ + 70	°C
Storage Temperature	T_{STG}	– 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{MR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, DRS, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		Gnd		0.2V_{DD}	V
Operating Current	I_{DD}	All output under no load		100	150	μA
Output Leakage Current	$I_{D(LKG)}$	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{OL1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{OL2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	t_{KD}		14		20	mS
On Hook Time Required to Clear Memory	t_{OH}		300			mS
Inter Digital Pause Time	t_{PIDP}			800		mS
Frequency Stability	ST	V_{DD} = 2.0 ~ 6.0V		± 10		%
Tone Output Frequency	$f_{O(TONE)}$			1.2		KHz

TEST CIRCUIT

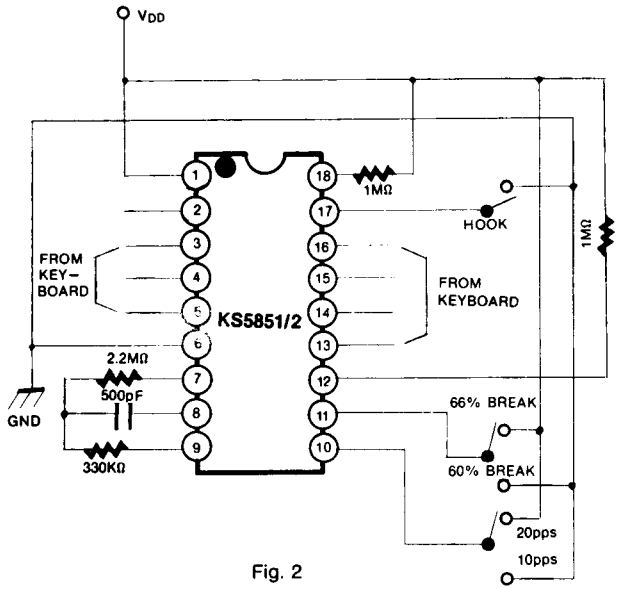


Fig. 2

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS5851)/Pacifier tone (KS5852)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse}}$ Output

APPLICATION INFORMATION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses key down condition by detecting one key input and enters the key's code into an on-chip memory.

The memory can be store up to 32 digits, and it allows key strobes to be entered at rates comparable to tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs, one to pulse the telephone line and one to mute the receiver, are provided.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum T_{OH} (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level.

This function will prevent the "Redial" or spontaneous outputing of incorrect data.

TIMING CHARACTERISTICS

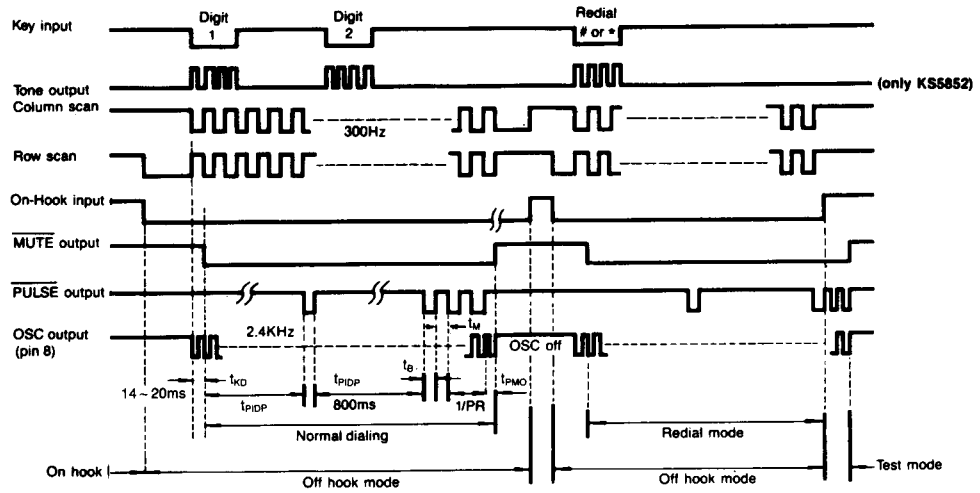


Fig. 3

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS complementally output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. Tone signal frequency is 1.2KHz when 10pps pulse rate is selected.

TYPICAL I-V CHARACTERISTICS

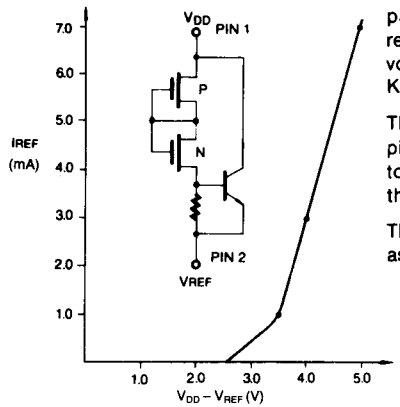


Fig. 4

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS5851. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volt higher than the minimum operating voltage of each particular KS5851.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS5851 is guaranteed.

The internal circuit of the V_{REF} function is shown in Figure 4 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5851/2 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 10msec of debounce time to be accepted.

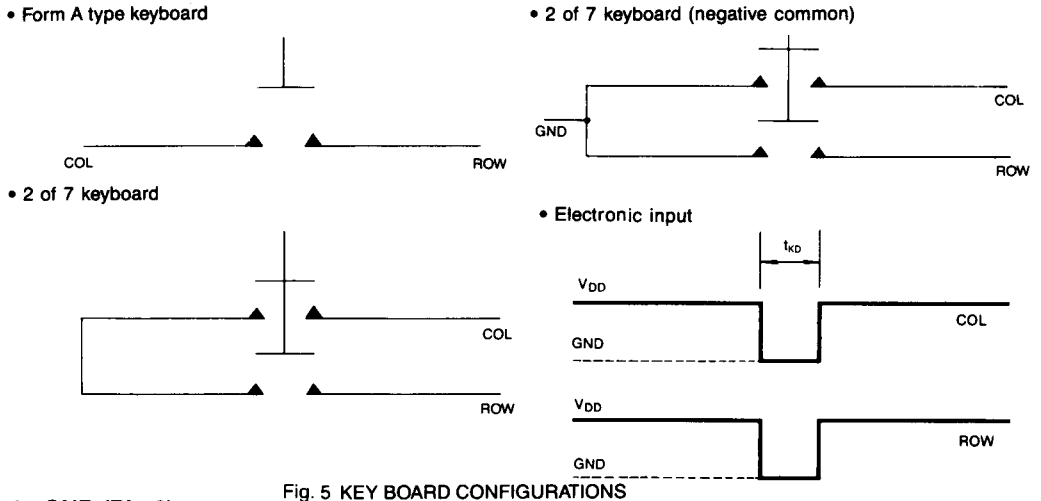


Fig. 5 KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in general applications.

5. OSCILLATOR (Pins 7, 8, 9)

The KS5851/2 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$t = RC\,[(1.386 + (3.5KC_S)/2K/(K+1))\ \ln\ (K/(1.5K+0.5))]$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.

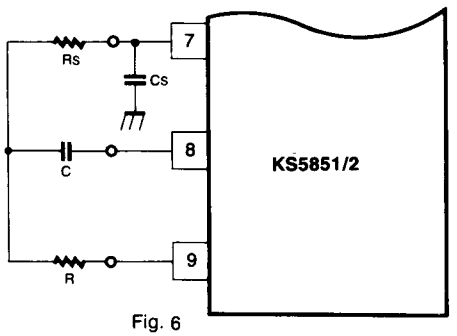


Fig. 6

6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{mute}}$ output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 3 the KS5851/2 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS5851/2 $\overline{\text{pulse}}$ output is an open circuit during make and pulls to the GND supply during break.

11. ESD PROTECTION

All Input/Output are protected ESD.

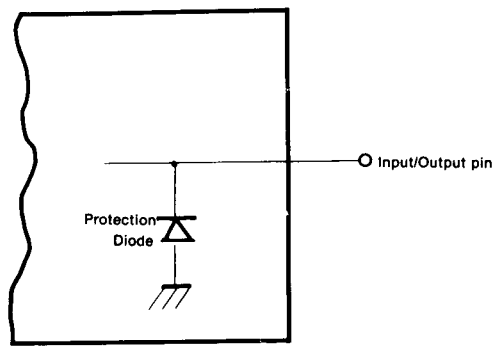


Fig. 7